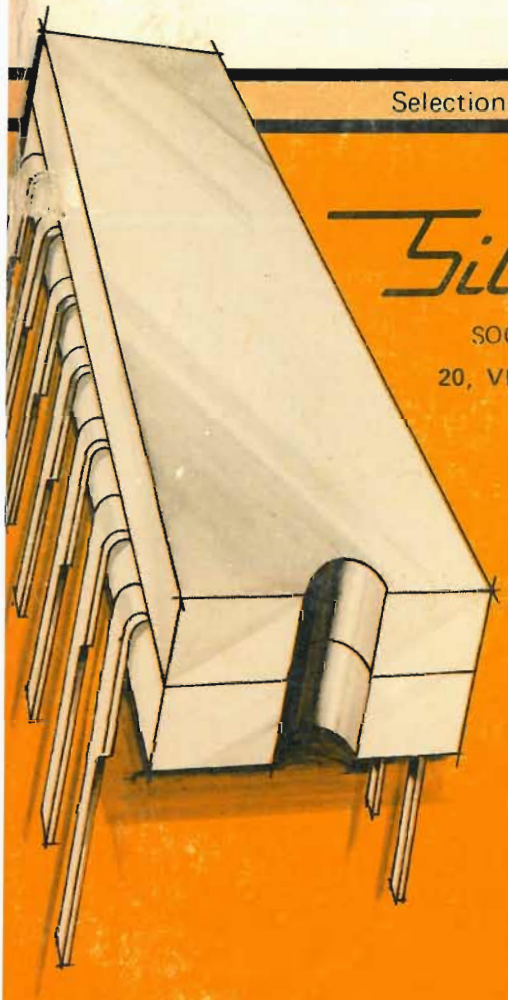
RCA

LINEAR Integrated Circuits

Selection Guide / Data



SSD-201C
1975 DATABOOK Series

RCA Solid State

A New Approach To Data Service . . .

1975 RCA Solid State DATABOOKS

Seven textbook-size volumes covering all current commercial RCA solid-state devices (through January 1, 1975)

Linear Integrated Circuits and DMOS Devices (Data only) SSD-201C
Linear Integrated Circuits and DMOS Devices (Application Notes only) SSD-202C
COS/MOS Digital Integrated Circuits SSD-203C
Power Transistors SSD-204C
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High-Reliability Devices SSD-207C

Announcement Newsletter: "What's New in Solid State" Availabe FREE to all DATABOOK users.

"Bingo-type Response-Card Service" included with Newsletter Available FREE to all DATABOOK users.

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NOTE: See pages 3 and 4 for additional information on this total data service. To qualify for Newsletter mailing, use the form on page 4 (unless you received your DATABOOK directly from RCA). You must qualify annually since a new mailing list is started for each edition of the DATABOOKS.

RCA LINEAR Integrated Circuits

This DATABOOK contains complete data on linear integrated circuits and DMOS (discrete MOS field-effect) devices presently available from RCA Solid State Division as standard products. Application notes on both linear IC's and DMOS devices are contained in a separate DATABOOK, SSD-202C.

For ease of type selection, product matrix charts are given on pages 10-18. Data sheets for linear IC's and DMOS devices are then included as nearly as possible in alphanumerical sequence of type numbers. Because some data sheets include more than one type number, however, some types may be out of sequence. If you don't find the type you're looking for where you expect it to be, please consult the Index to Devices on pages 6-7.

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RCA Limited | Sunbury-on-Thames | Middlesex TW16 7HW, England
RCA s.a. | 4400 Herstal | Liege, Belgium

RCA Solid State Total Data Service System

The RCA Solid State DATABOOKS are supplemented throughout the year by a comprehensive data service system that keeps you aware of all new device announcements and lets you obtain as much or as little product information as you need — when you need it.

New solid-state devices and related publications announced during the year are described in a newsletter entitled "What's New in Solid State". If you obtained your DATABOOK(s) directly from RCA, your name is already on the mailing list for this newsletter. If you obtained your book(s) from a source other than RCA and wish to receive the newsletter, please fill out the form on page 4, detach it, and mail it to RCA.

Each newsletter issue contains a "bingo"-type fast-response form for your use in requesting information on new devices of interest to you. If you wish to receive all new product information published throughout the year, without having to use the newsletter response form, you may subscribe to a mailing service which will bring you all new data sheets and application notes in a package every other month. You can also obtain a binder for easy filing of all your supplementary material. Provisions for obtaining information on the update mailing service and the binder are included in the order form on page 4.

Because we are interested in your reaction to this approach to data service, we invite you to add your comments to the form when you return it, or to send your remarks to one of the addresses listed at the top of the form. We solicit your constructive criticism to help us improve our service to you.

Order Form for "What's New in Solid State" and for further information on Update Mailings and Binders

Please fill out just one copy of this form, and mail it to:

(a) from U.S.A. and Canada:

RCA Solid State Division
Box 3200
Somerville, N. J., U.S.A. 08876

(b) from Latin America and Far East:

RCA Solid State
International Sales
Somerville, N. J., U.S.A. 08876

(c) from United Kingdom, Europe, Middle East, and Africa:

RCA Limited
Sunbury-on-Thames
Middlesex TW16 7HW, England

or

RCA s.a.
4400 Herstal
Liege, Belgium

☐ Please add my name to the mailing list for "What's New in Solid State"

☐ Please send me details on obtaining update mailings for my DATABOOKS and a binder for filing of supplementary material.

Name (Last) (Initials)

Company

Address (Number) (Street, RFD, P.O. Box)

Home ☐
Business ☐

(City) (State or Prov.)

(Country) (Zip or Pstl. Zone)

Function: (Check One)

A ☐ Executive/Administration
B ☐ Purchasing/Procurement
C ☐ Research/Development
D ☐ Design Engineer
E ☐ Application/Components Engineer
F ☐ Production/Manufacturing
G ☐ Documentation/Library
H ☐ Reliability/QA
I ☐ Education/Training
J ☐ Program/Project Management
K ☐ Marketing

Activity: (Check One)

A ☐ Broadcast
B ☐ Communication
C ☐ Instrumentation/Control
D ☐ Computer/Data Processing
E ☐ Computer, Peripheral
F ☐ Automotive
G ☐ Industrial
H ☐ Medical
I ☐ Research
J ☐ Transportation
K ☐ Consumer, Electronic
L ☐ Consumer, Appliance
M ☐ Space
N ☐ Ordnance
O ☐ Avionics
P ☐ Electronic Warfare

Product Interest: (Indicate order of interest if more than one is marked)

A ☐ Linear IC's
B ☐ Digital IC's, COS/MOS
C ☐ Digital IC's, Bipolar
D ☐ Thyristors/Rectifiers
E ☐ Liquid Crystals
F ☐ Semiconductor Diodes
G ☐ RF Power Semiconductors
H ☐ MOSFETS
I ☐ Power Transistors
J ☐ Power Hybrid Circuits

Table of Contents

Index to Linear Integrated Circuits

(Circuits marked with an asterisk are also available in chip form. A data sheet on Linear IC chips, File No. 516, is available on request.)

Index to Linear Integrated Circuits (cont'd)

Notes: For types available in beam-lead versions (File No. 515), refer to page 513.
For RCA linear IC packages, lead forms, and identifying suffix letters for package types, refer to page 19.

Index to DMOS Devices

Linear IC New Products Program

The linear integrated circuits listed below are some of the devices scheduled for introduction during 1975. For further information concerning announcement schedules and availability, contact your RCA representative or supplier or watch for announcement in the RCA Solid State Announcement Newsletter, "What's New In Solid State", referred to on the inside front cover of this DATABOOK.

Consumer Types

Description	Similar Industry Type
CD-4 Quadraphonic Demodulator and Noise-Suppression Circuit	
TV Horizontal Processor, Positive Sync	MC1391
TV Horizontal Processor, Negative Sync	MC1394
FM Detector and Limiter With Voltage Regulator	ULN2136
High-Gain Dual-Gate MOS/FET for TV Mixer Applications	3N211
Two-Terminal Temperature Sensor	
7-Watt Audio Amplifier with Load Dump Protection (Positive Voltage Transients)	

Industrial Types

Type No.	Description	Similar Industry Type	Availability
CA7800	Voltage Regulator Series	μA7800	1 Q '75
CA1488	Quad Line Driver	MC1488	2 Q '75
CA1489, 89A	Quad Line Receivers	MC1489A	2 Q '75
CA75361A	Memory Driver	SN75361A	2 Q '75
CA521	Memory Sense Amplifier	NE521	2 Q '75

Linear IC New Products Program (cont'd)

Consumer Types and Industrial Types Custom Programs

RCA has considerable experience in the design and production of custom circuits for high-volume equipment in the applications listed below. Our engineering staff is available for the design of circuits through either specialized chip designs or the remetallization of one of our existing standard circuits.

Applications:

- Automotive
- Home Entertainment
- Appliances
- Computer Interface
- Telecommunications
- Controls

Linear IC's Direct-Replacement Guide

Analog Devices Type No.	RCA Direct Replacement
AD101AH	CA101AT
AD201H	CA201T
AD301AH	CA301AT
AD741	CA741T
AD741C	CA741CT

Advanced Micro Devices Type No.	RCA Direct Replacement
AM101T	CA101T
AM101AT	CA101AT
AM201T	CA201T
AM301AT	CA301AT
AM307T	CA307T
AM741T	CA741T
AM741CT	CA741CT
AM747T	CA747T
AM747CT	CA747CT
AM748T	CA748T
AM748CT	CA748CT

Fairchild Semiconductor Type No.	RCA Direct Replacement
LM101AH	CA101AT
LM101H	CA101T
LM107H	CA107T
LM108AH	CA108AT
LM108H	CA108T
LM111H	CA111T
LM201AH	CA201AT
LM201H	CA201T
LM207H	CA207T
LM208AH	CA208AT
LM208H	CA208T
LM301AH	CA301AT
LM301AN	CA301AE
LM307H	CA307T
LM307N	CA307E
LM308AH	CA308AT
LM308H	CA308T
LM311H	CA311T
μA723HC	CA723CT
μA723HM	CA723T
741DC	CA741CE
741DM	CA741E
741HM	CA741T
741HC	CA741CT
741TC	CA741E
747DC	CA747CE
747DM	CA747E
747HC	CA747CT
747HM	CA747T

Fairchild Semiconductor Type No.	RCA Direct Replacement
748HC	CA748CT
748HM	CA748T
748TC	CA748CE
μA758	CA758E
FPQ3724P	CA3724G
FPQ3725P	CA3725G
U5B7748312	CA748T
U5B7748393	CA748CT
U5R7723312	CA723T
U5R7723393	CA723CT
U6A7723393	CA723CE

Intersil Type No.	RCA Direct Replacement
ICL-101-TY	CA101T
ICL-101A-TY	CA101AT
ICL-108-TY	CA108T
ICL-108A-TY	CA108AT
ICL-201-TY	CA201T
ICL-201A-TY	CA201AT
ICL-208-TY	CA208T
ICL-208A-TY	CA208AT
ICL-301A-PA	CA301AE
ICL-301A-TY	CA301AT
ICL-308-TY	CA308T
ICL-308A-TY	CA308AT
ICL-723-TZ	CA723T
ICL-723C-TZ	CA723CT
ICL-741-TY	CA741T
ICL-741C-TY	CA741CT
ICL-741-LNC	CA741CE
ICL-748-TY	CA748T
ICL-748C-TY	CA748CT
ICL-8741-PA	CA741E
ICL-8741C-PA	CA741CE
ICL-8748-PA	CA748E
ICL-8748C-PA	CA748CE

Motorola Semiconductor Type No.	RCA Direct Replacement
MLM101AG	CA101AT
MLM107G	CA107T
MLM111G	CA111T
MLM201AG	CA201AT
MLM207G	CA207T
MLM211G	CA211T
MC1310P	CA1310E
MC1311P	CA758E
MC1352P	CA1352E
MC1357P	CA2111AE
MC1398P	CA1398E
MC1441L	CA1541D

Motorola Semiconductor Type No.	RCA Direct Replacement
MC1458G	CA1458T
MC1458CP1	CA1458E
MC1541L	CA1541D
MC1558G	CA1558T
MC1723CG	CA723CT
MC1723CH	CA723CH
MC1723G	CA723T
MC1741G	CA741T
MC1741CG	CA741CT
MC1741CP1	CA741CE
MC1741P2*	CA741E
MC1741CP2*	CA741CE
MC1748G	CA748T
MC1748CG	CA748CT
MC3302P	CA339AE
MC3401P	CA3401E
MPQ3724P	CA3724G
MPQ3725P	CA3725G

National Semiconductor Type No.	RCA Direct Replacement
LM101AH	CA101AT
LM101H	CA101T
LM107H	CA107T
LM108AH	CA108AT
LM108H	CA108T
LM111H	CA111T
LM201AH	CA201AT
LM201H	CA201T
LM207H	CA207T
LM208AH	CA208AT
LM208H	CA208T
LM211H	CA211T
LM301AH	CA301AT
LM301AN	CA301AE
LM307H	CA307T
LM307N	CA307E
LM308AH	CA308AT
LM308H	CA308T
LM311H	CA311T
LM324N	CA324E
LM339AN	CA339AE
LM339D	CA339E
LM723CH	CA723CT
LM723H	CA723T
LM741H	CA741T
LM741CH	CA741CT
LM741CN	CA741CE
LM747H	CA747T
LM747CH	CA747CT
LM747CN	CA747CE
LM748H	CA748T
LM748CH	CA748CT

Linear IC's Direct-Replacement Guide (cont'd)

National Semiconductor Type No.	RCA Direct Replacement
LM748CN	CA748CE
LM1310N	CA1310E
LM1458H	CA1458T
LM1458N	CA1458E
LM1558H	CA1558T
LM1800N	CA758E
LM2111	CA2111AE
DH3724CN	CA3724G
DH3725CN	CA3725G

Precision Monolithic Type No.	RCA Direct Replacement
SSS108J	CA108T
SSS108AJ	CA108AT
SSS208J	CA208T
SSS208AJ	CA208AT
SSS308J	CA308T
SSS308AJ	CA308AT

Raytheon Type No.	RCA Direct Replacement
LM101AH	CA101AT
LM101H	CA101T
LM107H	CA107T
LM108AH	CA108AT
LM108H	CA018T
LM111H	CA111T
LM201AH	CA201AT
LM201H	CA201T
LM207H	CA207T
LM211H	CA211T
LM301AH	CA301AT
LM301AN	CA301AE
LM307H	CA307T
LM307N	CA307E
LM308AH	CA308AT
LM308H	CA308T
LM311H	CA311T
RC723T	CA723CT
RM723T	CA723T
RC741DN	CA741CE
RC741TE	CA741CT
RM741TE	CA741T
RC748DN	CA748CE
RC748TE	CA748CT
RM748TE	CA748T
RC1458DN	CA1458E
RC1458T	CA1458T
SP3724QD	CA3724G
SP3725QD	CA3725G
RM4558TE	CA1558T

Signetics Type No.	RCA Direct Replacement
LM101AH	CA101AT
LM101H	CA101T
LM107H	CA107T
LM201AH	CA201AT
LM201H	CA201T
LM301AH	CA301AT
LM301AN	CA301AE
LM307H	CA307T
LM307N	CA307E
μA723CL	CA723CT
μA723L	CA723T
N5558T	CA1458T
N5558V	CA1458E
N5741T	CA741CT
N5741V	CA741CE
N5747A	CA747CE

Signetics Type No.	RCA Direct Replacement
N5748T	CA748CT
N5748V	CA748CE
S5558T	CA1558T
S5741T	CA741T
S5748T	CA748T

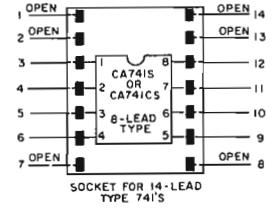
Silicon General Type No.	RCA Direct Replacement
SG101AT	CA101AT
SG101M	CA101S
SG101T	CA101T
SG107T	CA107T
SG108AT	CA108AT
SG108T	CA108T
SG111T	CA111T
SG201AT	CA201AT
SG201T	CA201T
SG207T	CA207T
SG208AT	CA208AT
SG208T	CA208T
SG211T	CA211T
SG301AM	CA301AE
SG301AT	CA301AT
SG307M	CA307E
SG307T	CA307T
SG308AT	CA308AT
SG308T	CA308T
SG311T	CA311T
SG339N	CA339E
SG339AN	CA339AE
SG723CT	CA723CT
SG723T	CA723T
SG741M	CA741E
SG741T	CA741T
SG741CM	CA741CE
SG741CT	CA741CT
SG747T	CA747T
SG747CT	CA747CT
SG748M	CA748E
SG748T	CA748T
SG748CM	CA748CE
SG748CT	CA748CT
SG1458M	CA1458E

Solitron Type No.	RCA Direct Replacement
UC4741	CA741T
UC7471C	CA741CT

Sprague Type No.	RCA Direct Replacement
ULN2111A	CA2111AE
ULN2125A	CA3120E
ULN2269A	CA3121E
ULN2741D	CA741T
ULN2747A	CA747CE
ULS2741D	CA741CT
ULX2210	CA1310E
ULX2244	CA758E

Texas Instruments Type No.	RCA Direct Replacement
SN52101AL	CA101AT
SN52101L	CA101T
SN52107L	CA107T
SN52108L	CA108T
SN52108AL	CA108AT
SN52558L	CA1558T
SN52558P	CA1558S
SN52741L	CA741T
SN52741P	CA741S
SN52747L	CA747T
SN52748L	CA748T
SN52748P	CA748S
SN72301AL	CA301AT
SN72301AN	CA301AE
SN72307L	CA307T
SN72307P	CA307E
SN72308L	CA308T
SN72308AL	CA308AT
SN72558L	CA1458T
SN72558P	CA1458E
SN72741L	CA741CT
SN72741P	CA741CE
SN72747	CA747CT
SN72748L	CA748CT
SN72748P	CA748CE
SN72301AL	CA301AT
SN72301AP	CA301AE
SN72307P	CA307E
SN72558P	CA1458E
SN76115N	CA1310E
SN76116N	CA758E
SN76650N	CA1352E

• Can be substituted for the corresponding 14-lead dual-in-line type by inserting device into 14-pin socket such that terminal No. 1 of the CA741 coincides with socket terminal No. 3 of the type to be replaced.



Note: RCA types in TO-5 packages are also supplied with dual-in-line formed leads ("DIL-CAN" package) and are designated with suffix letter (S). These types are both pin and electrical direct replacements for the corresponding 8-lead "Mini-Dip" dual-in-line types.

For prices and availability of RCA Linear Integrated Circuits, contact your RCA Distributor or your local RCA Sales Office.

Operational Amplifiers

		Micropower						High-Current							General Purpose																
															Single Unit															
															Low Noise															COS/MOS Output, MOS/FET Input
		Single OTA ●		Triple OTA ●			Single OP-AMP																							
		CA3080	CA3080A	CA3060A	CA3060B	CA3060	CA3078A	CA3078	CA3033	CA3033A	CA3047	CA3047A	CA3094	CA3094A	CA3094B	CA6741	CA6078A ▲	CA101	CA101A	CA201	CA201A	CA301A	CA107	CA207	CA307	CA741C	CA741	CA748C	CA748	CA3130	CA3130A	CA3130B
	File No.	475		537			535		360				598			592		786					785			531				817		
APPLICATIONS	Sample and Hold																													■	■	■
	Switching	■	■	■	■	■							■	■	■																	
	Schmitt Trigger	■	■	■	■	■			■	■	■	■	■	■	■															■	■	■
	Multivibrator	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	Modulator	■	■	■	■	■	■	■					■	■	■		■															
	Mixer	■	■	■	■	■	■	■					■	■	■		■															
	Detector	■	■	■	■	■	■	■					■	■	■		■															
	Comparator	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			■	■	■	■	■	■	■
	DC Amplifier	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■									■	■	■	■	■	■	■
	Timer												■	■	■			■	■	■	■	■	■	■	■					■	■	■
	Wideband Large Signal																															
FEATURES	Multiple Unit			■	■	■																										
	AGC Capability	■	■	■	■	■							■	■	■																	
	Balanced Input	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	Short-Circuit Protection	■	■	■	■	■	■	■								■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	Internal Frequency Compensation															■							■	■	■	■	■					
	Offset Adjustment						■	■	■	■	■	■					■	■	■	■	■	■						■	■	■	■	■
	Negative V_{ICR} near V^-	■	■	■	■	■	■	■					■	■	■		■													■	■	■
	Low Power Supply Current (= .1 mA)	■	■	■	■	■	■	■					■	■	■		■															
	Ultra-Low I_{IB}	■	■	■	■	■	■	■					■	■	■		■													■	■	■
	Very Low V_{IO} & I_{IO}																															
PACKAGE		TYPE DESIGNATION SUFFIX LETTER (See Note 1)																														
	Flat Pack Ceramic																															
	Dual In-Line Ceramic (DIC)			D	D	D			■	■																						
	Dual In-Line Plastic (DIP)	E*				E					■	■	E*	E*									E*		E*	E*		E*				
	TO-5 Style Straight Lead	■	■				T	T					T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
	TO-5 Style Dual-In-Line (DIL-CAN)	S	S				S	S					S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
	Frit Seal Dual In-Line Ceramic	F	F				F	F																								
	Beam Lead																										L					
	Chip							H																		H		H				

Note 1: The indicated suffix letter identifies the package type for the device type number having a suffix letter, a black square is shown for a type number with no suffix letter.

● Operational Transconductance Amplifier ▲ Micropower Type *Available in 8-lead DIP (MINI-DIP)

Operational Amplifiers

		General Purpose					Wideband																Precision					
		Multiple Unit				Quad.																						
		CA747C	CA747	CA1458	CA1558	CA3401	CA3008	CA3008A	CA3010	CA3010A	CA3015	CA3015A	CA3016	CA3016A	CA3029	CA3029A	CA3030	CA3030A	CA3037	CA3037A	CA3038	CA3038A	CA3100	CA108	CA108A	CA208	CA208A	CA308	CA308A
	File No.	531				630	316	310	316	310	316	310	316	310	316	310	316	310	316	310	316	310	625	621					
APPLICATIONS	Switching																												
	Schmitt Trigger																												
	Multivibrator	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■		■	■	■	■	■	■
	Modulator																												
	Mixer																												
	Detector																												
	Comparator	■	■	■	■																		■	■	■	■	■	■	■
	DC Amplifier	■	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■		■	■	■	■	■	■
	Timer																							■	■	■	■	■	■
	Wideband Large Signal																						■						
FEATURES	Multiple Unit	■	■	■	■	■																							
	AGC Capability																												
	Balanced Input	■	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■		■	■	■	■	■	■
	Short-Circuit Protection	■	■	■	■																			■	■	■	■	■	■
	Internal Frequency Compensation	■	■	■	■																			■	■	■	■	■	■
	Offset Adjustment	■	■				■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■							
	Negative V_{ICR} near V^-					■																							
	Low Power Supply Current (< 1 mA)																							■	■	■	■	■	■
	Ultra-Low I_{IB}																							■	■	■	■	■	■
	Very Low V_{IO} & I_{IO}																								■		■		■
PACKAGE	TYPE DESIGNATION SUFFIX LETTER (See Note 1)																												
	Flat Pack Ceramic						■	■					■	■															
	Dual In-Line Ceramic (DIC)																		■	■	■	■							
	Dual In-Line Plastic (DIP)	E		E*		E									■	■	■	■											
	TO-5 Style Straight Lead	T	T	T	T				■	■	■	■											T	T	T	T	T	T	T
	TO-5 Style Dual In-Line (DIL-CAN)			S	S																		S	S	S	S	S	S	S
	Frit Seal Dual In-Line Ceramic																						F						
	Beam Lead																												
	Chip	H				H																	H				H		

Note 1 The indicated suffix letter identifies the package type for the device type number having a suffix letter. a black square is shown for a type number with no suffix letter.

*Available in 8-lead DIP (MINI-DIP)

Arrays

		Diode Arrays		Transistor Arrays																	
		Individual	Quad Plus Two	General-Purpose								2 Transistors, 2 Zener Diodes, 1 Diode	Dual Darlington Connected			Darlington Connected Pair Plus Two Individual			
				n-p-n					p-n-p		p-n-p & n-p-n										
		CA3019	CA3039	CA3081	CA3082	CA3083	CA3183A	CA3183	CA3084		CA3096	CA3096A	CA3093	CA3036	CA3050	CA3051	CA3018	CA3018A	CA3118A	CA3118	
	File No.	236	343	480		481		532	482		595		533	275		361	338		532		
Applications	Comparator					■	■	■					■								
	Detector	■	■			■	■	■			■	■			■	■	■	■	■	■	
	Differential Amplifier					■	■	■	■		■	■	■	■	■	■	■	■	■	■	
	Limiter	■	■			■	■	■	■								■	■	■	■	
	Mixer	■	■			■	■	■	■								■	■	■	■	
	Modulator	■	■			■	■	■	■								■	■	■	■	
	Multivibrator	■	■			■	■	■	■								■	■	■	■	
	Oscillator			■	■	■	■	■	■								■	■	■	■	
	Schmitt Trigger					■	■	■													
	Sense Amplifier					■	■	■			■	■									
	Switching	■	■	■	■	■	■	■	■												
	Thyristor & SCR Control			■	■	■	■	■			■	■	■				■	■	■	■	
	Timer																				
	VHF																				
	Regulator												■								
Features	High Input Resistance																				
	Balanced Input					■	■	■	■		■	■		■	■	■	■	■	■	■	
	Balanced Output					■	■	■	■					■	■	■	■	■	■	■	
	Low Noise										■	■		■							
	AGC Capability																■	■	■	■	
	Multiple Unit													■	■	■	■	■	■	■	
	Wide Band																■	■	■	■	
		TYPE DESIGNATION SUFFIX LETTER (SEE NOTE 1)																			
Package	Flat Pack Ceramic																				
	Dual In-Line Ceramic														■						
	Dual In-Line Plastic			■	■	■	E	E	■		E	E	E			■					
	TO-5 Style Straight Lead	■	■														■	■	T	T	
	TO-5 Style Formed Lead																				
	Frit Seal Dual-In-Line Ceramic			F	F	F															
	Chip	H	H	H	H	H		H	H		H		H				H			H	
	Beam-Lead					L			L								L				

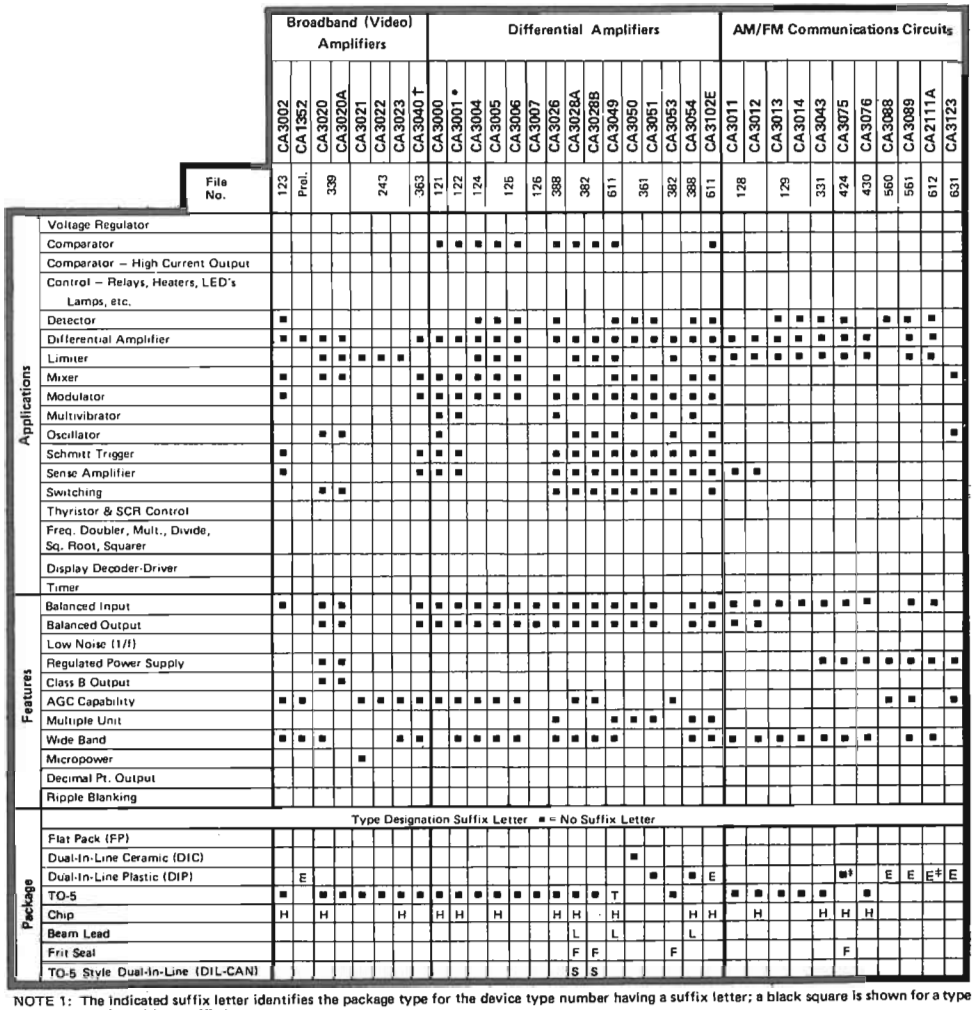
NOTE 1: The indicated suffix letter identifies the package type for the device type number having a suffix letter; a black square is shown for a type number with no suffix letter.

Arrays

		Transistor Arrays									Amplifier Arrays					
		Differentially Connected Pair Plus Three Individual					Super β Diff. Amp. Plus 3 n-p-n Trans.	1 n-p-n & 1 p-n-p/n-p-n transistors, 1 zener diode, 1 PUT* 1 SCR▲ (Thyristor)	COS/MOS Array 3 n-channel & 3 p-channel transistors	High-Freq. n-p-n	Dual Independent (Differential)				Three Ampl.	Four Ampl.
		CA3045	CA3046	CA3086	CA3146A	CA3146	CA3095	CA3097	CA3600	CA3127	CA3026	CA3049	CA3102	CA3054	CA3035	CA3048
	File No.	341		483	532		591	633	619	662	388	611		388	274	377
Applications	Comparator							■	■							
	Detector	■	■	■	■	■	■			■	■	■	■			
	Differential Amplifier	■	■	■			■		■	■	■	■	■			
	Limiter			■					■							
	Mixer			■			■		■	■		■	■			■
	Modulator			■						■		■	■			
	Multivibrator			■			■		■	■		■	■			■
	Oscillator			■			■	■	■	■		■	■			
	Schmitt Trigger			■						■						
	Sense Amplifier			■						■		■	■			
	Switching			■				■	■	■		■	■			
	Thyristor & SCR Control			■				■	■							
	Timer							■	■							
	VHF							■		■						
	Regulator							■								
Features	High Input Resistance								■							
	Balanced Input	■	■	■	■	■	■			■		■	■			
	Balanced Output	■	■	■	■	■	■			■		■	■			
	Low Noise						■		■						■	■
	AGC Capability						■			■		■	■			
	Multiple Unit	■	■	■	■	■	■		■	■		■	■	■	■	■
	Wide Band	■	■	■	■	■	■			■		■	■		■	
Package	TYPE DESIGNATION SUFFIX LETTER (SEE NOTE 1)															
	Flat Pack Ceramic															
	Dual In-Line Ceramic	■	■	■												
	Dual In-Line Plastic				E	E	E	E	E	E			E	■		■
	TO-5 Style Straight Lead										■	■			■	
	TO-5 Style Formed Lead														VI	
	Frit Seal Dual-In-Line Ceramic	F														
	Chip	H				H	H	H			H	H	H	H	H	H
	Beam-Lead	L										L		L		

* Programmable Unijunction Transistor ▲ Silicon Controlled Rectifier

Broadband (Video) and Differential Amplifiers, and AM/FM Communications Circuits



NOTE 1: The indicated suffix letter identifies the package type for the device type number having a suffix letter; a black square is shown for a type number with no suffix letter.

• CA3001 is also useful as a Broadband (Video) Amplifier.

† CA3040 is also useful as a Differential Amplifier.

‡ In quad-in-line package (QUIP)

Power-Control and Voltage-Regulator Circuits, Analog Multiplier, and Computer-Interface Circuits

		Power Control										Voltage Regulators			Analog Multiplier	Computer Interface Circuits				
		Thyristor Control			Power Control Switch/ Ampl.			Programmable Comparator	Timers	Photo Det.					Sense Ampl.	Decoder Drivers			
		CA3058	CA3059	CA3079	CA3097	CA3094A	CA3094B	CA3094	CA3099	CA555, C	CA3062	CA3085	CA3085A	CA3085B	CA3091	CA1541	CD2500E	CD2501E	CD2502E	CD2503E
	File No.	490			633	598			620	834	421	491			534	536	392			
Applications	Voltage Regulator					■	■	■				■	■	■		Sense Amplifier				
	Comparator	■	■	■	■	■	■	■	■											
	Comparator – High Current Output	■	■	■		■	■	■	■			■	■	■						
	Control – Relays, Heaters, LED's, Lamps, Etc.	■	■	■	■	■	■	■	■											
	Detector	■	■	■							■				■					
	Differential Amplifier	■	■	■		■	■	■	■											
	Limiter																			
	Mixer					■	■	■							■					
	Modulator					■	■	■	■	■					■					
	Multivibrator				■	■	■	■	■		■									
	Oscillator	■	■	■	■	■	■	■	■	■										
	Schmitt Trigger				■	■	■	■	■											
	Sense Amplifier																			
	Switching	■	■	■		■	■	■	■			■								
	Thyristor & SCR Control	■	■	■	■	■	■	■	■			■	■	■						
	Freq. Doubler, Mult., Divide, Sq. Root, Squarer														■					
	Display Decoder-Driver																■	■	■	■
	Timer	■	■	■	■	■	■	■	■	■										
Features	Balanced Input					■	■	■	■		■									
	Balanced Output																			
	Low Noise (1/f)					■	■	■				■	■	■						
	Regulated Power Supply	■	■	■					■											
	Class B Output																			
	AGC Capability					■	■	■												
	Multiple Unit																			
	Wide Band																			
	Micropower					■	■	■	■											
	Decimal Pt. Output																■		■	
	Ripple Blanking																	■		■
Package		Type Designation Suffix Letter ■ = No Suffix Letter																		
	Flat Pack (FP)																			
	Dual-In-Line Ceramic (DIC)	■													D	D				
	Dual-In-Line Plastic (DIP)		■	■	E			E	E		E		E				E	E	E	E
	TO-5					T	T	T			T	■	■	■						
	Chip		H		H			H	H				H		H	H				
	Beam Lead												L							
	Frit Seal																			
	TO-5 Style Dual-In-Line (DIL-CAN)					S	S	S			S		S	S	S					

NOTE 1: The indicated suffix letter identifies the package type for the device type number having a suffix letter; a black square is shown for a type number with no suffix letter.

CA555, CA555C, CA3085, CA3085A available in 8-lead DIP (MINI-DIP) package.

Consumer Circuits

		Audio Circuits						Multiplex Decoders			AM Rcvr. Ckts.		FM Receiver Circuits								
		Pre-Amp.		Drivers		Power Amplifiers							FM IF Subsystems						FM IF Gain Blocks		
		CA3036	CA3052	CA3094	CA3094A, B	CA810	CA3131, CA3132	CA758	CA1310	CA3090A	CA3088	CA3123	CA2111A	CA3089	CA3075	CA3043	CA3013, CA3014	CA3011	CA3012	CA3076
	File No.	387		598		Prel.	Prel.	760	761	684	560	631	612	561	424	331	129	128		430
Circuit Functions	Audio Driver			■	■			Stereo Multiplex Decoder												
	Audio Preamplifier	■	■	■	■						■			■	■	■	■			
	ACC																			
	AFC/AFT													■						
	AFPC																			
	AGC			■	■						■			■						
	Chroma Amplifier																			
	Chroma Demodulator																			
	Chroma Signal Processor																			
	Converter										■	■								
	Detector										■		■	■	■	■	■			
	Video Amplifier																	■	■	■
	Sync Processor																			
	IF Amplifier										■	■	■	■	■	■	■	■	■	■
	Limiter												■	■	■	■	■	■	■	■
	Oscillator											■								
	Audio Power Amplifier					■	■													
	Tint Control																			
Package		(TYPE DESIGNATION SUFFIX LETTER (See Note 1)																		
	Dual-In-Line Plastic		■				EM	E	E		E	E	E	E						
	Quad-In-Line Plastic					Q,QM				Q			Q		■					
	TO-5 Standard Lead	■		T	T											■	■	■	■	■
	TO-5 Formed Lead																			

Note 1: Where a code letter is shown (E, EM, Q, T, V1), add the code letter as a suffix to the type number to identify the package (and lead configuration) option. A black square indicates no suffix code is added to the type number for that package option.

Consumer Circuits

TV Receiver Circuits

Circuit Functions	Remote Control	Automatic Fine-Tuning (AFT)		IF Systems: Sound					IF Systems: Pix		Chroma Systems: 2 Package								Chroma Systems: 3 Package			"Jungle" Circuit
	CA3035	CA3044	CA3064	CA3134	CA3041	CA3042	CA3065	CA2111A	CA3068	CA1352	CA3066	CA3067	CA3070	CA3121	CA3067	CA3126	CA1398	CA3125	CA3128	CA3070	CA3071	CA3072	CA3120
File No.	274	340	396	Prel.	318	319	412	612	467	Prel.	466		468	688	466	860	686	685	Prel.	468			691
Audio Driver					■	■	■																
Audio Preamplifier	■				■	■	■	■															
ACC											■		■	■		■	■		■	■	■		
AFC/AFT		■	■																				
AFPC													■			■			■	■			
AGC									■	■													■
Chroma Amplifier											■			■		■	■		■		■		
Chroma Demodulator												■		■	■			■				■	
Chroma Processor; PAL Systems											■		■	■		■	■		■	■	■		
Converter																							
Detector		■	■	■	■	■	■	■	■				■							■			
Video Amplifier									■									■			■		■
Sync Processor																							■
IF Amplifier		■	■	■	■	■	■	■	■	■													
Limiter		■		■	■	■	■	■															
Oscillator											■		■		■	■	■		■	■			
Audio Power Amplifier				■																			
Tint Control												■	■				■			■			
Package: (TYPE DESIGNATION SUFFIX LETTER (See Note 1))																							
Dual-In-Line Plastic			E	E				E		E			■	E			E	E		■	■	■	E
Quad-In-Line Plastic					■	■	■	Q	■		■	■			■	Q			Q				
TO-5 Standard Lead	■	■																					
TO-5 Formed Lead	V1	V1	■																				

Note 1 Where a code letter is shown (E, EM, Q, T, V1), add the code letter as a suffix to the type number to identify the package (and lead configuration) option. A black square indicates no suffix code is added to the type number for that package option.

DMOS (Discrete MOS Field-Effect) Devices

		Industrial Types													Consumer Types											
		Single-Gate							Dual-Gate			Dual-Gate Protected			Single-Gate			Dual-Gate				Dual-Gate Protected					
		3N128	3N138	3N139	3N142	3N143	3N152	3N153	3N154	3N140	3N141	3N159	3N187	3N200	40819	40467A	40468A	40559A	40600	40601	40602	40603	40604	40673	40820	40821	40822	40823	40841
	File No.	309	283	284	286	309	314	320	335	285	285	326	436	437	463	324	323	323	333	333	333	334	334	381	464	464	465	465	489
Applications	RF Amplifier, Mixer	■			■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	Chopper		■					■																					■
	General-Purpose Amplifier			■	■															■									■
	Oscillator	■		■	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Features	Low-Noise						■					■	■	■															
	Low-Leakage		■					■		■	■	■							■	■	■	■	■						
	High-Gain						■			■		■	■	■															
	Gain-Controlled									■	■	■	■	■	■				■	■	■	■	■	■	■	■	■	■	■
	Premium-Performance						■					■	■	■															

All MOS/FET devices are supplied in the JEDEC TO-72 package

RCA LINEAR IC PACKAGES AND LEAD FORMS

D-Suffix: Dual-In-Line Welded-Seal Ceramic Package (DIC)

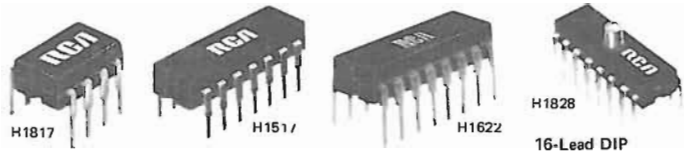
14-Lead DIC

16-Lead DIC

F-Suffix: Dual-In-Line Frit-Seal Ceramic Package

8-Lead Frit Seal | 14-Lead Frit Seal | 16-Lead Frit Seal

E-Suffix: Dual-In-Line Plastic Package (DIP)



8-Lead MINI-DIP | 14-Lead DIP | 16-Lead DIP | 16-Lead DIP with "Power Stud"

EM-Suffix: Modified Dual-In-Line Plastic Package with Heat Sink

16-Lead DIP

Q-Suffix: Quad-In-Line Plastic Package (QUIP)

Integral Bent-Down Wing-Tab Heat Sink

14-Lead QUIP | 16-Lead QUIP | 20-Lead QUIP | 16-Lead Modified QUIP

QM-Suffix: Modified Quad-In-Line Plastic Package (QUIP) with Integral Flat and Pierced Wing-Tab Heat Sink

16-Lead QUIP

T-Suffix: TO-5 Style Package with Straight Leads

8-Lead TO-5 | 10-Lead TO-5 | 12-Lead TO-5

S-Suffix: TO-5 Style Package with Dual-In-Line Formed Leads (DIL-CAN)

8-Lead TO-5 DIL-CAN

V1-Suffix: TO-5 Style Package with Radial Formed Leads

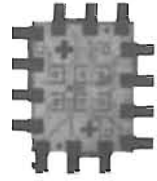
10-Formed-Lead TO-5

K-Suffix: Ceramic Flat Package (FP)

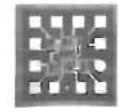
14-Lead FP

JEDEC TO-72: MOS/FET Devices

L-Suffix: IC Beam Lead



H-Suffix: IC Chip



RCA
Solid State
Division

Operating Considerations for RCA Solid State Devices

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces. For specific information on voltage creepage, the user should consult references such as the JEDEC Standard No. 7 "Suggested Standard on Thyristors," and JEDEC Standard RS282 "Standards for Silicon Rectifier Diodes and Stacks".

The metal shells of some solid state devices operate at the collector voltage and for some rectifiers and thyristors at the anode voltage. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

TRANSISTORS AND THYRISTORS WITH FLEXIBLE LEADS

Flexible leads are usually soldered to the circuit elements. It is desirable in all soldering operatings to provide some slack or an expansion elbow in each lead to prevent excessive tension on the leads. It is important during the soldering operation to avoid excessive heat in order to prevent possible damage to the devices. Some of the heat can be absorbed if the flexible lead of the device is grasped between the case and the soldering point with a pair of pliers.

TRANSISTORS AND THYRISTORS WITH MOUNTING FLANGES

The mounting flanges of JEDEC-type packages such as the TO-3 or TO-66 often serve as the collector or anode terminal. In such cases, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. Under no circumstances, however, should the mounting flange of a transistor be soldered directly to the heat sink or chassis because the heat of the soldering operation could permanently damage the device. Soldering is the preferred method for mounting thyristors; see "Rectifiers and Thyristors," below. Devices which cannot be soldered can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may be soldered to the pins close to the pin seals provided care is taken to conduct excessive heat away from the seals; otherwise the heat of the soldering operation could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must have sufficient thermal capacity to assure that the heat dissipated in the heat sink itself does not raise the device mounting-flange temperature above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

In many applications the chassis is connected to the voltage-supply terminal. If the recommended mounting hardware shown in the data bulletin for the specific solid-state device is not available, it is necessary to use either an anodized aluminum insulator having high thermal conductivity or a mica insulator between the mounting-flange and the chassis. If an insulating aluminum washer is required, it should be drilled or punched to provide the two mounting holes for the terminal pins. The burrs should then be removed from the washer and the washer anodized. To insure that the anodized insulating layer is not destroyed during mounting, it is necessary to remove the burrs from the holes in the chassis.

It is also important that an insulating bushing, such as glass-filled nylon, be used between each mounting bolt and the chassis to prevent a short circuit. However, the insulating bushing should not exhibit shrinkage or softening under the operating temperatures encountered. Otherwise the thermal resistance at the interface between device and heat sink may increase as a result of decreasing pressure.

PLASTIC POWER TRANSISTORS AND THYRISTORS

RCA power transistors and thyristors (SCR's and triacs) in molded-silicone-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. The following paragraphs provide guidelines for handling and mounting of these plastic-package devices, recommend forming of leads to meet specific mounting requirements, and describe various mounting arrangements, thermal considerations, and cleaning methods. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor.

Lead-Forming Techniques

The leads of the RCA VERSAWATT in-line plastic packages can be formed to a custom shape, provided they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. The use of a properly designed fixture for this operation eliminates the need for repeated lead bending. When the use of a special bending fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least 1/8 inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT in-line package are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed. The maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance not less than 1/8 inch from the plastic case. When

wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of RCA molded-plastic high-power packages are not designed to be reshaped. However, simple bending of the leads is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends; repeated bendings should be avoided.

Mounting

Recommended mounting arrangements and suggested hardward for the VERSAWATT package are given in the data bulletins for specific devices and in RCA Application Note AN-4142. When the package is fastened to a heat sink, a rectangular washer (RCA Part No. NR231A) is recommended to minimize distortion of the mounting flange. Excessive distortion of the flange could cause damage to the package. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch.

Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphtalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided.

Modification of the flange can also result in flange distortion and should not be attempted. The package should not be soldered to the heat sink by use of lead-tin solder because the heat required with this type of solder will cause the junction temperature of the device to become excessively high.

The TO-220AA plastic package can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp. Socket No. PTS-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. DC74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.
2. Always fasten the package to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

The maximum allowable power dissipation in a solid state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating. However, when the device is mounted on a heat sink, care must be taken to assure that all portions of the thermal circuit are considered.

To assure efficient heat transfer from case to heat sink when mounting RCA molded-plastic solid state power devices, the following special precautions should be observed:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used on both sides of the insulating washer if one is employed.
6. Thin insulating washers should be used. (Thickness of factory-supplied mica washers range from 2 to 4 mils).
7. A lock washer or torque washer, made of material having sufficient creep strength, should be used to prevent degradation of heat sink efficiency during life.

A wide variety of solvents is available for degreasing and flux removal. The usual practice is to submerge components in a solvent bath for a specified time. However, from a reliability stand point it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), do not adversely affect the life of the component. This consideration applies to all non-hermetic and molded-plastic components.

It is, of course, impractical to evaluate the effect on long-term device life of all cleaning solvents, which are marketed with numerous additives under a variety of brand names. These solvents can, however, be classified with

respect to their component parts as either acceptable or unacceptable. Chlorinated solvents tend to dissolve the outer package and, therefore, make operation in a humid atmosphere unreliable. Gasoline and other hydrocarbons cause the inner encapsulant to swell and damage the transistor. Alcohol is an acceptable solvent. Examples of specific, acceptable alchols are isopropanol, methanol, and special denatured alcohols, such as SDA1, SDA30, SDA34, and SDA44.

Care must also be used in the selection of fluxes for lead soldering. Rosin or activated rosin fluxes are recommended, while organic or acid fluxes are not. Examples of acceptable fluxes are:

1. Alpha Reliaros No. 320-33
2. Alpha Reliaros No. 346
3. Alpha Reliaros No. 711
4. Alpha Reliafoam No. 807
5. Alpha Reliafoam No. 809
6. Alpha Reliafoam No. 811-13
7. Alpha Reliafoam No. 815-35
8. Kester No. 44

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and a physical standpoint.

RECTIFIERS AND THYRISTORS

A surge-limiting impedance should always be used in series with silicon rectifiers and thyristors. The impedance value must be sufficient to limit the surge current to the value specified under the maximum ratings. This impedance may be provided by the power transformer winding, or by an external resistor or choke.

A very efficient method for mounting thyristors utilizing the "modified TO-5" package is to provide intimate contact between the heat sink and at least one half of the base of the device opposite the leads. This package can be mounted to the heat sink mechanically with glue or an expoxy adhesive, or by soldering, the most efficient method.

The use of a "self-jigging" arrangement and a solder preform is recommended. If each unit is soldered individually, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. For more detailed thyristor mounting considerations, refer to Application Note AN3822, "Thermal Considerations in Mounting of RCA Thyristors".

MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

RF POWER TRANSISTORS

Mounting and Handling

Stripline rf devices should be mounted so that the leads are not bent or pulled away from the stud (heat sink) side of the device. When leads are formed, they should be supported to avoid transmitting the bending or cutting stress to the ceramic portion of the device. Excessive stresses may destroy the hermeticity of the package without displaying visible damage.

Devices employing silver leads are susceptible to tarnishing; these parts should not be removed from the original tarnish-preventive containers and wrappings until ready for use. Lead solderability is retarded by the presence of silver tarnish; the tarnish can be removed with a silver cleaning solution, such as thiourea.

The ceramic bodies of many rf devices contain beryllium oxide as a major ingredient. These portions of the transistors should not be crushed, ground, or abraded in any way because the dust created could be hazardous if inhaled.

Operating

Forward-Biased Operation. For Class A or AB operation, the allowable quiescent bias point is determined by reference to the infrared safe-area curve in the appropriate data bulletin. This curve depicts the safe current/voltage combinations for extended continuous operation.

Load VSWR. Excessive collector load or tuning mismatch can cause device destruction by over-dissipation or secondary breakdown. Mismatch capability is generally included on the data bulletins for the more recent rf transistors.

See RCA RF Power Transitor Manual, Technical Series RMF-430, pp 39-41, for additional information concerning the handling and mounting of rf power transistors.

*Trade Mark: Emerson and Cumming, Inc.

INTEGRATED CIRCUITS

Handling

All COS/MOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces protect COS/MOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. See ICAN-6000, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

Mounting

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress. The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

Operating

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type, such as the CD4049 or CD4050, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to V_{SS} or V_{DD}. A useful range of values for such resistors is from 10 kilohms to 1 megohm.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes. Input currents of less than 10 milliamperes prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can damage many of the higher-output-current COS/MOS types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

For detailed COS/MOS IC operating and handling considerations, refer to Application Note ICAN-6000 "Handling and Operating Considerations for MOS Integrated Circuits".

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

*Mil-M-38510A, paragraph 3.5.6.1 (a), lead material.

Technical Data-Linear IC's

RCA
Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA101, CA101A, CA201, CA201A, CA301A Types

S-Suffix Types
8-LEAD TO-5 with Dual-In-Line Formed Leads (DIL-CAN)
H-1787

T-Suffix Types
8-LEAD TO-5
H-1528

CA301AE
8-LEAD DUAL-IN-LINE PLASTIC PACKAGE (MINI-DIP) H-1817

Operational Amplifiers

For Military, Industrial, and Commercial Applications

Features:

- Short-circuit protection and latch-free operation
- Unity-gain phase compensation with a single 30-pF capacitor

		CA101	CA201	CA101A	CA201A	CA301A	
Max. V_{IO}	T_A = 25°C	5	7.5	2	2	7.5	mV
Max. I_{IO}	T_A = 25°C	200	500	10	10	50	nA
Min. A_{OL}	T_A = 25°C	50	20	50	50	25	V/mV
T_A Range (Operating)		−55 to +125	0 to +70	−55 to +125	−25 to +85	0 to +70	°C
Slew Rate (Summing ampl.)		—	—	10	10	10	V/μs

RCA-CA101, CA101A, CA201, CA201A, and CA301A are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These types, which are externally phase compensated, permit a choice of operation for optimum high-frequency performance at a selected gain; unity-gain compensation can be obtained with a single 30-pF capacitor.

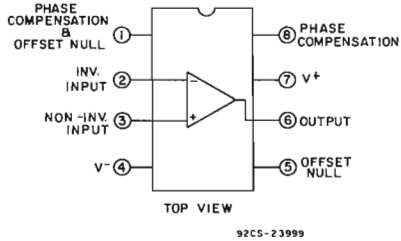
Types CA101A and CA201A have all the desirable features and characteristics of the CA101 and CA201, respectively, plus superior input-offset characteristics, and improved noise performance.

All types are available in 8-lead TO-5 style packages with standard leads (T suffix) and with dual-in-line formed leads "DIL-CAN" (S suffix). Type CA301A is also available in an 8-lead dual-in-line plastic package "MINI-DIP" (E suffix), and in chip form (H suffix).

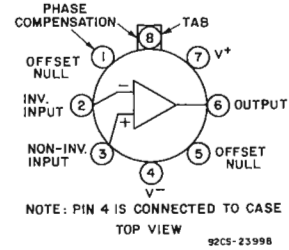
Types CA101T, S; CA101AT, S; CA201T, S; CA201AT, S; and CA301AT, S, E are direct replacements for industry types 101, 101A, 201, 201A, 301A in packages with similar terminal arrangements.

Applications:

- Long-interval integrator
- Timers
- Sample and hold circuits
- Summing amplifiers
- Multivibrators
- Comparators
- Instrumentation
- AC/DC converters
- Inverting amplifiers
- Sine- & square-wave generators
- Capacitance multipliers & simulated inductors



b — Plastic package for CA301A



a — TO-5 style package for all types

Fig.1 — Functional diagrams.

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25^oC$*

DC SUPPLY VOLTAGE (between V^+ and V^- terminals):	
CA101, CA101A, CA201, CA201A	44 V
CA301A	36 V
DC INPUT VOLTAGE	±15 V
(For supply voltage less than ± 15 V, the Input Voltage rating is equel to the DC Supply Voltage)	
DIFFERENTIAL INPUT VOLTAGE	±30 V
OUTPUT SHORT-CIRCUIT DURATION	Indefinite*
DEVICE DISSIPATION:	
Up to $T_A = 75^oC$	500 mW
Above $T_A = 75^oC$	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating —	
CA101, CA101A	−55 to +125 °C
CA201A	−25 to +85 °C
CA201, CA301A	0 to +70 °C
Storage (All types)	−65 to +150 °C
LEAD TEMPERATURE (During Soldering):	
At a distence 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C

* At $T_A \leq 70^oC$ and $T_C \leq 125^oC$ (CA101);
$T_A \leq 75^oC$ and $T_C \leq 125^oC$ (CA101A, CA201A);
$T_A \leq 55^oC$ and $T_C \leq 70^oC$ (CA201, CA301A).

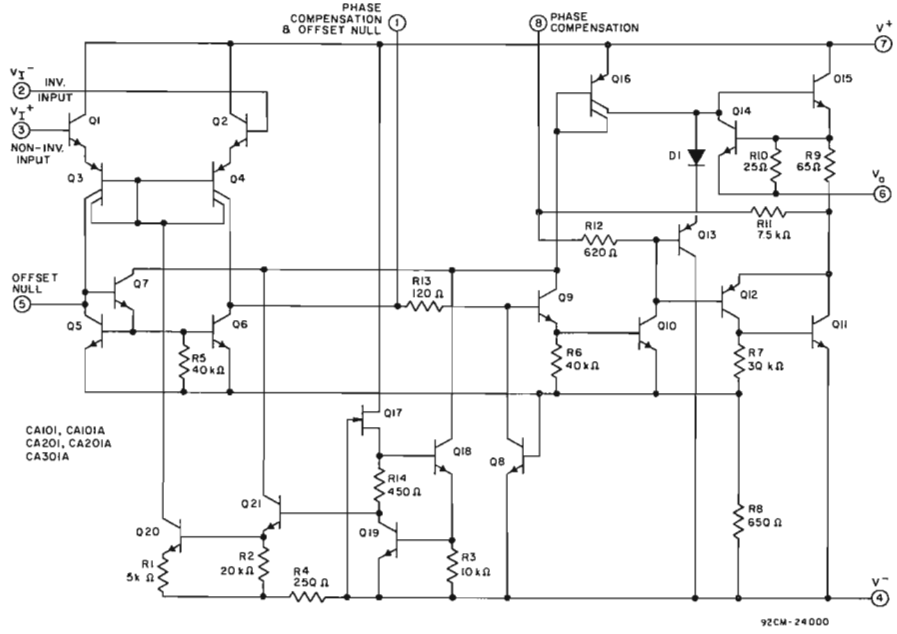


Fig.2 — Schematic diagram.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS▲ Supply Voltage ($V^{\pm}$) = 5 to 15 V		CA101			CA101A CA201A			CA201			CA301A			UNITS
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	T_A=25°C	$R_S \leq 10k\Omega$	–	1	5	–	–	–	–	2	7.5	–	–	–	mV
			$R_S \leq 50k\Omega$	–	–	–	–	0.7	2	–	–	–	–	2	7.5	
			$R_S \leq 10k\Omega$	–	–	6	–	–	–	–	–	10	–	–	–	
			$R_S \leq 50k\Omega$	–	–	–	–	–	3	–	–	–	–	–	10	
Average Temperature Coefficient of Input Offset Voltage	αV_{IO}		$R_S \leq 10k\Omega$	–	6	–	–	–	–	–	10	–	–	–	–	$\mu V/^{\circ}C$
			$R_S \leq 50\Omega$	–	3	–	–	–	–	–	6	–	–	–	–	
				–	–	–	–	3	15	–	–	–	–	6	30	
Average Temperature Coefficient of Input Offset Current	αI_{IO}	−55°C to +25°C		–	–	–	–	0.02	0.2	–	–	–	–	–	–	nA/°C
		0°C to +25°C		–	–	–	–	–	–	–	–	–	–	0.02	0.6	
		+25°C to +70°C		–	–	–	–	–	–	–	–	–	–	0.01	0.3	
		+25°C to +125°C		–	–	–	–	0.01	0.1	–	–	–	–	–	–	
Input Offset Current	I_{IO}	T_A=0°C		–	–	–	–	–	–	–	150	750	–	–	–	nA
		T_A=25°C		–	40	200	–	1.5	10	–	100	500	–	3	50	
		T_A=70°C		–	–	–	–	–	–	–	50	400	–	–	–	
		T_A=125°C		–	10	200	–	–	–	–	–	–	–	–	–	
				–	–	–	–	–	20	–	–	–	–	–	70	
		T_A=−55°C		–	100	500	–	–	–	–	–	–	–	–	–	
Input Bias Current	I_{IB}	T_A=−55°C		–	0.28	1.5	–	–	–	–	–	–	–	–	–	µA
		T_A=0°C		–	–	–	–	–	–	–	0.32	2	–	–	–	
		T_A=25°C		–	0.12	0.5	–	0.03	0.075	–	0.25	1.5	–	0.07	0.25	
				–	–	–	–	–	0.1	–	–	–	–	–	0.3	
Supply Current	$I^{\pm}$	T_A=25°C	$V^{\pm}$=15V	–	–	–	–	–	–	–	–	–	–	1.8	3	mA
			$V^{\pm}$=20V	–	1.8	3	–	1.8	3	–	1.8	3	–	–	–	
		T_A=125°C	$V^{\pm}$=20V	–	1.2	2.5	–	1.2	2.5	–	–	–	–	–	–	
Open-Loop Differential Voltage Gain	A_{OL}	T_A=25°C $V^{\pm}$=15V V_O=±10V $R_L \geq 2k\Omega$		50	160	–	50	160	–	20	150	–	25	160	–	V/mV
		$V^{\pm}$=15V V_O=±10V $R_L \geq 2k\Omega$		25	–	–	25	–	–	15	–	–	15	–	–	
Input Resistance	R_I	T_A=25°C		0.3	0.8	–	1.5	4	–	0.1	0.4	–	0.5	2	–	MΩ
Output Voltage Swing	V_{OPP}	$V^{\pm}$=15V R_L=10kΩ		±12	±14	–	±12	±14	–	±12	±14	–	±12	±14	–	V
		$V^{\pm}$=15V R_L=2kΩ		±10	±13	–	±10	±13	–	±10	±13	–	±10	±13	–	
Common-Mode Input-Voltage Range	V_{ICR}	$V^{\pm}$=15V		±12	–	–	–	–	–	±12	–	–	±12	–	–	V
		$V^{\pm}$=20V		–	–	–	±15	–	–	–	–	–	–	–	–	
Common-Mode Rejection Ratio	CMRR		$R_S \leq 10k\Omega$	70	90	–	–	–	–	65	90	–	–	–	–	dB
			$R_S \leq 50k\Omega$	–	–	–	80	96	–	–	–	–	70	90	–	
Supply-Voltage Rejection Ratio	PSRR		$R_S \leq 10k\Omega$	70	90	–	–	–	–	70	90	–	–	–	–	dB
			$R_S \leq 50k\Omega$	–	–	–	80	96	–	–	–	–	70	90	–	

▲ Characteristics applicable over operating temperature range (T_A) as shown below, unless otherwise specified:

CA101, C101A: −55 to +125°C CA201A: −25 to +85°C CA201, CA301A: 0 to 70°C

TYPICAL STATIC CHARACTERISTICS

Type CA101

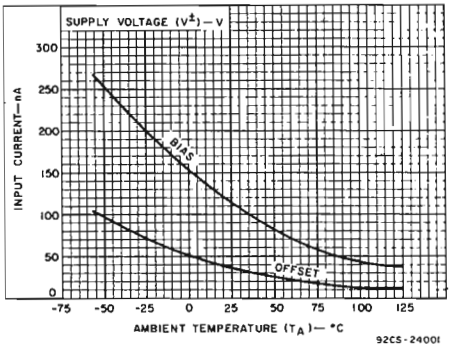


Fig.3 — Input current (I_{IO}, I_{IB}) vs. temperature.

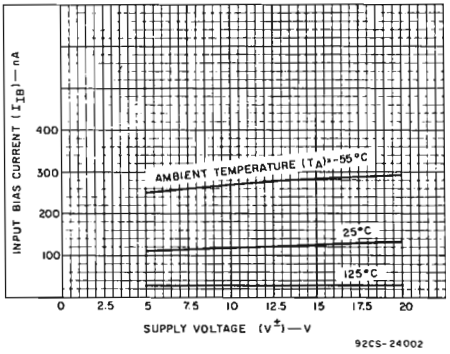


Fig.4 — Input bias current vs. supply voltage.

Types CA101A and CA201A

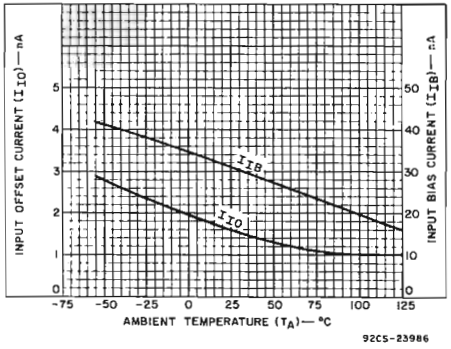


Fig. 5 — Input current (I_{IO}, I_{IB}) vs. temperature.

Types CA101, CA101A, and CA201A

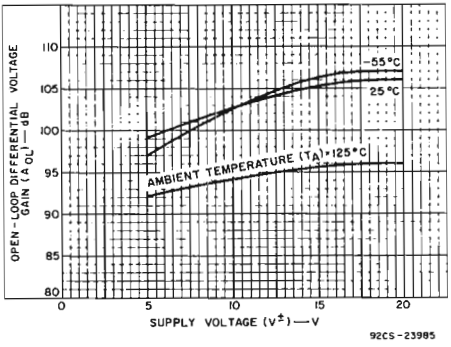


Fig.6 — Voltage gain vs. supply voltage.

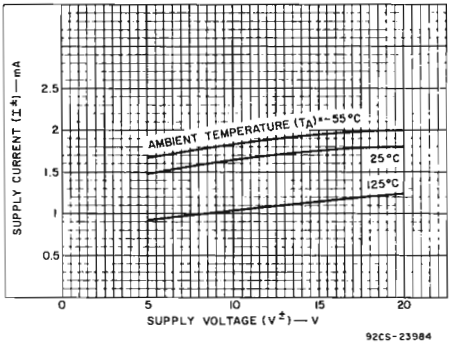


Fig.7 — Supply characteristics.

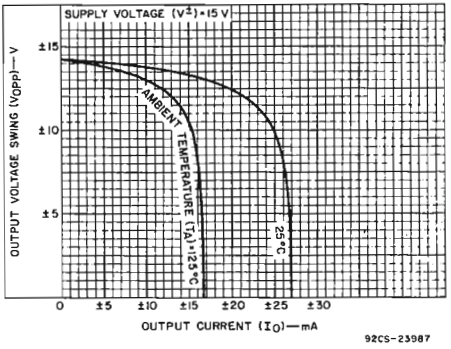


Fig.8 — Output characteristics.

TYPICAL STATIC CHARACTERISTICS (Cont'd)

Type CA201

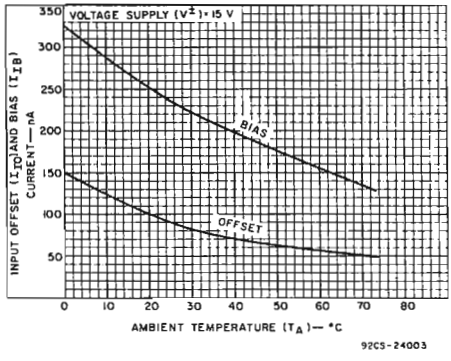


Fig.9 – Input current (I_{IO}, I_{IB}) vs. temperature.

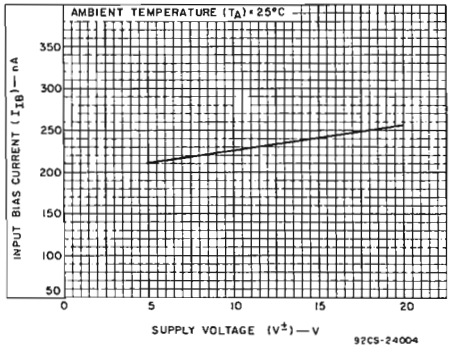


Fig.10 – Input bias current (I_{IB}) vs. supply voltage.

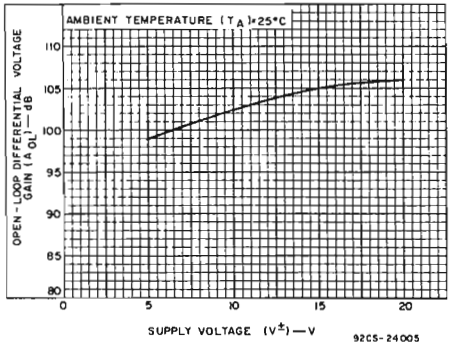


Fig.11 – Voltage gain vs. supply voltage.

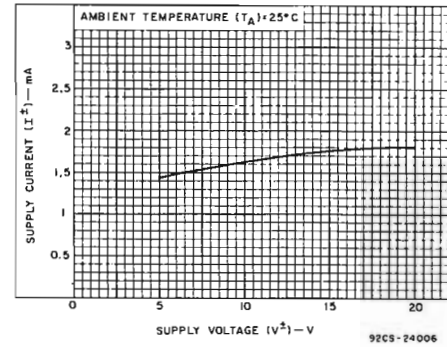


Fig.12 – Supply characteristics.

Type CA301A

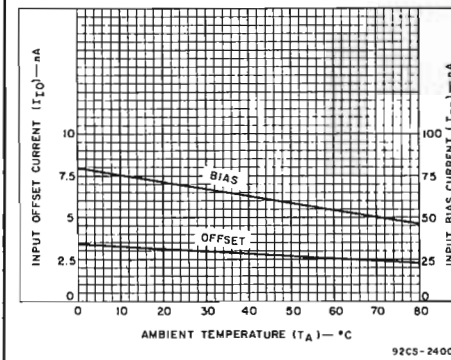


Fig.13 – Input current (I_{IO}, I_{IB}) vs. temperature.

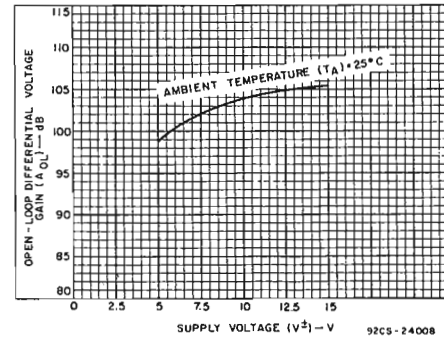


Fig.14 – Voltage gain vs. supply voltage.

TYPICAL STATIC CHARACTERISTICS (Cont'd)
Type CA301A

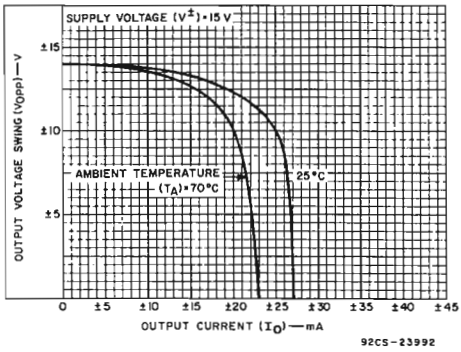


Fig. 15 — Output characteristics.

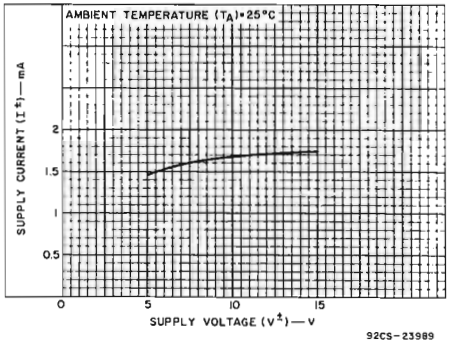


Fig. 16 — Supply characteristics.

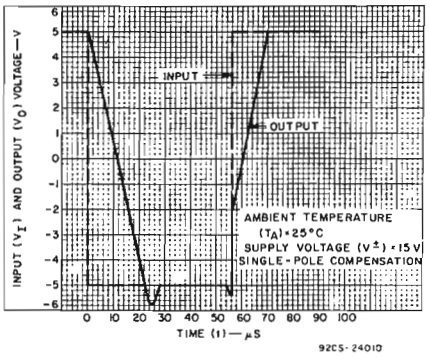


Fig. 18 — Voltage follower (V_I, V_O) pulse response.

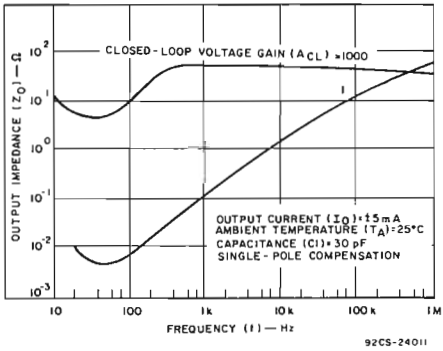


Fig. 19 — Closed-loop output impedance vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA101A AND CA201A

Single-Pole Compensation

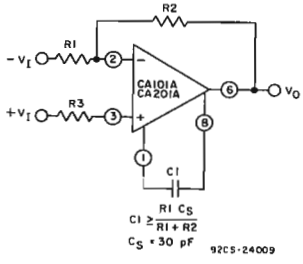


Fig. 17 — Test circuit employing single-pole compensation.

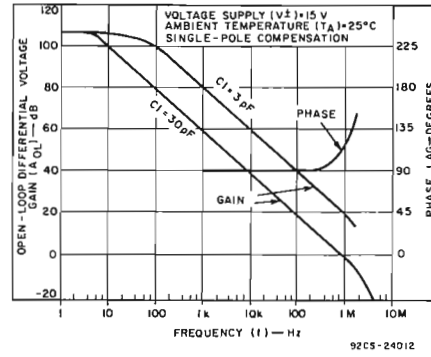


Fig. 20 — Voltage gain and phase lag vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA101A AND CA201A

Single-Pole Compensation (Cont'd)

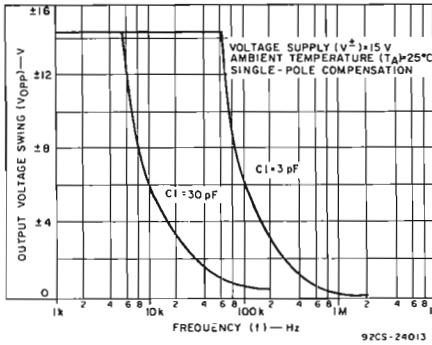


Fig.21 – Output voltage swing vs. frequency.

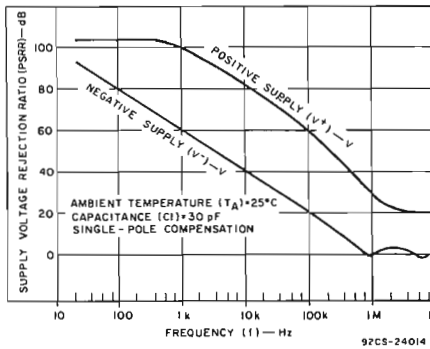


Fig.22 – Supply voltage rejection ratio vs. frequency.

FOR TYPES CA101A AND CA201A

Two-Pole Compensation

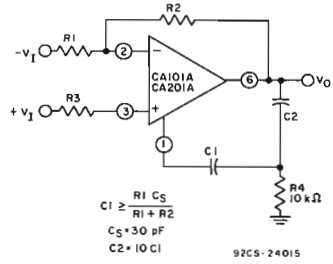


Fig.23 – Test circuit employing two-pole compensation.

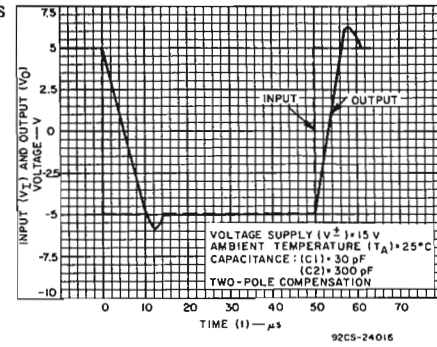


Fig.24 – Voltage follower pulse response.

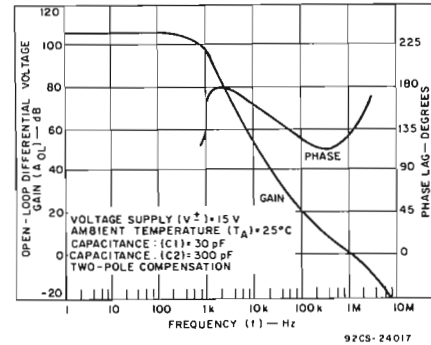


Fig.25 – Voltage gain and phase lag vs. frequency.

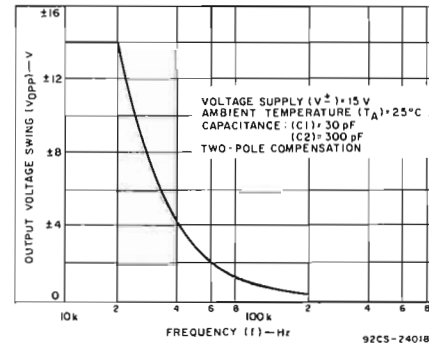


Fig.26 – Output voltage swing vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS (Cont'd) FOR TYPES CA101A AND CA201A

Feed-Forward Compensation

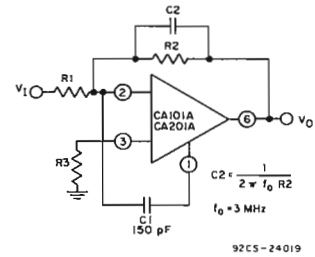


Fig.27 – Test circuit employing feedforward compensation.

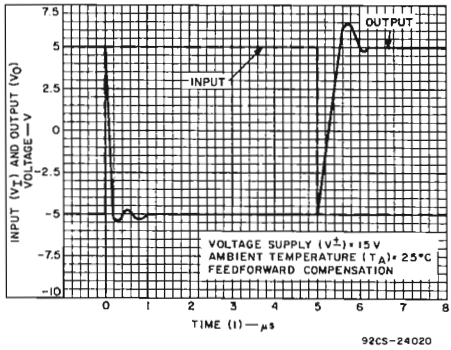


Fig.28 – Inverter pulse response.

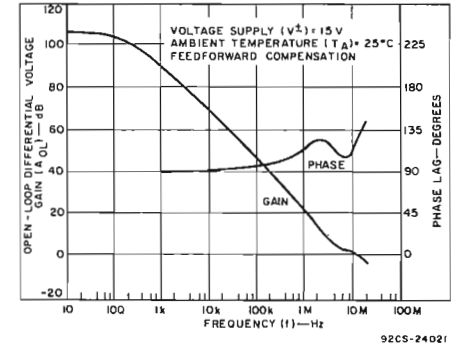


Fig.29 – Voltage gain and phase lag vs. frequency.

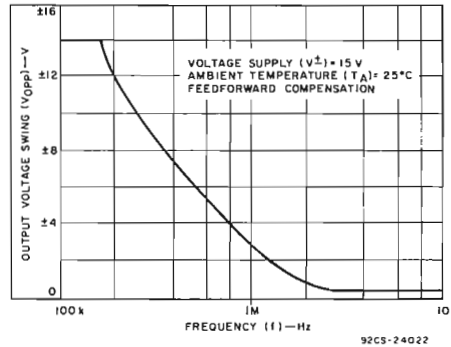


Fig.30 – Output voltage swing vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS FOR TYPES CA101A AND CA201A

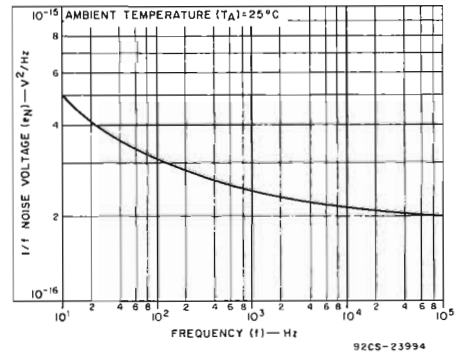


Fig.31 – I/f noise voltage vs. frequency.

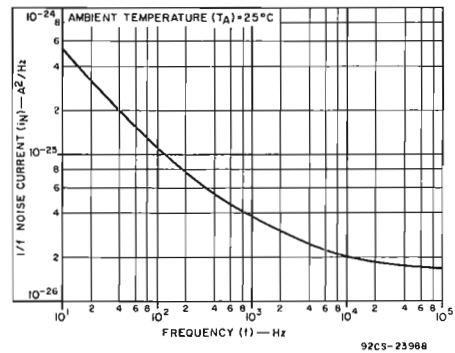


Fig.32 – I/f noise current vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS (Cont'd)

FOR TYPES CA101A AND CA201A

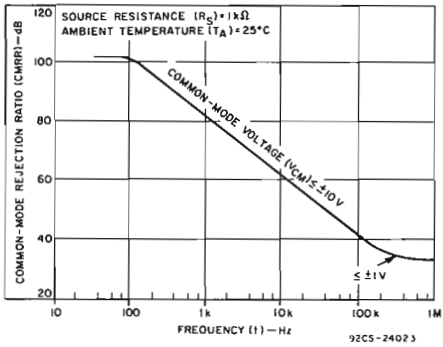


Fig.33 – Common-mode rejection ratio vs. frequency.

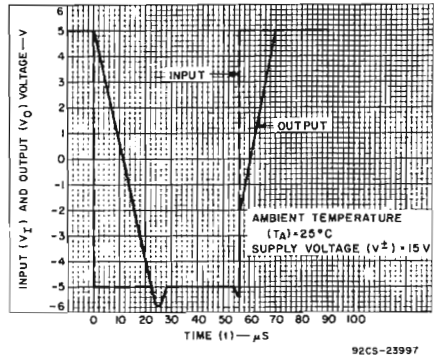


Fig.36 – Voltage follower pulse response.

Types CA101, CA201, CA301A

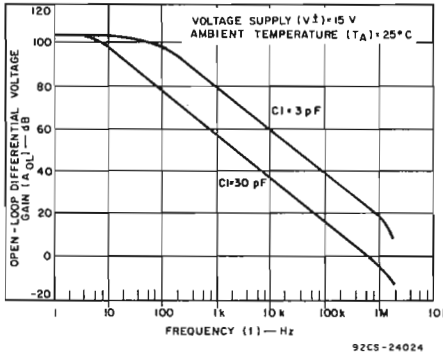


Fig.34 – Voltage gain vs. frequency.

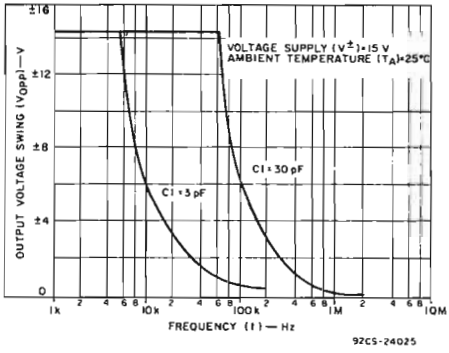


Fig.35 – Output voltage swing vs. frequency.

Type CA301A

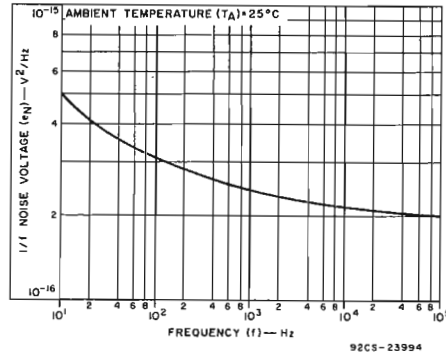


Fig.37 – I/f noise voltage vs. frequency.

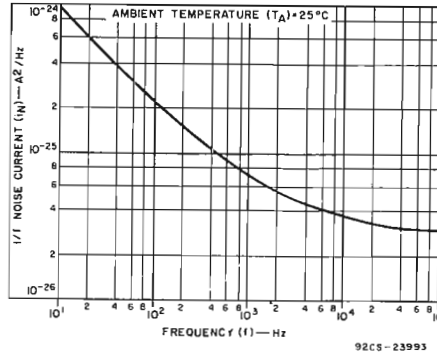


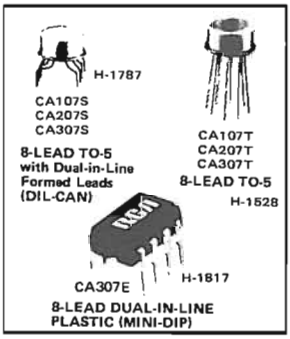
Fig.38 – I/f noise current vs. frequency.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA107, CA207, CA307 Types



Operational Amplifiers

For Military, Industrial, and Commercial Applications

Type \ Feature	Max. V_{IO} (mV)	Max. I_{IO} (nA)	Max. I_{IB} (nA)	Temp. Range (T_A) °C
CA107	3	20	100	−55 to +125
CA207	3	20	100	−25 to +85
CA307	10	70	300	0 to +70

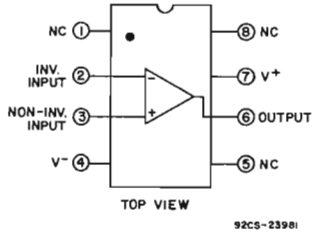
RCA-CA107, CA207, CA307 are general-purpose operational amplifiers intended for use in military, industrial, and commercial applications. A 30-pF on-chip capacitor provides internal frequency compensation. Low input current over temperature range (100 nA max.) for the CA107 and CA207 make these types especially well suited for applications such as long interval timers and sample-and-hold circuits.

The CA107, CA207, and CA307 are supplied in the standard 8-lead TO-5 style package ("T" suffix), the 8-lead TO-5 style with dual-in-line formed leads ("S" suffix), and in chip form ("H" suffix). The CA307 is also available in the 8-lead dual-in plastic "MINI-DIP" package ("E" suffix).

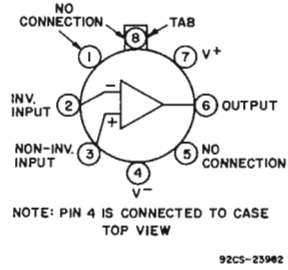
Applications:

- Long-interval integrators
- Timers
- Sample-and-hold circuits
- Summing amplifiers
- Multivibrators

The CA107T,S, CA207T,S, and CA307T,S,E are direct replacements for industry types 107, 207, and 307 in packages with similar terminal arrangements.



FUNCTIONAL DIAGRAM FOR PLASTIC PACKAGE.



FUNCTIONAL DIAGRAM FOR TO-5 STYLE PACKAGES.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals):		
CA107, CA207	44	V
CA307	36	V
DC INPUT VOLTAGE	±15	V
(For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage)		
DIFFERENTIAL INPUT VOLTAGE	±30	V
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite	
DEVICE DISSIPATION UP TO T_A = 70°C	500	mW
Above T_A = 70°C Derate linearly at	6.67	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating – CA107	−55°C to +125°C	
CA207	−25°C to +85°C	
CA307	0°C to +70°C	
Storage – All Types	−65°C to +150°C	
LEAD TEMPERATURE (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C	

* For CA307 continuous short circuit is allowed for Case Temperature to +70°C and ambient temperature to +55°C.

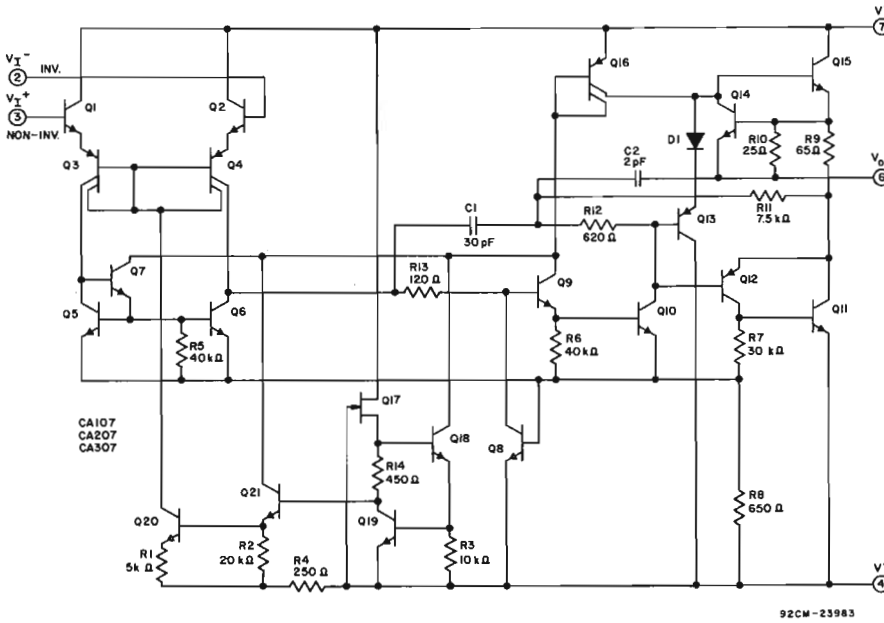


Fig. 1 – Schematic diagram of CA107, CA207, and CA307.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS▲ Supply Voltage ($V^{\pm}$) = 5 V to 15 V	LIMITS						UNITS
			CA107 CA207			CA307			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	$T_A = 25°C$, $R_S \leq 50\ k\Omega$	–	0.7	2	–	2	7.5	mV
		$R_S \leq 50\ k\Omega$	–	–	3	–	–	10	
Average Temperature Coefficient of Input Offset Voltage	αV_{IO}		–	3	15	–	6	30	$\mu V/°C$
Input Offset Current	I_{IO}		–	–	20	–	–	70	nA
		$T_A = 25°C$	–	1.5	10	–	3	50	
Average Temperature Coefficient of Input Offset Current	αI_{IO}	See Note 1	–	0.01	0.1	–	0.01	0.3	nA/°C
		See Note 2	–	0.02	0.2	–	0.02	0.6	
Input Bias Current	I_{IB}		–	–	100	–	–	300	nA
		$T_A = 25°C$	–	30	75	–	70	250	
Supply Current	$I^{\pm}$	$T_A = +125°C$, $V^{\pm} = 20$ V	–	1.2	2.5	–	–	–	mA
		$T_A = 25°C$, $V^{\pm} = 20$ V, (CA307 $V^{\pm} = 15$ V)	–	1.8	3	–	1.8	3	
Open-Loop Differential Voltage Gain	A_{OL}	$V^{\pm} = 15$ V, $V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25	–	–	15	–	–	V/mV
		$V^{\pm} = 15$ V, $V_O = \pm 10$V $R_L \geq 2\ k\Omega$, $T_A = 25°C$	50	160	–	25	160	–	
Input Resistance	R_I	$T_A = 25°C$	1.5	4	–	0.5	2	–	MΩ
Output Voltage Swing	V_{OPP}	$V^{\pm} = 15$ V, $R_L = 10\ k\Omega$	±12	±14	–	±12	±14	–	V
		$V^{\pm} = 15$ V, $R_L = 2\ k\Omega$	±10	±13	–	±10	±13	–	
Input Voltage Range	V_{ICR}	$V^{\pm} = 20$ V, (CA307 $V^{\pm} = 15$ V)	±15	–	–	±12	–	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 50\ k\Omega$	80	96	–	70	90	–	dB
Supply-Voltage Rejection Ratio	PSRR	$R_S \leq 50\ k\Omega$	80	96	–	70	96	–	dB

Note 1: For CA107, +25 to +125°C; For CA207, +25 to +85°C: For CA307, +25 to 70°C.

Note 2: For CA107, –55 to +25°C; For CA207, –25 to +25°C: For CA307, 0 to +25°C.

▲ Characteristics applicable over operating temperature range as shown below unless otherwise specified.

CA107 – T_A = –55 to +125°C

CA207 – T_A = –25 to +85°C

CA307 – T_A = 0 to 70°C

TYPICAL CHARACTERISTICS FOR CA107, CA207

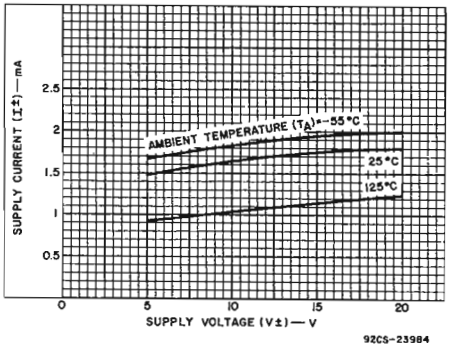


Fig. 2 – Supply current vs. supply voltage.

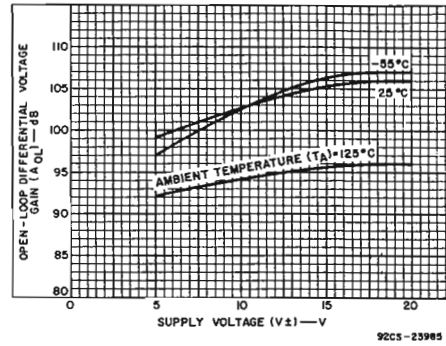


Fig. 3 – Open-loop differential voltage gain vs. supply voltage.

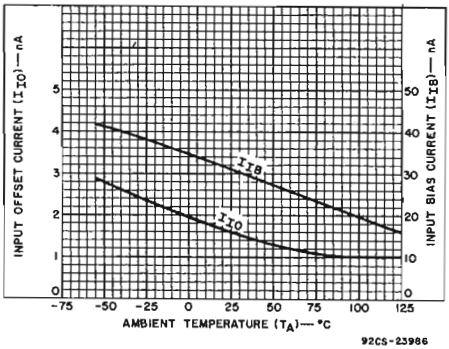


Fig. 4 – Input offset and input bias current vs. ambient temperature.

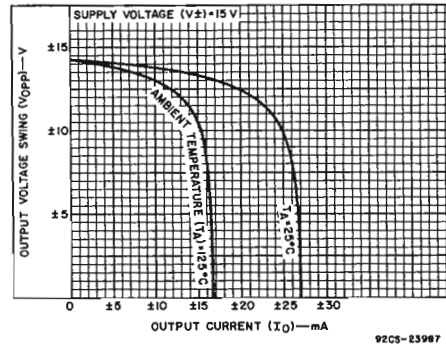


Fig. 5 – Output voltage swing vs. output current.

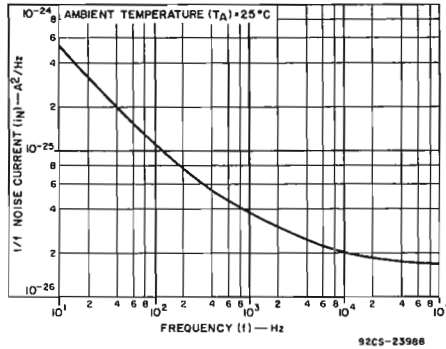


Fig. 6 – 1/f noise current vs. frequency.

TYPICAL CHARACTERISTICS FOR CA307

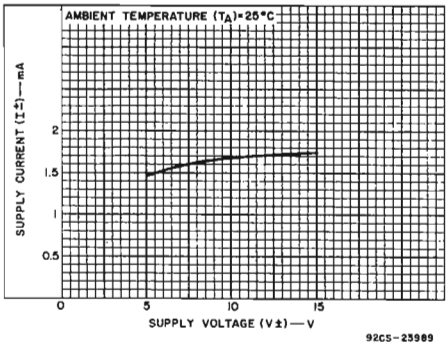


Fig. 7 – Supply current vs. supply voltage.

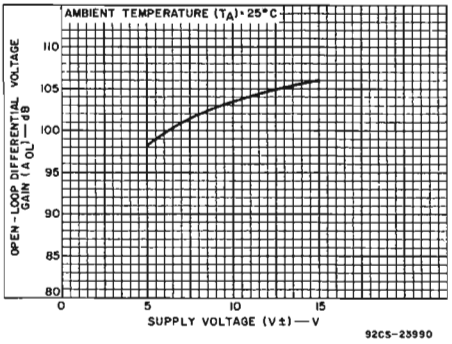


Fig. 8 – Open-loop differential voltage gain vs. supply voltage.

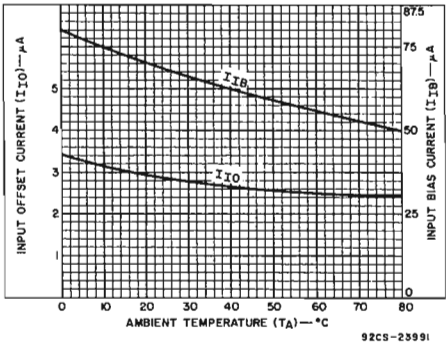


Fig. 9 – Input offset and input bias current vs. ambient temperature.

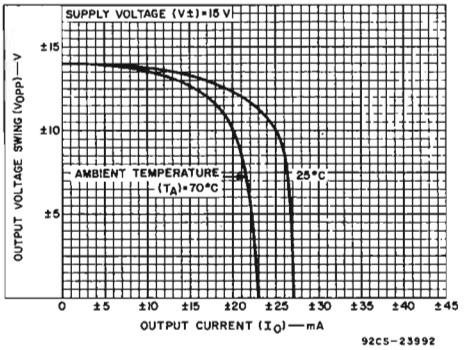


Fig. 10 – Output voltage swing vs. output current.

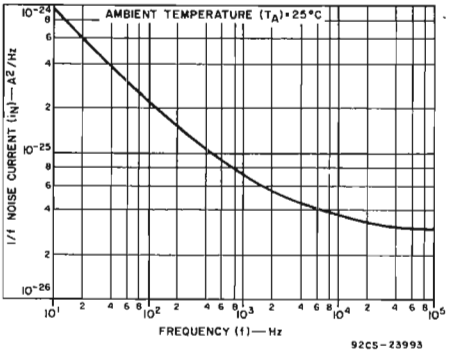


Fig. 11 – 1/f noise current vs. frequency.

TYPICAL CHARACTERISTICS FOR ALL TYPES

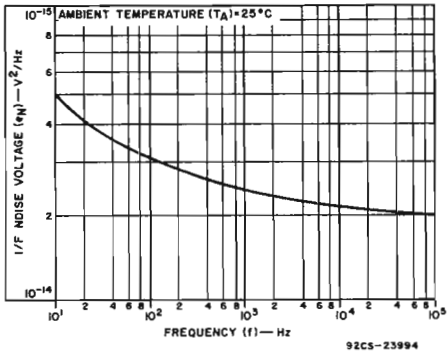


Fig. 12 – 1/f noise voltage vs. frequency.

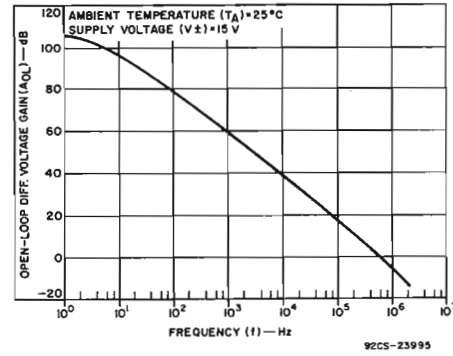


Fig. 13 – Open-loop differential voltage gain vs. frequency.

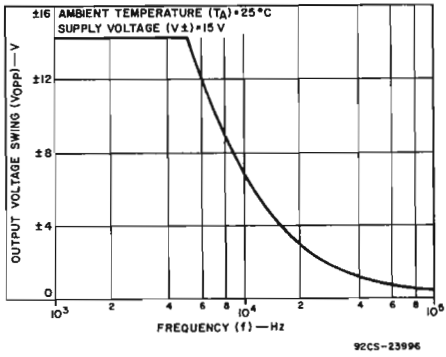


Fig. 14 – Output voltage swing vs. frequency.

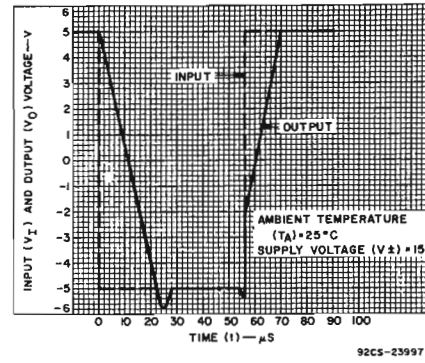


Fig. 15 – Input and output voltage vs. time.

RCA
Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA108T CA108S CA108AT CA108AS
CA208T CA208S CA208AT CA208AS
CA308T CA308S CA308AT CA308AS

CA108S, AS
CA208S, AS
CA308S, AS

8-LEAD TO-5
with Dual-In-Line
Formed Leads

H-1787

CA108T, AT
CA208T, AT
CA308T, AT

8-LEAD TO-5

H-1528

Precision Operational Amplifiers

For Military, Industrial, and Commercial Applications

Features:

- Maximum input bias current — 2 nA for CA108 & CA208 series
  7 nA for CA308 series
- Maximum input offset current — 0.2 nA for CA108 & CA208 series
  1 nA for CA308 series
- Supply current of only 300 μA, even in saturation
- Maximum input offset voltage of 0.5 mV for "A" suffix types

RCA-CA108T, CA108AT, CA108S, CA108AS, CA208T, CA208AT, CA208S, CA208AS, CA308T, CA308AT, CA308S, and CA308AS are uncompensated precision operational amplifiers using super-beta transistors and feature very low offset parameters, high input impedance, and defined drift rates with temperature change.

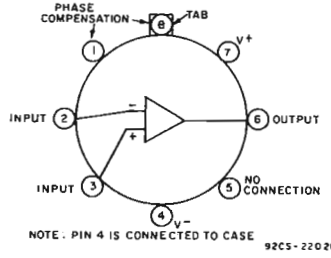
In addition to low drift, these super-beta op-amps have input currents sufficiently low to insure low drift, even when using high source resistances, e.g., 10 megohms.

These devices have sufficient supply rejection to operate from unregulated power supplies within a range of ±2 V to ±20 V, and the input bias current is specifically controlled for use in sample-and-hold applications.

The "A" versions have all the desirable features and characteristics of their prototypes plus exceptionally low input offset voltage characteristics. The CA108, CA108A, CA208, CA208A, CA308, and CA308A are direct replacements for industry types 108,108A,208,208A,308,308A, and they are supplied in either standard 8-lead TO-5 packages or in 8-lead TO-5 packages with dual-in-line formed leads ("DIL-CAN").

Applications:

- Instrumentation
- Summing amplifier
- Comparator
- Multivibrators
- Band-pass filters
- Sample and hold



NOTE: PIN 4 IS CONNECTED TO CASE

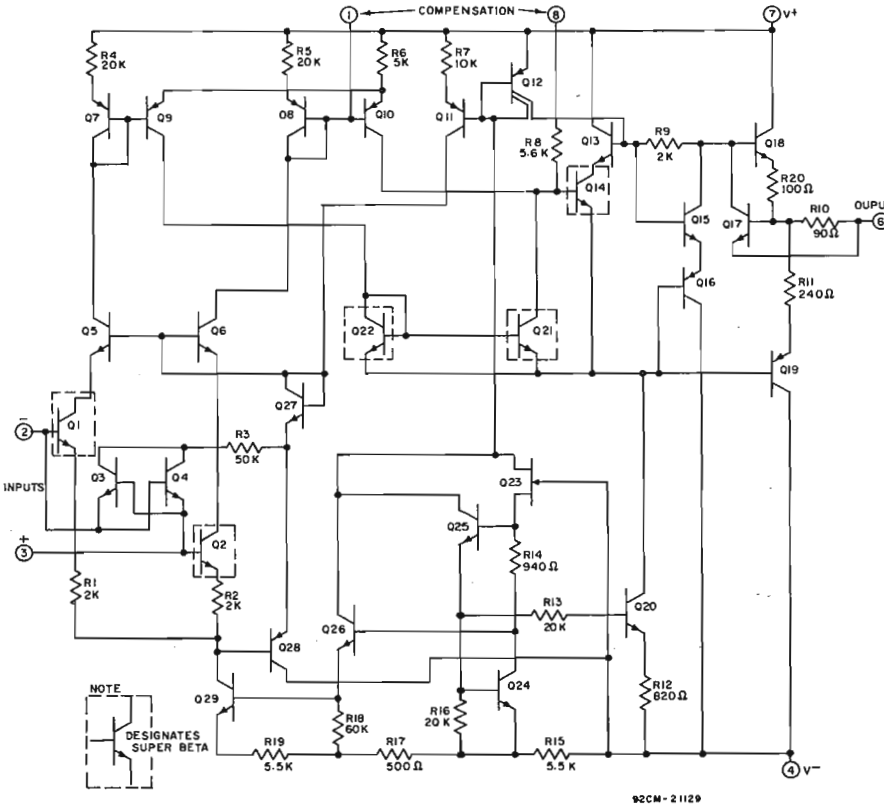
92CS-22020

FUNCTIONAL DIAGRAM

ELECTRICAL CHARACTERISTICS, MAXIMUM VALUES AT T_A = 25°C	CA108T CA108S	CA108AT CA108AS	CA208T CA208S	CA208AT CA208AS	CA308T CA308S	CA308AT CA308AS
Input Offset Voltage (V_{IO})	2 mV	0.5 mV	2 mV	0.5 mV	7.5 mV	0.5 mV
Input Offset Current (I_{IO})	0.2 nA				1 nA	
Input Bias Current (I_{IB})	2 nA			7 nA		
Average Temperature Coefficient of Input Offset Voltage ($\Delta V_{IO}/\Delta T$)	15 μV/°C	5 μV/°C	15 μV/°C	5 μV/°C	30 μV/°C	5 μV/°C
Ambient Operating-Temperature Range	−55 to +125°C		−25 to +85°C		0 to +70°C	

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25^oC$:*

DC Supply Voltage (Between V^+ and V^- Terminals):	
CA108, CA108A, CA208, CA208A	40 V
CA308, CA308A	36 V
DC Input Voltage	±15 V
(For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage)	
Differential Input Current	±10 mA
Output Short-Circuit Duration	Indefinite
Device Dissipation	500 mW
Ambient Temperature Range:	
Operating – CA108, CA108A	-55^oC to $+125^oC$
CA208, CA208A	-25^oC to $+85^oC$
CA308, CA308A	0^oC to $+70^oC$
Storage – All Types	-65^oC to $+150^oC$
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	$+300\ ^oC$



ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS FIG. No.	TEST CONDITIONS Supply Voltage (V) = ±5 V to ±15 V	LIMITS CA108 CA208 Min.	CA108 CA208 Typ.	CA108 CA208 Max.	CA108A CA208A Min.	CA108A CA208A Typ.	CA108A CA208A Max.	CA308 Min.	CA308 Typ.	CA308 Max.	CA308A Min.	CA308A Typ.	CA308A Max.	UNITS
Input Offset Voltage	V_{IO}	6,7	T_A = 25°C	–	0.7	2	–	0.3	0.5	–	2	7.5	–	0.3	0.5	mV
			Note 1	–	–	3	–	–	1	–	–	10	–	–	0.73	
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{IO}}{\Delta T}$		Note 1	–	3	15	–	1	5	–	6	30	–	1	5	µV/°C
Input Offset Current	I_{IO}	8,9	Note 1	–	–	0.4	–	–	0.4	–	–	1.5	–	–	1.5	nA
			T_A = 25°C	–	0.05	0.2	–	0.05	0.2	–	0.2	1	–	0.2	1	
Average Temperature Coefficient of Input Offset Current	$\frac{\Delta I_{IO}}{\Delta T}$		Note 1	–	0.5	2.5	–	0.5	2.5	–	2	10	–	2	10	pA/°C
Input Bias Current	I_{IB}	10, 11	Note 1	–	–	3	–	–	3	–	–	10	–	–	10	nA
			T_A = 25°C	–	0.8	2	–	0.8	2	–	1.5	7	–	1.5	7	
Supply Current	I_O	12, 13	T_A = +125°C	–	0.15	0.4	–	0.15	0.4	–	–	–	–	–	–	mA
			T_A = 25°C	–	0.3	0.6	–	0.3	0.6	–	0.3	0.8	–	0.3	0.8	
Large-Signal Voltage Gain	A_V	2,14 15	V = ±15 V, T_A = 25°C V_O = ±10 V, $R_L \geq 10$ kΩ	50	300	–	80	300	–	25	300	–	80	300	–	V/mV
			V = ±15 V, V_O = ±10 V $R_L \geq 10$ kΩ, Note 1	25	–	–	40	–	–	15	–	–	60	–	–	
Input Resistance	R_I		T_A = 25°C	30	70	–	30	70	–	10	40	–	10	40	–	MΩ
Output Voltage	V_O	16, 17	V = ±15 V, R_L = 10 kΩ, Note 1	±13	±14	–	±13	±14	–	±13	±14	–	±13	±14	–	V
Input Voltage Range	V_I		V = ±15 V, Note 1	±13.5	–	–	±13.5	–	–	±14	–	–	±14	–	–	
Common-Mode Rejection Ratio	CMRR		Note 1	85	100	–	96	110	–	80	100	–	96	110	–	dB
Supply-Voltage Rejection Ratio	V_{RR}		Note 1	80	96	–	96	110	–	80	96	–	96	110	–	

Note 1: Ambient Temperature (T_A) over applicable operating temperature range as shown below unless otherwise specified.

CA108 CA108A	CA208 CA208A	CA308 CA308A
−55 to +125°C	−25 to +85°C	0 to +70°C

TEST CIRCUITS

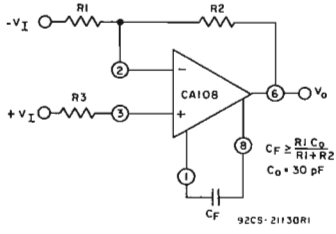


Fig. 2—Standard frequency-compensation.

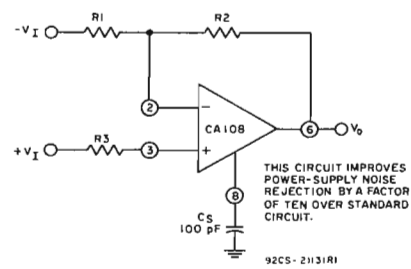


Fig. 3—Alternate frequency-compensation.

TYPICAL APPLICATIONS

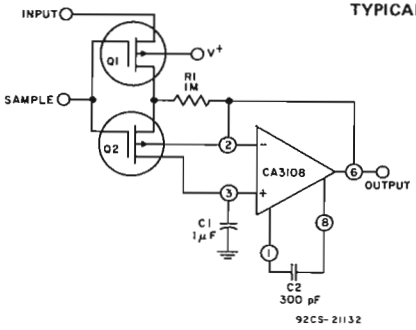


Fig. 4 – Sample-and-hold circuit.

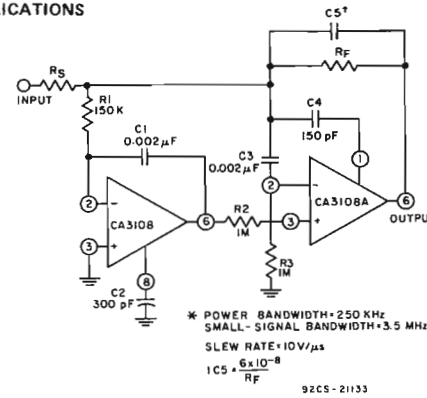


Fig. 5 – Fast summing amplifier circuit.*

CHARACTERISTIC CURVES

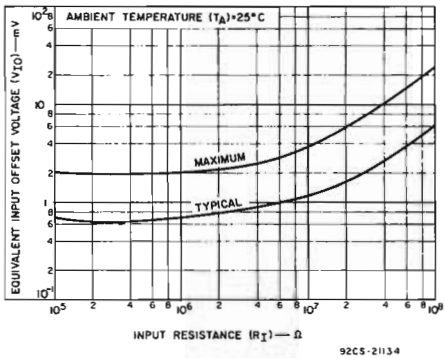


Fig. 6 – Input offset error for CA108, CA108A, CA208, and CA208A.

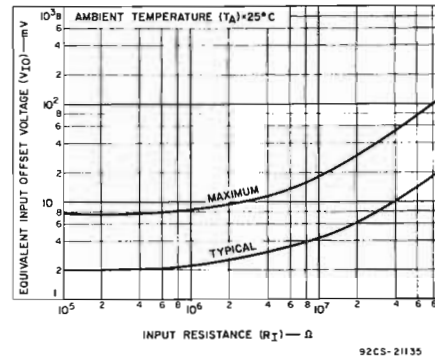


Fig. 7 – Input offset error for CA308 and CA308A.

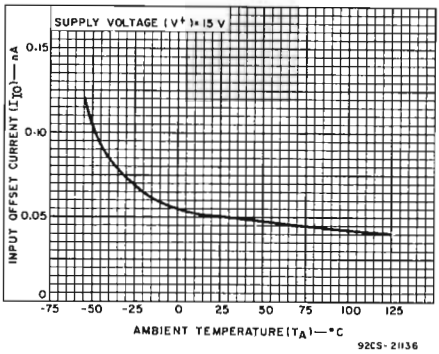


Fig. 8 – Input offset current vs. temperature for CA108, CA108A, CA208, and CA208A.

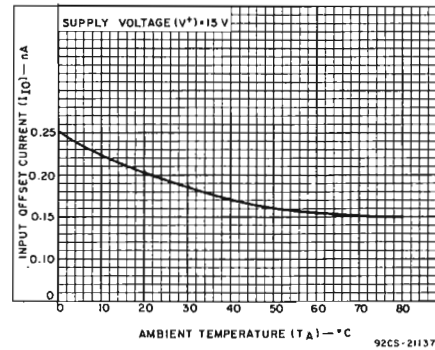


Fig. 9 – Input offset current vs. temperature for CA308 and CA308A.

CHARACTERISTIC CURVES (Cont'd)

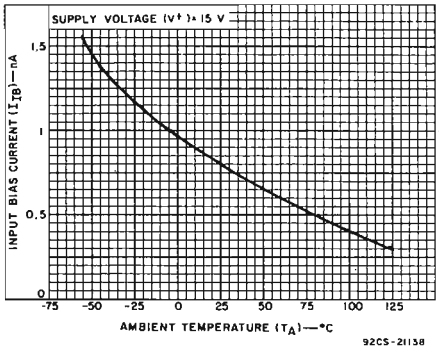


Fig. 10 – Input bias current vs. temperature for CA108, CA108A, CA208, and CA208A.

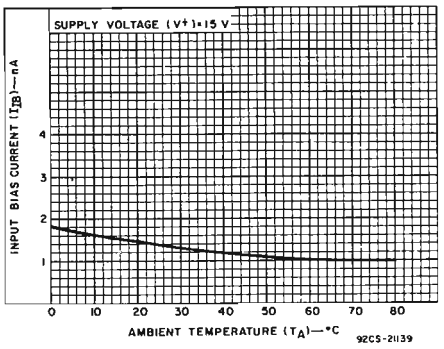


Fig. 11 – Input bias current vs. temperature for CA308 and CA308A.

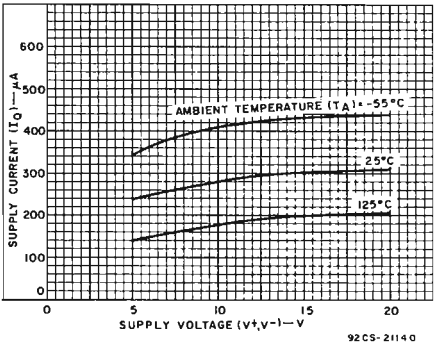


Fig. 12 – Supply current vs. supply voltage for CA108, CA108A, CA208, and CA208A.

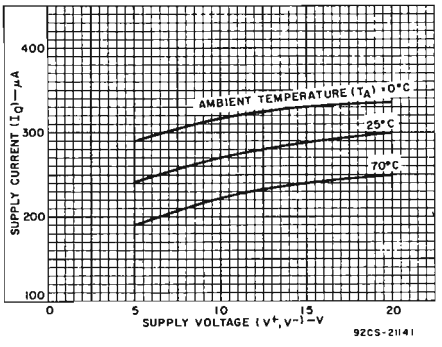


Fig. 13 – Supply currant vs. supply voltage for CA308 CA308A.

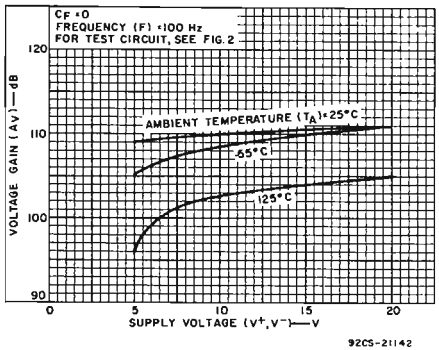


Fig. 14 – Voltage gain vs. supply voltage for CA108, CA108A, CA208, and CA208A.

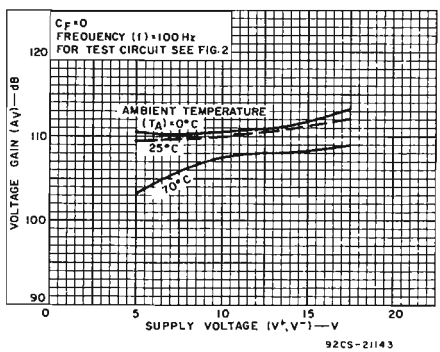


Fig. 15 – Voltage gain vs. supply voltage for CA308 and CA308A.

CHARACTERISTIC CURVES (Cont'd)

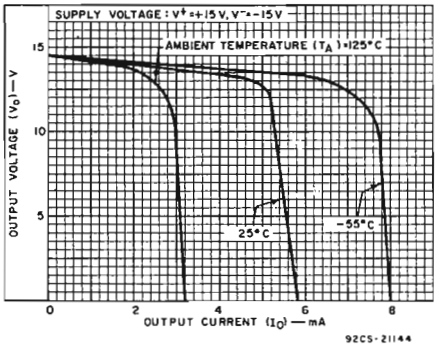


Fig. 16 – Output voltage vs. output current for CA108, CA108A, CA208, and CA208A.

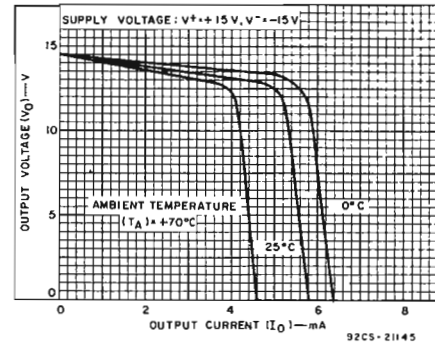


Fig. 17 – Output voltage vs. output current for CA308 and CA308A.

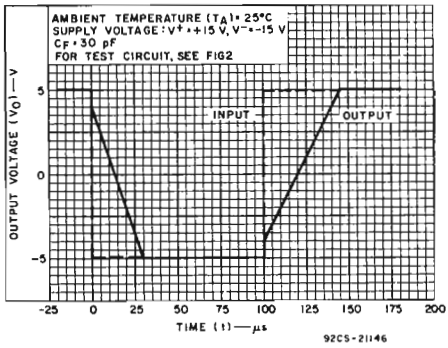


Fig. 18 – Voltage-follower pulse response for all types.

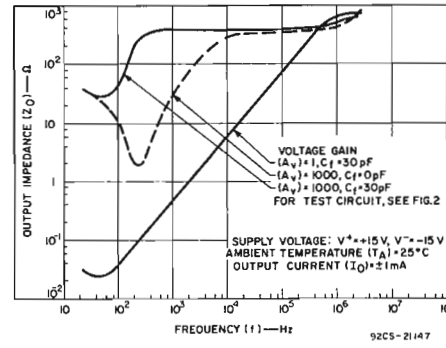


Fig. 19 – Closed-loop output impedance for all types.

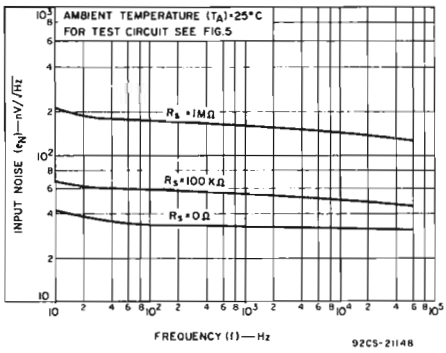


Fig. 20 – Input noise voltage for all types.

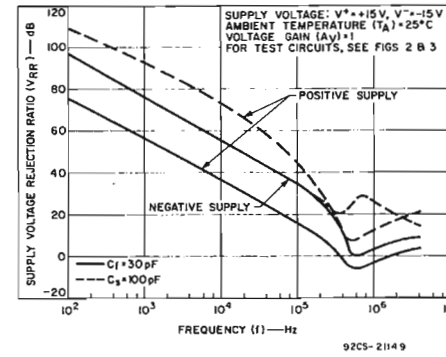


Fig. 21 – Power-supply rejection for all types.

CHARACTERISTIC CURVES (Cont'd)

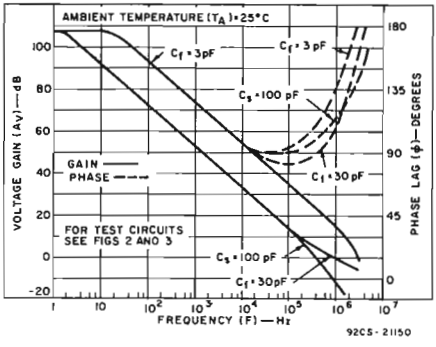


Fig. 22 – Open-loop frequency response for all types.

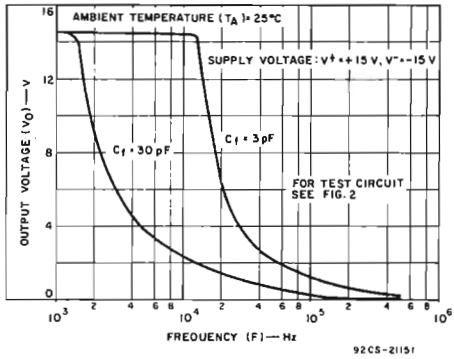


Fig. 23 – Large-signal frequency response for all types.

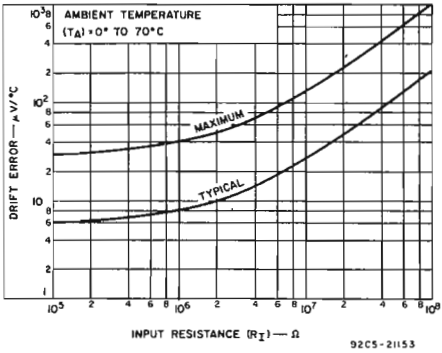


Fig. 24 – Drift error vs. input resistance for CA108, CA108A, CA208, and CA208A.

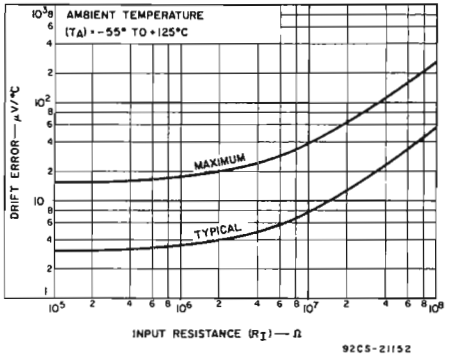


Fig. 25 – Drift error vs. input resistance for CA308 and CA308A.

RCA
Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA111, CA211, CA311 Types

("S" SUFFIX)
8-LEAD TO-5 with Dual-In-Line Formed Leads "DIL-CAN"
H-1787

("T" SUFFIX)
8-LEAD TO-5
H-1528

Voltage Comparators

For Commercial and Industrial Applications

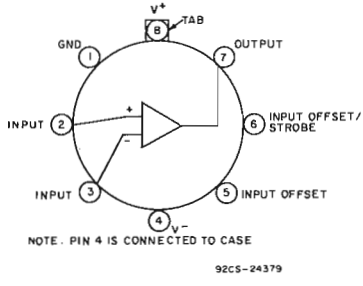
Features

- Single- or dual-supply operation
- Power consumption — 135 mW at ±15 V
- Strobe capability
- Low input-offset current:
  CA111, CA211 — 4 nA (typ.)
  CA311 — 6 nA (typ.)
- Differential input-voltage range — ±30 V
- Directly interchangeable with National Semiconductor types LM111H, LM211H, and LM311

The RCA-CA111, CA211, and CA311 are monolithic voltage comparators that operate from dual supplies up to ±15 V, or from single supplies down to 5 V. This single-supply capability makes the outputs of these devices compatible with RTL, DTL, TTL, and MOS circuits. In addition, they can drive lamps or relays, and switch voltages up to 50 V (CA311, 40 V) at currents as high as 50 mA.

The inputs and the outputs of the CA111, CA211, and CA311 can be isolated from system ground, allowing the output to drive loads referred to ground, V^+, or V^-.

The CA111, CA211, and CA311 are supplied in the 8-lead TO-5 style package ("T" suffix), and the "DIL-CAN", an 8-lead TO-5 style package with dual-in-line formed leads ("S" suffix). The CA311 is also supplied in chip form ("H" suffix). These types are direct replacements for industry types 111, 211, and 311 in similar packages.



FUNCTIONAL DIAGRAM

Applications

- Multivibrators
- Positive and negative peak detectors
- Crystal oscillators
- Zero-crossing detectors
- Solenoid, relay, and lamp drivers

MAXIMUM RATINGS, *Absolute Maximum Values at* $T_A = 25^\circ C$

DC SUPPLY VOLTAGE (between V^+ and V^- terminals)	36 V
DC INPUT VOLTAGE*	±15 V
DIFFERENTIAL INPUT VOLTAGE	±30 V
OUTPUT TO NEGATIVE SUPPLY VOLTAGE (V_{7-4}):	
CA111, CA211	50 V
CA311	40 V
GROUND TO NEGATIVE SUPPLY VOLTAGE (V_{1-4})	30 V
OUTPUT SHORT-CIRCUIT DURATION	10 s
DEVICE DISSIPATION:	
Up to $T_A = 25^\circ C$	500 mW
Above $T_A = 25^\circ C$	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating:	
CA111	−55 to +125°C
CA211	−25 to +85°C
CA311	0 to +70°C
Storage, all types	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

*This rating applies for ±15 V supplies. The positive input-voltage limit is 30 V above the negative supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS FIG. NO.	SUPPLY VOLTAGE ($V^{\pm}$) = 15 V UNLESS OTHERWISE SPECIFIED		LIMITS CA111 CA211 TYP.	CA111 CA211 MAX.	CA311 TYP.	CA311 MAX.	UNITS
Input Offset Voltage	V_{IO}	16,24	$R_S \leq 5$ kΩ, Note 2	T_A=25°C	0.7	3	2	7.5	mV
				Note 1	–	4	–	10	
Saturation Voltage		13,22	V_I = –5 mV, I_O = 50 mA (For CA311, V_I = –10 mV)	T_A=25°C	0.75	1.5	–	–	V
			$V^+ \geq$ 4.5 V, V^- = 0, V_I = –6 mV, $I_{SINK} \leq$ 8 mA (For CA311, V_I = –10 mV)	Note 1	0.23	0.4	–	–	
Input Voltage Range	V_{IPP}			Note 1	±14	–	±14	–	V
Input Offset Current	I_{IO}	9,18	Note 2	T_A=25°C	4	10	6	50	nA
				Note 1	–	20	–	70	
Input Bias Current	I_{IB}	8,17	Note 2	T_A=25°C	60	100	100	250	nA
				Note 1	–	150	–	300	
Positive Supply Current	I^+			T_A=25°C	5.1	6	5.1	7.5	mA
Negative Supply Current	I^-			T_A=25°C	4.1	5	4.1	5	mA
Output Leakage Current		15,24	$V_I \geq$ 5 mV, V_O = 35 V (For CA311, V_I = –10 mV)	T_A=25°C	0.2	10	–	–	nA
				Note 1	0.1	0.5	–	–	μA
Strobe On Current				T_A=25°C	3	–	3	–	mA
Voltage Gain	A			T_A=25°C	200	–	200	–	V/mV
Response Time		2,3, 4,5	100 mV Input Step with 5 mV overdrive voltage	T_A=25°C	200	–	200	–	ns

Note 1: Ambient temperature (T_A) over applicable operating temperature range as shown below.

CA111	CA211	CA311
–55 to +125°C	–25 to +85°C	0 to +70°C

Note 2: The input offset characteristics given are the values required to drive the output to within 1 V of either supply with a 1-mA load. These characteristics define an error band which takes into account the worst-case effects of voltage gain and input impedance. The input offset voltage, input offset current, and input bias current specifications apply for any supply voltage from a 5 V single supply up to a ±15 V dual supply.

TYPICAL CHARACTERISTICS – ALL TYPES

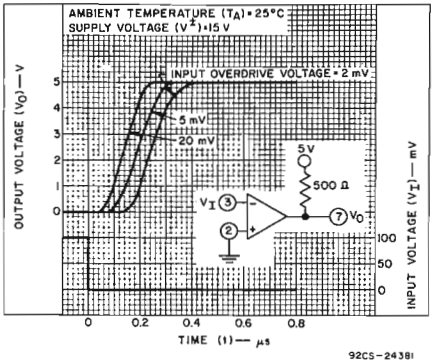


Fig. 1—Response time for various input overdrive voltages—positive input.

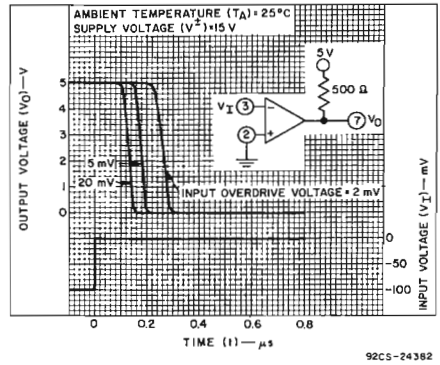


Fig. 2—Response time for various input overdrive voltages—negative input.

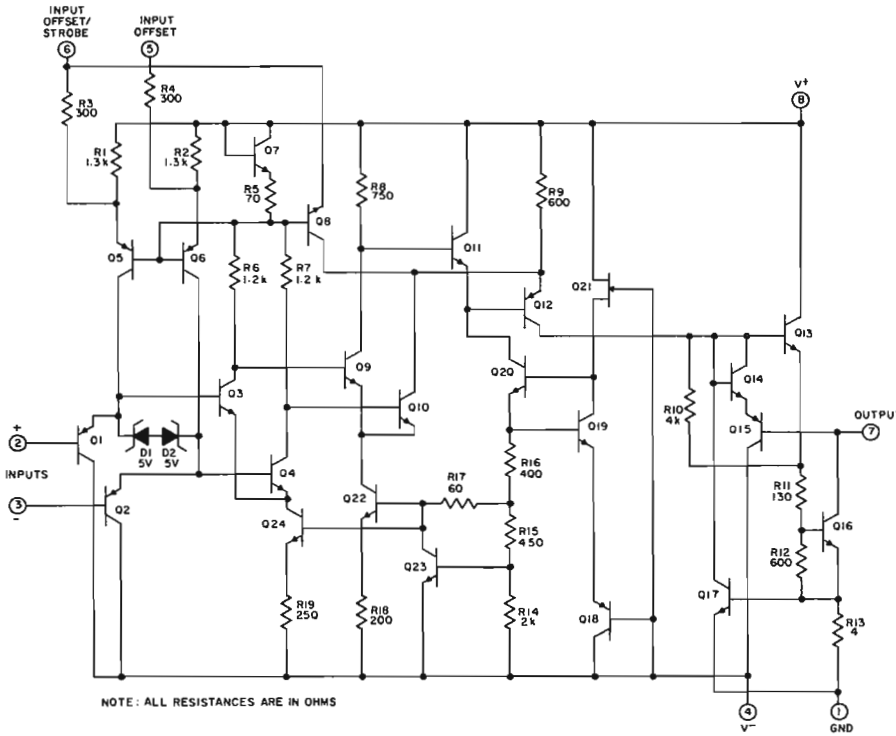


Fig. 3—Schematic diagram for CA111, CA211, and CA311.

TYPICAL CHARACTERISTICS – ALL TYPES (CONT'D)

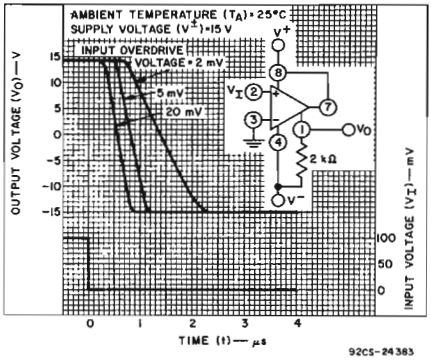


Fig. 4—Response time for various input overdrive voltages—positive input.

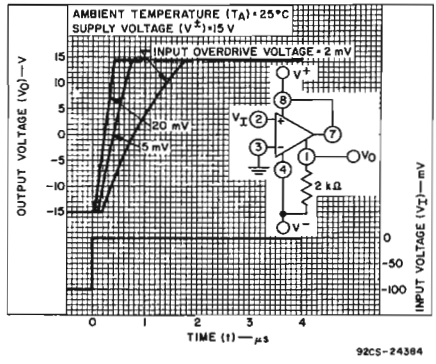


Fig. 5—Response time for various input overdrive voltages—negative input.

TYPICAL CHARACTERISTICS – ALL TYPES (CONT'D)

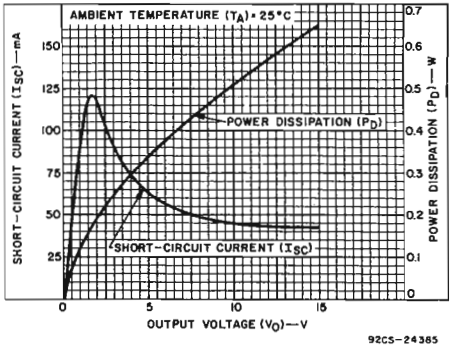


Fig. 6—Ouptut limiting characteristics.

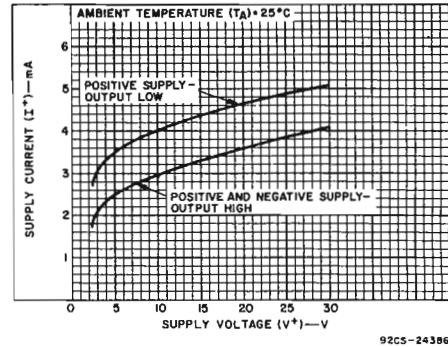


Fig. 7—Supply current vs. supply voltage.

TYPICAL CHARACTERISTICS – CA111, CA211

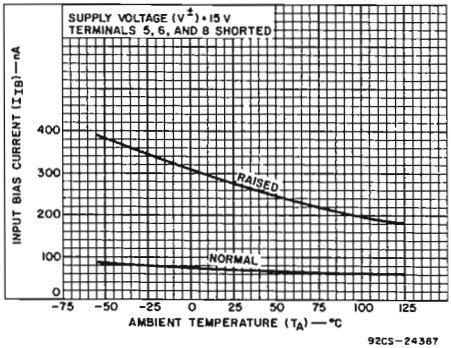


Fig. 8—Input bias current vs. ambient temperature.

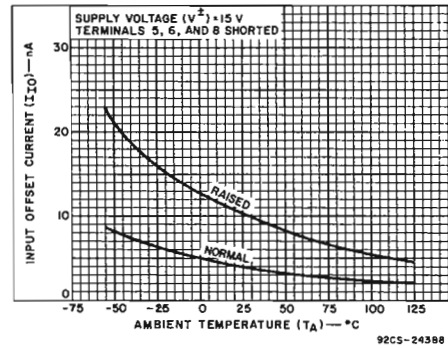


Fig. 9—Input offset current vs. ambiant temperature.

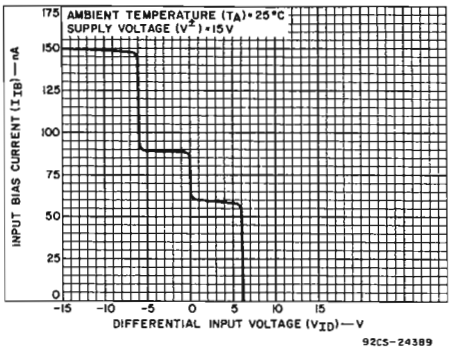


Fig. 10—Input characteristics.

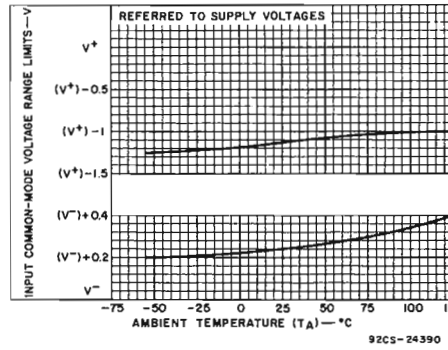


Fig. 11—Common-mode voltage range limits vs. ambient temperature.

TYPICAL CHARACTERISTICS – CA111, CA211 (CONT'D)

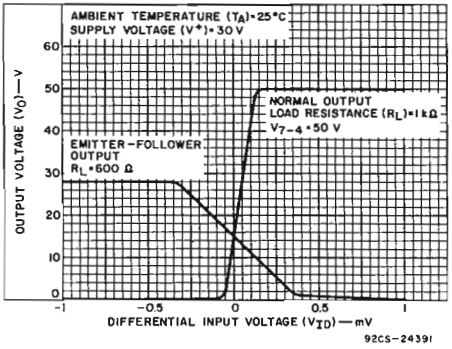


Fig. 12—Transfer function.

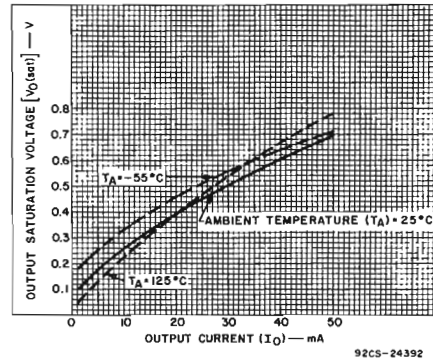


Fig. 13—Output saturation voltage vs. output current.

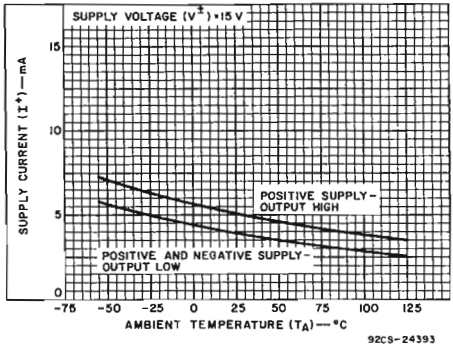


Fig. 14—Supply current vs. ambient temperature.

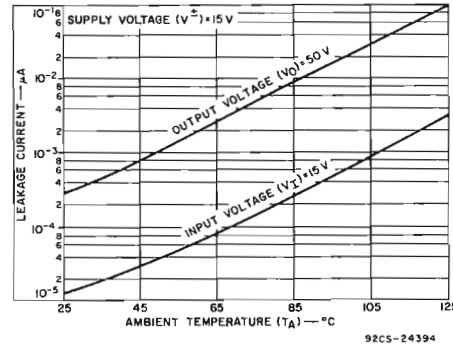


Fig. 15—Input and output leakage current vs. ambient temperature.

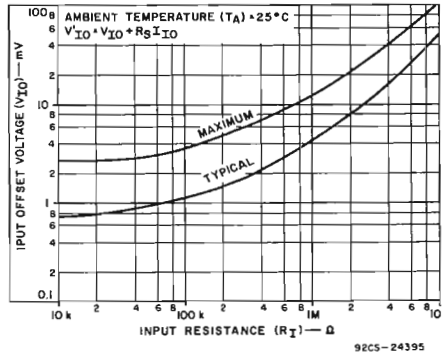


Fig. 16—Offset error.

TYPICAL CHARACTERISTICS – CA311

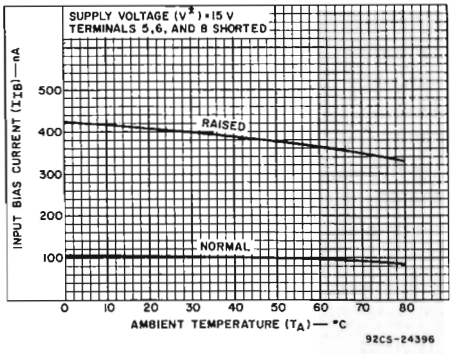


Fig. 17—Input bias current vs. ambient temperature.

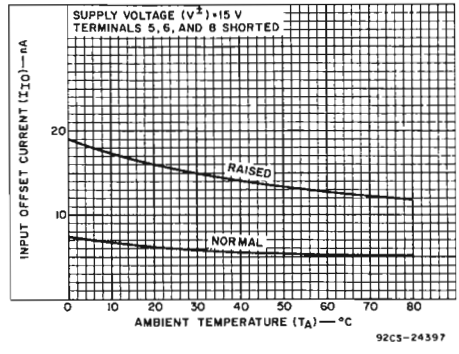


Fig. 18—Input offset current vs. ambient temperature.

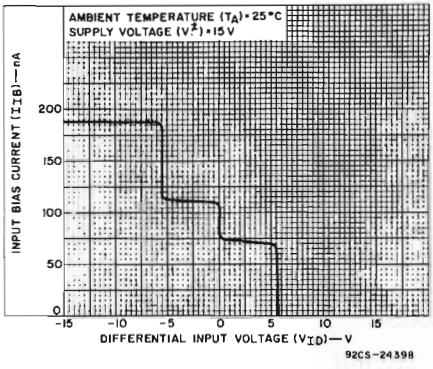


Fig. 19—Input characteristics.

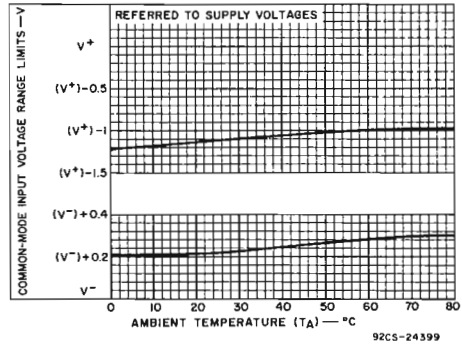


Fig. 20—Common-mode voltage range limits vs. ambient temperature.

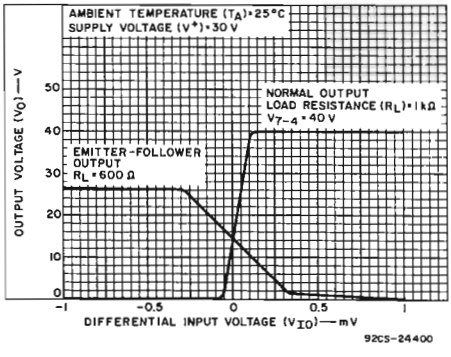


Fig. 21—Transfer function.

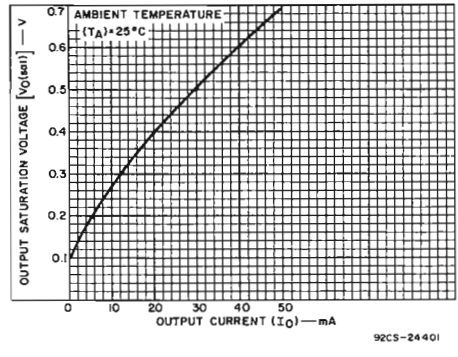


Fig. 22—Output saturation voltage vs. output current.

TYPICAL CHARACTERISTICS – CA311 (CONT'D)

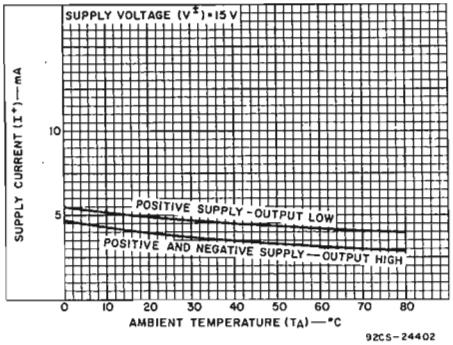


Fig. 23–Supply current vs. ambient temperature.

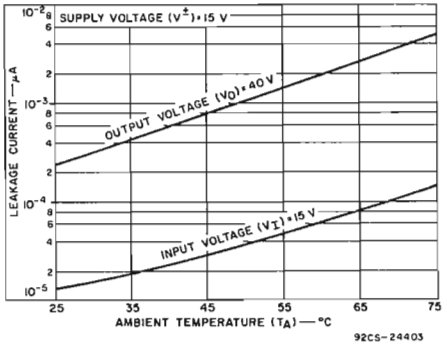


Fig. 24–Input and output leakage current vs. ambient temperature.

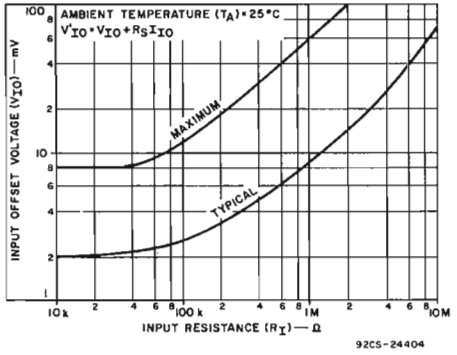


Fig. 25–Offset error.

TYPICAL APPLICATIONS

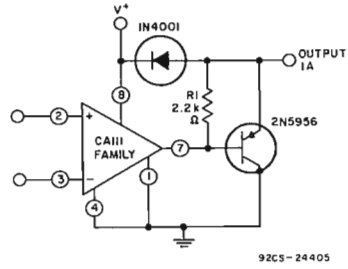


Fig. 26–Comparator and solesnoid driver.

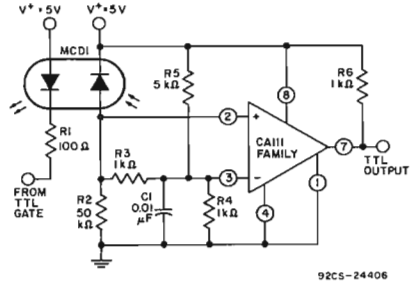


Fig. 27–Digital transmission isolator.

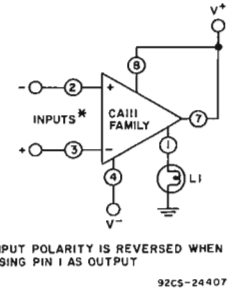


Fig. 28–Driving a ground-referred load.

TYPICAL APPLICATIONS (CONT'D)

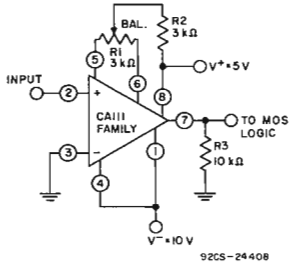


Fig. 29—Zero-crossing detector driving MOS logic.

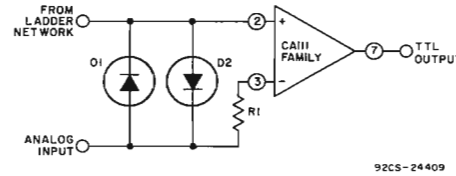


Fig. 30—Using clamp diodes to improve response.

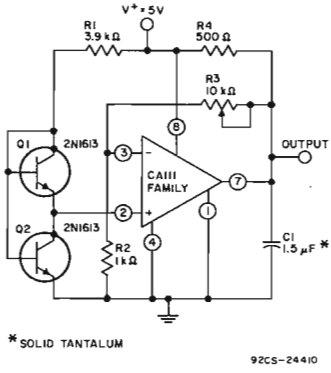


Fig. 31—Low-voltage adjustable-reference supply.

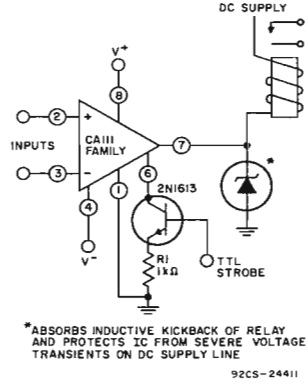


Fig. 32—Relay driver with strobe.

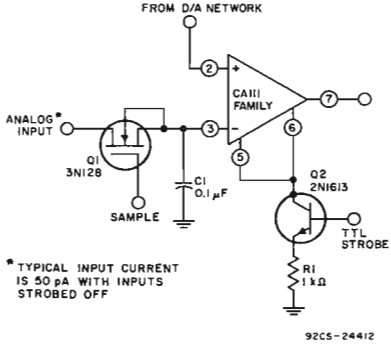


Fig. 33—Strobing off both input and output stages.

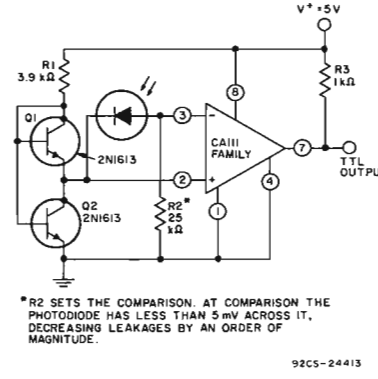


Fig. 34—Precision photodiode comparator.

TYPICAL APPLICATIONS (CONT'D)

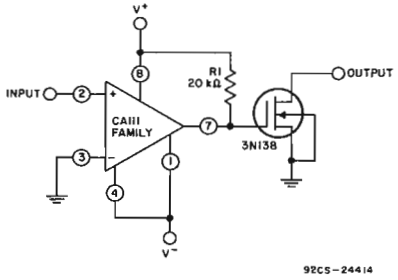


Fig. 35—Zero-crossing detector driving an MOS switch.

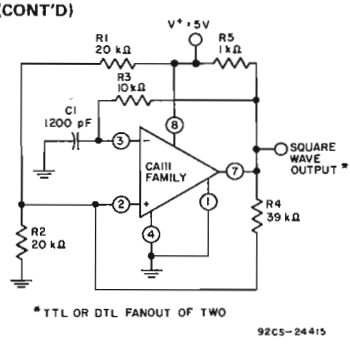


Fig. 36—100-kHz free-running multivibrator.

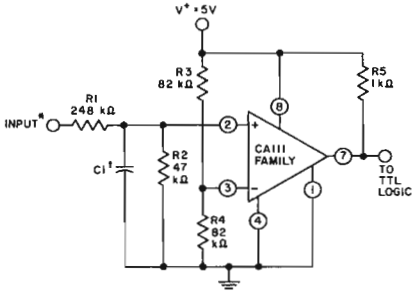


Fig. 37—TTL interface with high-level logic.

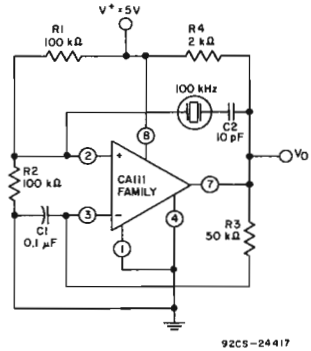


Fig. 38—Crystal oscillator.

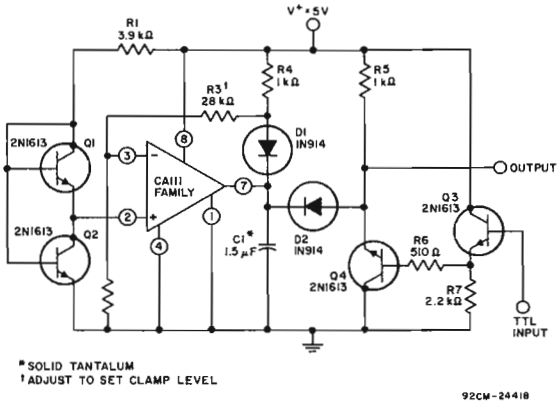


Fig. 39—Precision squarer.

TYPICAL APPLICATIONS (CONT'D)

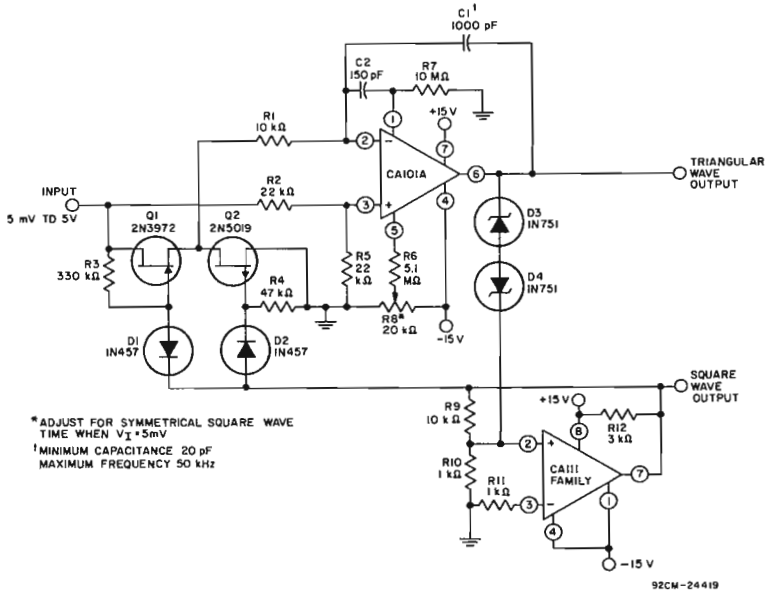


Fig. 40—10-Hz to 10-kHz voltage controlled oscillator.

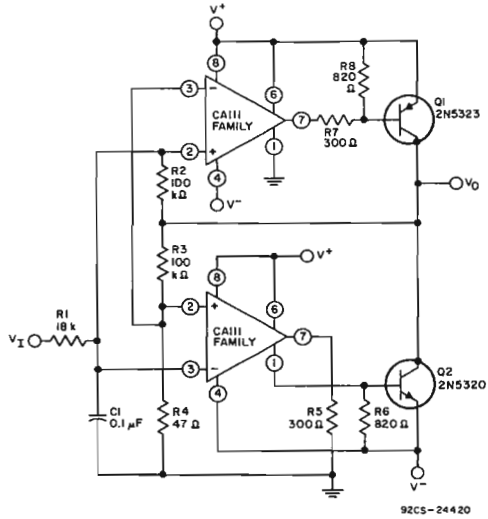


Fig. 41—Switching power amplifier.

TYPICAL APPLICATIONS (CONT'D)

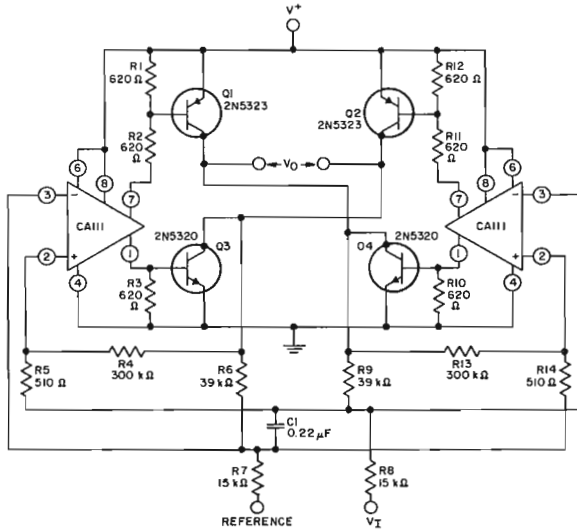


Fig. 42—Switching power amplifier.

92CS-24421

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA339E
CA339AE

14-Lead Dual-in-Line
Plastic Package

H-1517

Quad Voltage Comparators

For Industrial and Commercial Applications

Features:

- Operation from single or dual supplies
- Common-mode input-voltage range to ground
- Output voltage compatible with TTL, DTL, ECL, MOS, and CMOS
- Differential input-voltage range equal to the supply voltage
- Maximum input offset voltage:
  CA339A -- 2 mV
  CA339 -- 5 mV

The RCA-CA339E and CA339AE types consist of four independent single- or dual-supply voltage comparators on a single monolithic substrate. The common-mode input-voltage range includes ground even when operated from a single supply, and the low power-supply current drain makes these comparators suitable for battery operation. These types are designed to interface directly with TTL and CMOS.

The CA339AE has all the features and characteristics of the CA339E plus an even lower input-offset-voltage characteristic. They are supplied in the 14-lead dual-in-line plastic package ("E" suffix) and are direct replacements for industry types 339 and 339A in similar packages. The CA339 is also available in chip form (CA339H).

Applications:

- Square-wave generators
- Time-delay generators
- Pulse generators
- Multivibrators
- High-voltage digital logic gates
- A/D converters
- MOS clock timers

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C:*

DC SUPPLY VOLTAGE	36 V or ± 18 V
DC DIFFERENTIAL INPUT VOLTAGE	±36 V
INPUT VOLTAGE	−0.3 V to + 36 V
INPUT CURRENT (V_I <−0.3 V)*	50 mA
OUTPUT SHORT CIRCUIT TO GROUND▲	
(Single Supply)	Continuous
DEVICE DISSIPATION:	
Up to T_A = 25°C	570 mW
Above T_A = 25°C	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55°C to +125°C
Storage	−65 to +150 °C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C

* Inputs must not go more negative than −0.3 V.

▲ Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current independent of V^+ is approximataly 20 mA.

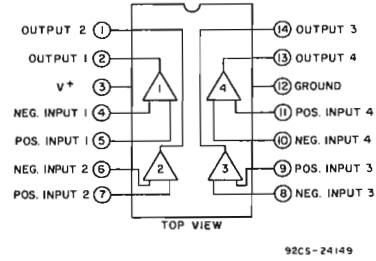


Fig. 1 — Functional diagram.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS ($V^+ = 5$ V, Unless otherwise indicated)		LIMITS CA339 CA339A MIN.	TYP.	MAX.	UNITS
Input Offset Voltage: CA339	V_{IO}	At Output Switch Point $V \cong 1.4$ V, $V_{REF} = 1.4$ V $R_S = 0$	25°C	–	2	5	mV
			0 to 70 °C	–	–	9	
CA339A			25°C	–	1	2	
			0 to 70 °C	–	–	4	
Differential Input Voltage	V_{ID}	Keep all inputs ≥ 0 V for V− (If Used), TA = 0 to 70°C, NOTE 1		–	–	36	V
Saturation Voltage	V_{SAT}	$V_I^- = 1$ V, $V_I^+ = 0$ V, $I_{SINK} \leq 4$ mA	25°C	–	250	500	mV
			0 to 70 °C	–	–	700	
Common-Mode Input Voltage Range	V_{ICR}	NOTE 2	25°C	0	–	$(V^+) - 1.5$	V
			0 to 70 °C	0	–	$(V^+) - 2$	
Input Offset Current	I_{IO}	$I_I^+ - I_I^-$	25°C	–	5	50	nA
			0 to 70 °C	–	–	150	
Input Bias Current	I_{IB}	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	250	nA
			0 to 70 °C	–	–	400	
Supply Current	I^+	$R_L = \infty$ on all comparators, $T_A = 25°C$		–	0.8	2	mA
Output Leakage Current		$V_I^+ \geq 1$ V, $V_I^- = 0$, $V_O = 5$ V	25°C	–	0.1	–	nA
		$V_I^+ \geq 1$ V, $V_I^- = 0$ $V_O = 30$ V	0 to 70 °C	–	–	1	μA
Output Sink Current		$V_I^- \geq 1$ V, $V_I^+ = 0$, $V_O \leq 1.5$ V, $T_A = 25°C$		6	16	–	mA
Voltage Gain CA339E	A	$R_L \geq 15$ kΩ, $T_A = 25°C$		–	200	–	V/mV
CA339AE		$R_L \geq 15$ kΩ, $T_A = 25°C$		50	200	–	V/mV
Large Signal Response Time		V_I = TTL Logic Swing $V_{REF} = +1.4$ V, $V_{RL} = 50$ V, $R_L = 5.1$ kΩ, $T_A = 25°C$		–	300	–	ns
Response Time		$V_{RL} = 5$ V, $R_L = 5.1$ kΩ, $T_A = 25°C$, See Figs. 5 & 6		–	1.3	–	μs

NOTE 1: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than −0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

NOTE 2: The upper end of the common-mode voltage range is $(V^+) - 1.5$ V, but either or both inputs can go to +30 V without damage.

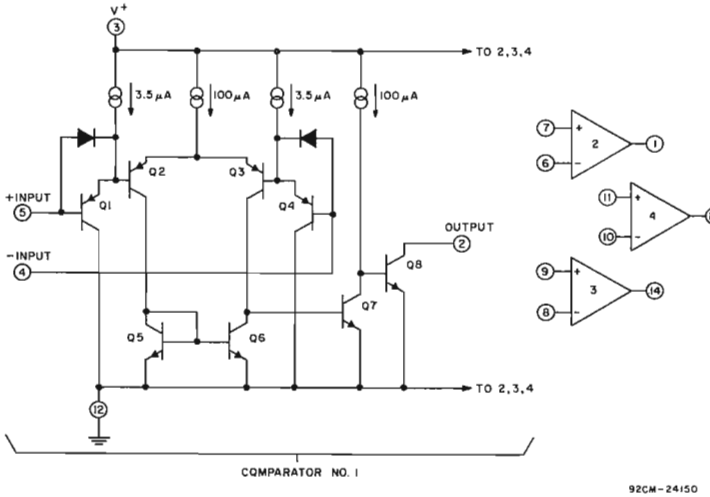


Fig.2 – Schematic diagram.

TYPICAL CHARACTERISTICS

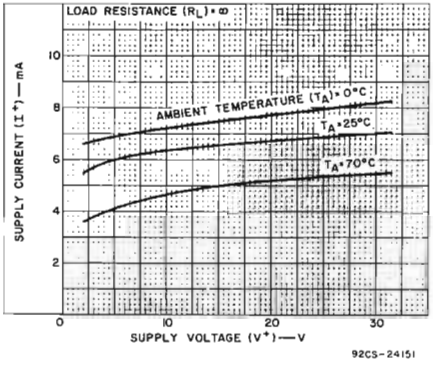


Fig.3 – Supply current vs. supply voltage.

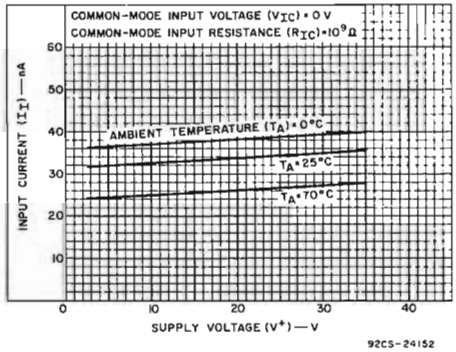


Fig.4 – Input current vs. supply voltage.

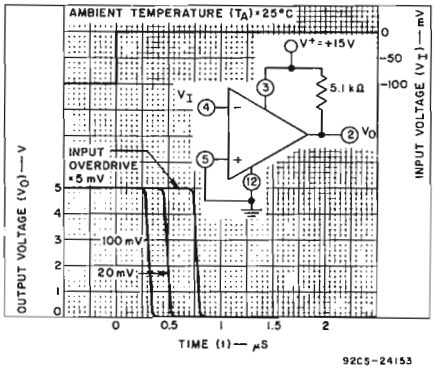


Fig.5 — Response time for various input overdrives — negative transition.

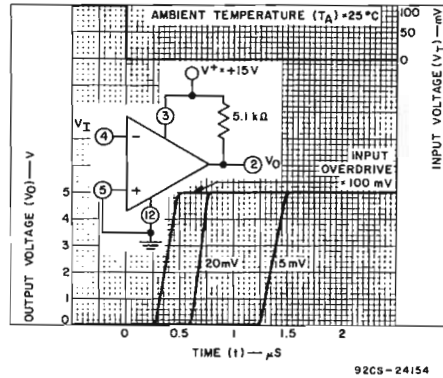


Fig.6 — Response time for various input overdrives — positive transition.

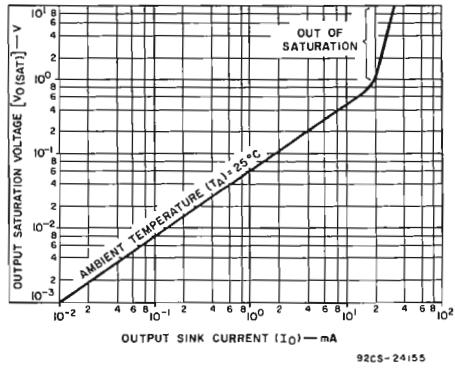


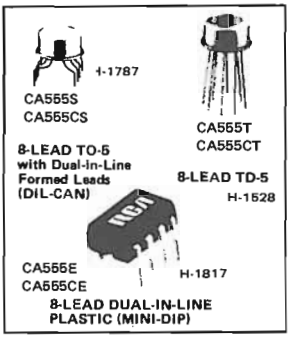
Fig.7 — Output saturation voltage vs. output sink current.

RCA
Solid State
Division

Linear integrated Circuits

Monolithic Silicon

CA555, CA555C



Timers

For Timing Delays &
Oscillator Application

Features:

- Accurate timing from microseconds through hours
- Astable and monostable operation
- Adjustable duty cycle
- Output capable of sourcing or sinking up to 200 mA
- Output capable of driving TTL devices
- Normally ON and OFF outputs
- High-temperature stability — 0.05%/°C
- Directly interchangeable with SE555, NE555, MC1555, and MC1455

The RCA-CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free-running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the waveform signal, and the output of these circuits can source or sink up to a 200-milliampere current or drive TTL circuits.

The CA555 and CA555C are supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead TO-5 style packages with dual-in-line formed leads ("DIL-CAN", S suffix), 8-lead dual-in-line plastic packages ("MINI-DIP", E suffix), and in chip form (H suffix). These types are direct replacements for industry types in packages with similar terminal arrangements (e.g. SE555 and NE555, MC1555 and MC1455, respectively).

Applications:

- Precision timing
- Sequential timing
- Time-delay generation
- Pulse generation
- Pulse-width and -position modulation
- Pulse detector

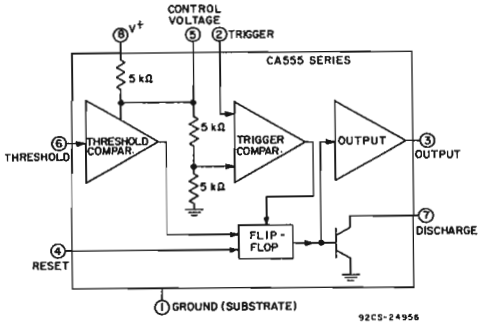


Fig. 1 – Functional diagram of the CA555 series.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

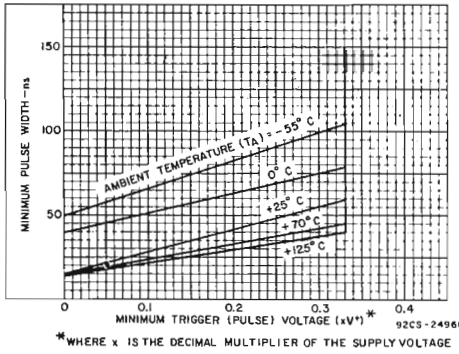
DC SUPPLY VOLTAGE	18	V
DEVICE DISSIPATION:		
Up to T_A = 55°C	600	mW
Above T_A = 55°C .....Derate linearly	5	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16" ± 1/32" (1.59 ± 0.79) from case for 10 seconds max.	+265	°C

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C, V^+ = 5 to 15 V unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS						UNITS
				CA555			CA555C			
				Min.	Typ.	Max.	Min.	Typ.	Max.	
DC Supply Voltage	V^+			4.5	–	18	4.5	–	16	V
DC Supply Current (Low State)*	I^+	V^+ = 5 V, R_L = ∞		–	3	5	–	3	6	mA
		V^+ = 15 V, R_L = ∞		–	10	12	–	10	15	
Threshold Voltage	V_{TH}			–	(2/3)V^+	–	–	(2/3)V^+	–	V
Trigger Voltage		V^+ = 5 V		1.45	1.67	1.9	–	1.67	–	V
		V^+ = 15 V		4.8	5	5.2	–	5	–	
Trigger Current				–	0.5	–	–	0.5	–	μA
Threshold Current▲	I_{TH}			–	0.1	0.25	–	0.1	0.25	μA
Reset Voltage				0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current				–	0.1	–	–	0.1	–	mA
Control Voltage Level		V^+ = 5 V		2.9	3.33	3.8	2.6	3.33	4	V
		V^+ = 15 V		9.6	10	10.4	9	10	11	
Output Voltage Drop: Low State	V_{OL}	V^+ = 5 V	I_{SINK} = 5 mA	–	–	–	–	0.25	0.35	V
			I_{SINK} = 8 mA	–	0.1	0.25	–	–	–	
		V^+ = 15 V	I_{SINK} = 10 mA	–	0.1	0.15	–	0.1	0.25	V
			I_{SINK} = 50 mA	–	0.4	0.5	–	0.4	0.75	
			I_{SINK} = 100 mA	–	2.0	2.2	–	2.0	2.5	
			I_{SINK} = 200 mA	–	2.5	–	–	2.5	–	
High State	V_{OH}	V^+ = 5 V	I_{SOURCE} = 100 mA	3.0	3.3	–	2.75	3.3	–	V
		V^+ = 15 V	I_{SOURCE} = 100 mA	13.0	13.3	–	12.75	13.3	–	
			I_{SOURCE} = 200 mA	–	12.5	–	–	12.5	–	
Timing Error (Monostable): Initial Accuracy		R_A, R_B = 1 to 100 kΩ		–	0.5	2	–	1	–	%
Frequency Drift with Temperature		C = 0.1 μF		–	30	100	–	50	–	p/m/°C
Drift with Supply Voltage		Tested at V^+ = 5 V and V^+ = 15 V		–	0.05	0.2	–	0.1	–	%/V
Output Rise Time	t_r			–	100	–	–	100	–	ns
Output Fall Time	t_f			–	100	–	–	100	–	ns

* When the output is in a high state, the dc supply current is typically 1 mA less than the low-state value.

▲ The threshold current will determine the sum of the values of R_A and R_B to be used in Fig. 6 (astable operation); the maximum total $R_A + R_B$ = 20 MΩ.



*WHERE x IS THE DECIMAL MULTIPLIER OF THE SUPPLY VOLTAGE

Fig. 2 – Minimum pulse width vs. minimum trigger voltage.

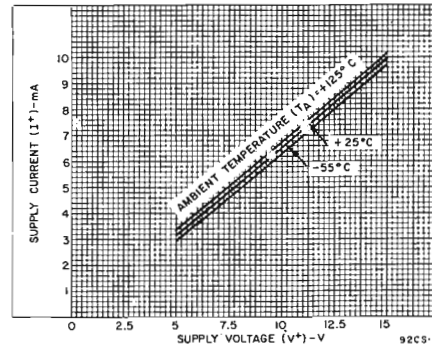


Fig. 3 – Supply current vs. supply voltage.

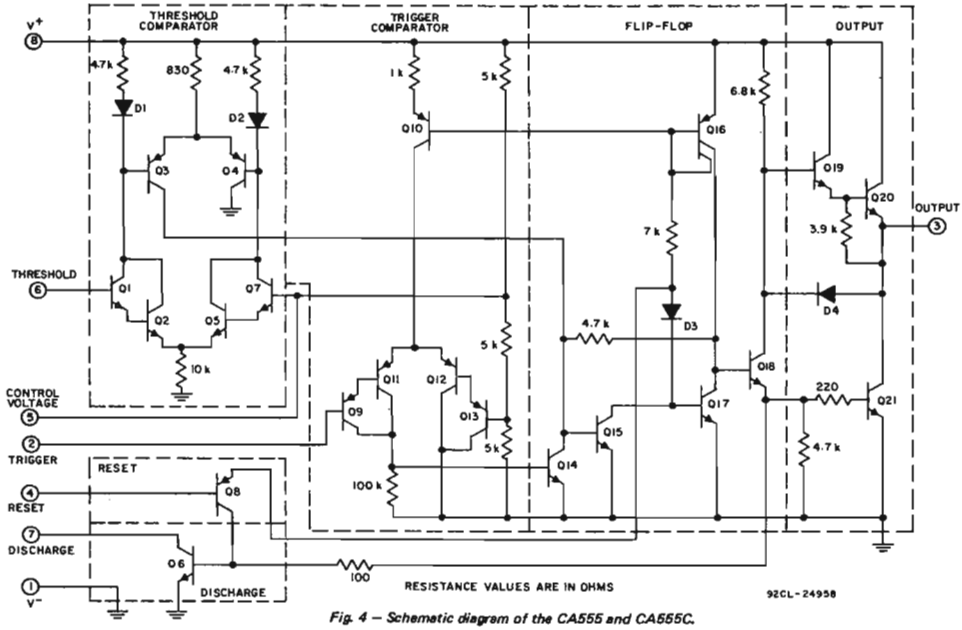
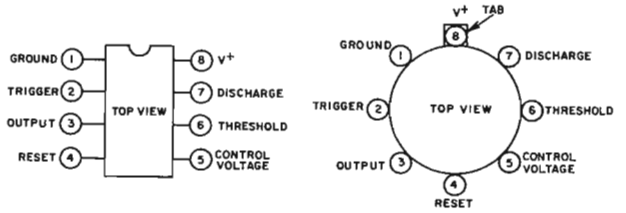


Fig. 4 — Schematic diagram of the CA555 and CA555C.



a. MINI-DIP plastic package **b. TO-5 style package**

Fig. 5 — Terminal assignment diagrams.

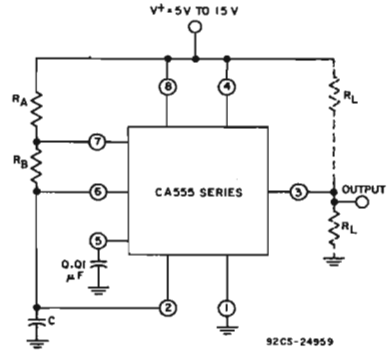


Fig. 6 — Astable oscillator circuit.

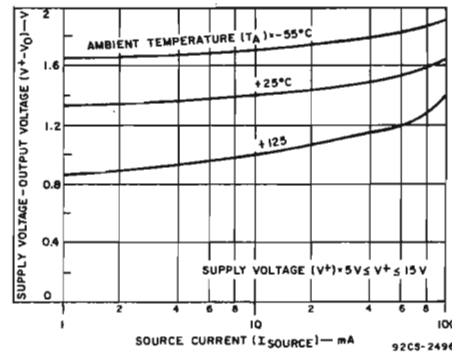


Fig. 7 — Output voltage drop (high state) vs. source current.

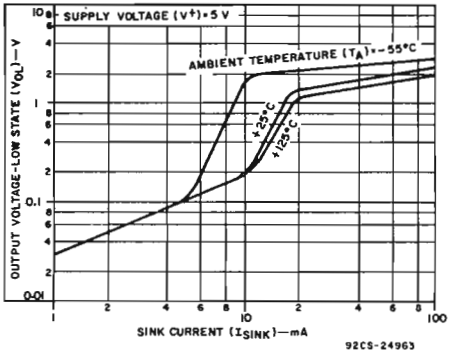


Fig. 8 — Output voltage-low state vs. sink current at $V^+ = 5$ V.

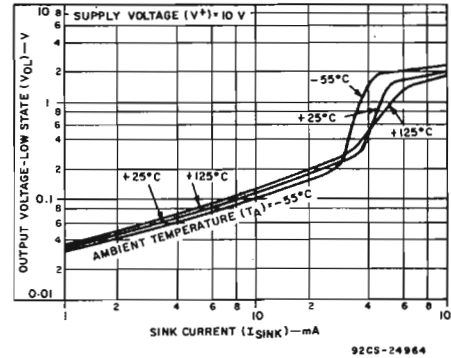


Fig. 9 — Output voltage-low state vs. current at $V^+ = 10$ V.

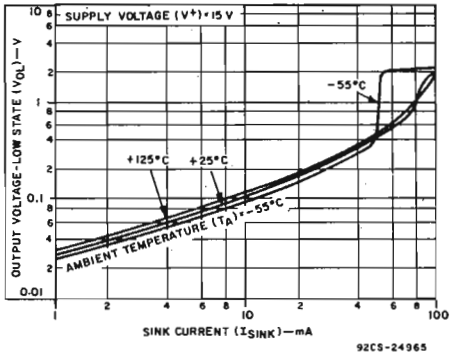


Fig. 10 — Output voltage-low state vs. sink current at $V^+ = 15$ V.

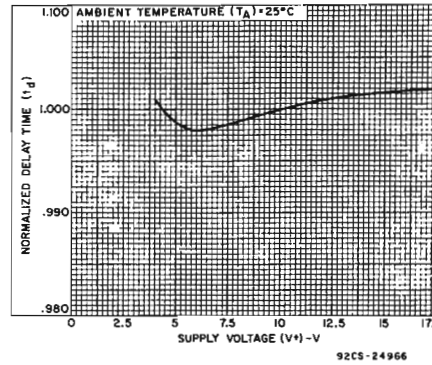


Fig. 11 — Delay time vs. supply voltage.

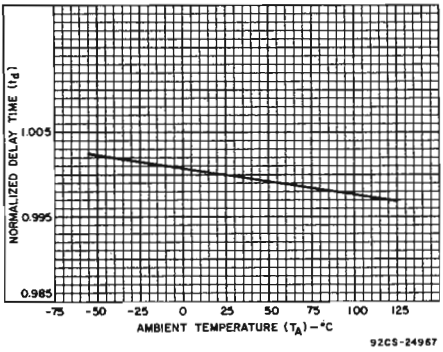


Fig. 12 — Delay time vs. temperature.

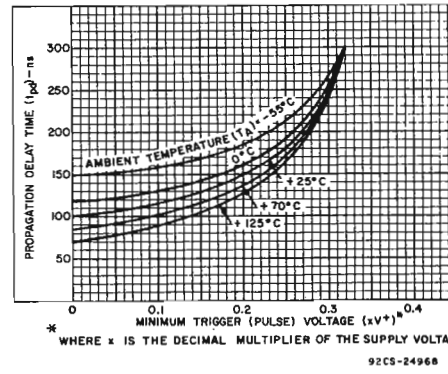


Fig. 13 — Propagation delay time vs. trigger voltage.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA723T, CA723CT
CA723E, CA723CE

"T" Suffix

10-Lead TO-5 H-1384

"E" Suffix

14-Lead Dual-In-Line Plastic Package H-1517

Voltage Regulators

For Regulated Output Voltages Adjustable from 2 V to 37 V at Currents up to 150 mA Without External Pass Transistors

Features:

- Up to 150 mA output current
- Positive and negative voltage regulation
- Regulation in excess of 10 A with suitable pass transistors
- Input and output short-circuit protection
- Load and line regulation: 0.03%
- Direct replacement for 723 and 723C industry types
- Adjustable output voltage: 2 to 37 V

RCA-CA723 and CA723C are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2 to 37 volts at currents up to 150 milliamperes.

Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150 milliamperes and in excess of 10 amperes with the use of suitable n-p-n or p-n-p external pass transistors.

The CA723 and CA723C are supplied in the 10-lead TO-5-style ceramic package (T suffix), and the 14-lead dual-in-line plastic package (E suffix), and are direct replacements for industry types 723, 723C, μA723, and μA723C in packages with similar terminal arrangements. They are also available in chip form ("H" suffix).

All CA723-series circuits can be operated over the full military-temperature range of −55°C to +125°C. Refer to the chart of Electrical Characteristics for characteristics limits over several temperature ranges.

Applications

- Series and shunt voltage regulator
- Floating regulator
- Switching voltage regulator
- High-current voltage regulator
- Temperature controller

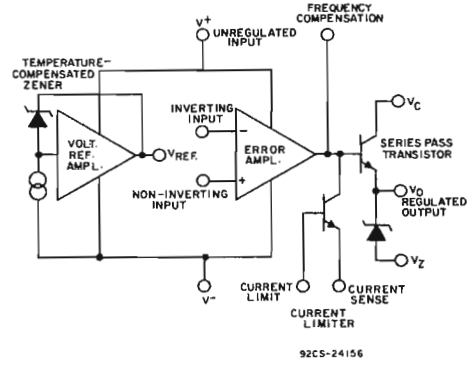


Fig. 1 — Functional diagram of the CA723 and CA723C.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals)	40	V
PULSE VOLTAGE FOR 50-ms PULSE WIDTH (Between V^+ and V^- Terminals)	50	V
DIFFERENTIAL INPUT-OUTPUT VOLTAGE	40	V
DIFFERENTIAL INPUT VOLTAGE:		
Between Inverting and Non-Inverting Inputs	±5	V
Between Non-Inverting Input and V^-	8	V
CURRENT FROM ZENER DIODE TERMINAL (V_Z)	25	mA
CURRENT FROM VOLTAGE REFERENCE TERMINAL (V_{REF})	15	mA

DEVICE DISSIPATION:

Up to $T_A = 25^oC$ –	
CA723T, CA723CT	800 mW
CA723E, CA723CE	1000 mW
Above $T_A = 25^oC$ –	
CA723T, CA723CT	Derate linearly 6.3 mW/°C
CA723E, CA723CE	Derate linearly 8.3 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	–55 to +125 °C
Storage	–65 to +150 °C
LEAD TEMPERATURE (During Soldering):	
At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C

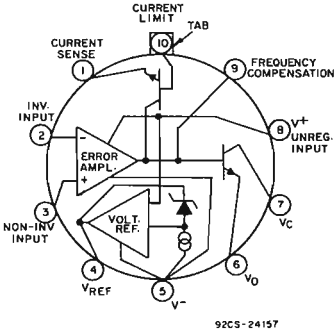


Fig.2 – Terminal arrangement of the CA723T and CA723CT in the TO-5 style package.

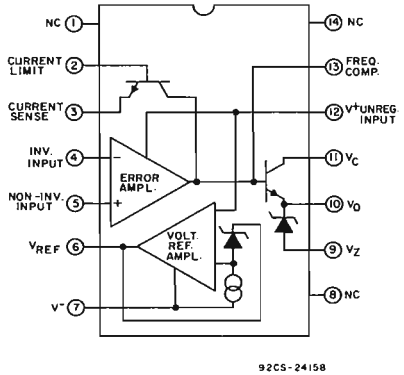


Fig.3 – Terminal arrangement of the CA723E and CA723CE in the dual-in-line plastic package.

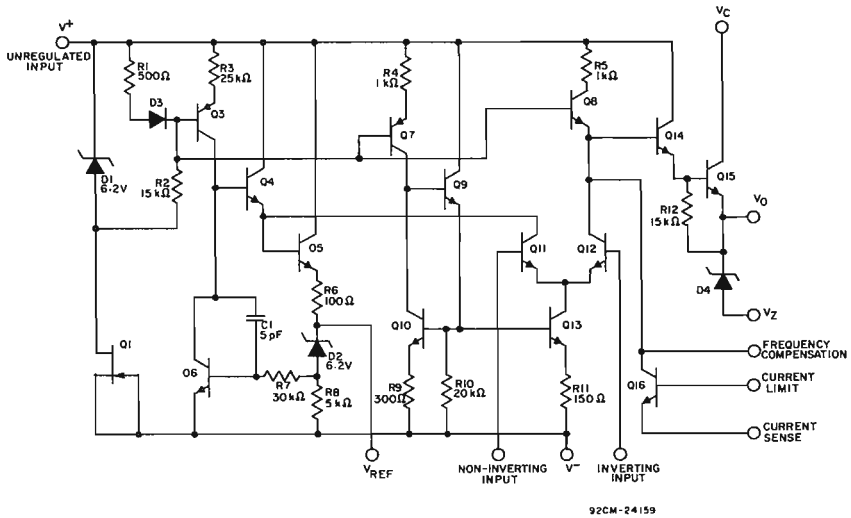


Fig.4 – Equivalent schematic diagram of the CA723 and CA723C.

ELECTRICAL CHARACTERISTICS:

CHARACTERISTIC	SYMBOL	TEST CONDITIONS (See Note)	CA723			CA723C			UNIT
		T_A=25°C, V_I=V^+=V_C=12 V, V^-=0, V_O=5 V, I_L=1 mA, C_I=100 pF, $Z_{DIVIDER}$ ≤ 10 kΩ (into error amplifier as shown in Fig.23) unless otherwise indicated	Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Regulator Current	I_Q	I_L=0, V_I=30 V	–	2.3	3.5	–	2.3	4.0	mA
Input Voltage Range	V_I		9.5	–	40	9.5	–	40	V
Output Voltage Range	V_O		2.0	–	37	2.0	–	37	V
Differential Input-Output Voltage	V_I–V_O		3.0	–	38	3.0	–	38	V
Reference Voltage	V_{REF}		6.95	7.15	7.35	6.80	7.15	7.50	V
Line Regulation		V_I=12 to 40 V	–	0.02	0.2	–	0.1	0.5	%V_O
		V_I=12 to 15 V	–	0.01	0.1	–	0.01	0.1	
		V_I=12 to 15 V, T_A=–55 to +125°C	–	–	0.3	–	–	–	
		V_I=12 to 15 V, T_A=0 to 70°C	–	–	–	–	–	0.3	
Load Regulation		I_L=1 to 50 mA	–	0.03	0.15	–	0.03	0.2	%V_O
		I_L=1 to 50 mA, T_A=–55 to +125°C	–	–	0.6	–	–	–	
		I_L=1 to 50 mA, T_A=0 to 70°C	–	–	–	–	–	0.6	
Output-Voltage Temperature Coefficient	ΔV_O	T_A=–55 to +125°C	–	0.002	0.015	–	–	–	%/°C
		T_A=0 to 70°C	–	–	–	–	0.003	0.015	
Ripple Rejection		f=50 Hz to 10 kHz	–	74	–	–	74	–	dB
		f=50 Hz to 10 kHz, C_{REF}=5 μF	–	86	–	–	86	–	
Short-Circuit Limiting Current	I_{LIM}	R_{SCP}=10 Ω, V_O=0	–	65	–	–	65	–	mA
Equivalent Noise Output Voltage	V_{NOISE}	BW=100 to 10 kHz, C_{REF}=0	–	20	–	–	20	–	μV_{RMS}
		BW=100 to 10 kHz, C_{REF}=5 μF	–	2.5	–	–	2.5	–	

Note: Line and load regulation specifications are given for condition of a constant chip temperature; for high dissipation conditions, temperature drifts must be separately taken into account.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723

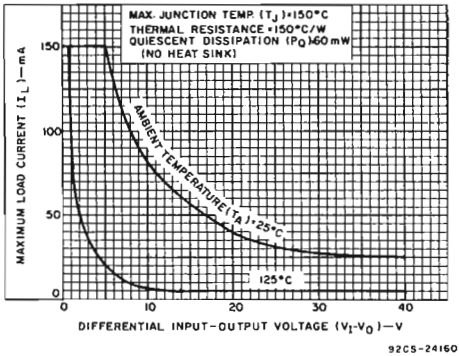


Fig.5 — Max. load current vs differential input-output voltage.

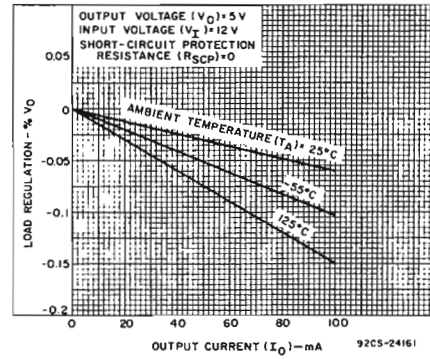


Fig.6 — Load regulation without current limiting.

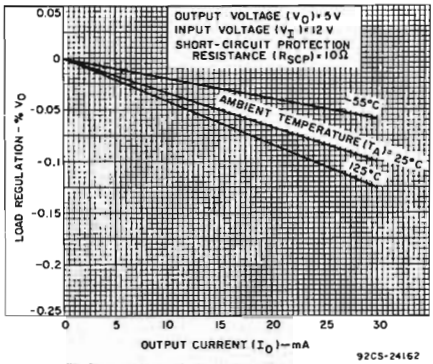


Fig.7 — Load regulation with current limiting.

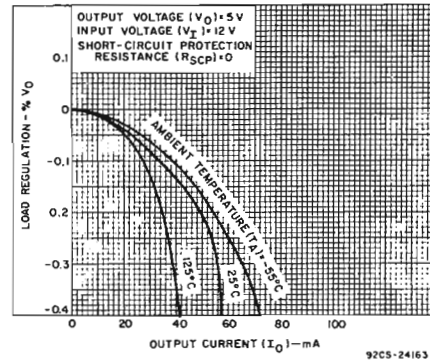


Fig.8 — Load regulation with current limiting.

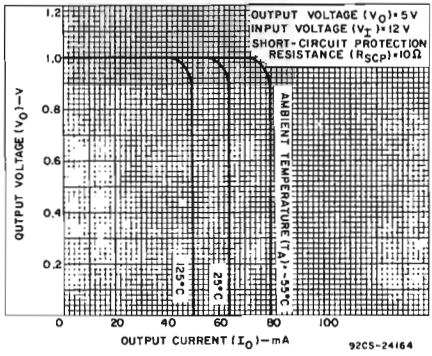


Fig.9 — Current limiting characteristics.

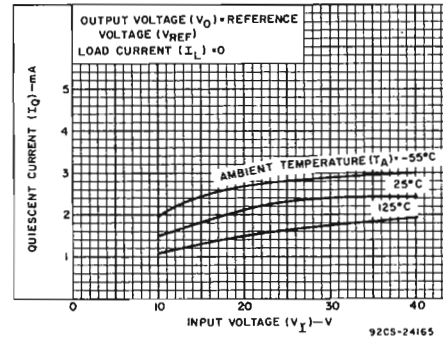


Fig.10 — Quiescent current vs. input voltage.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723C

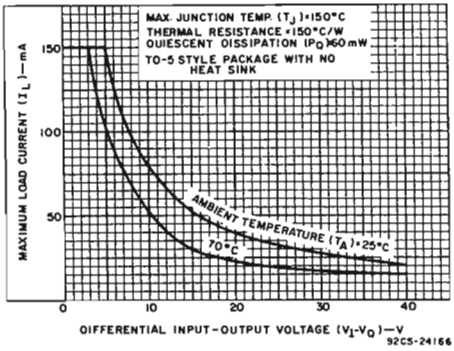


Fig. 11 — Max. load current vs differential input-output voltage for CA723CT.

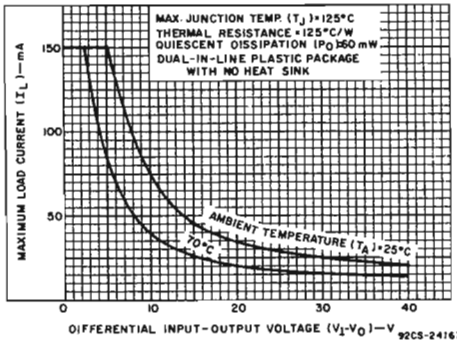


Fig. 12 — Max. load current vs differential input-output voltage for CA723CE.

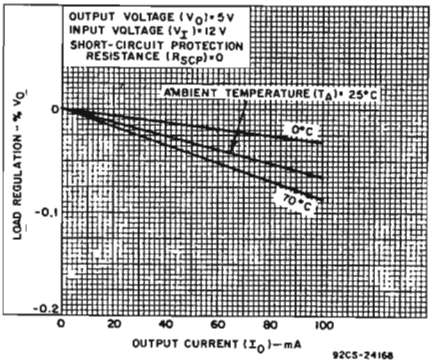


Fig. 13 — Load regulation without current limiting.

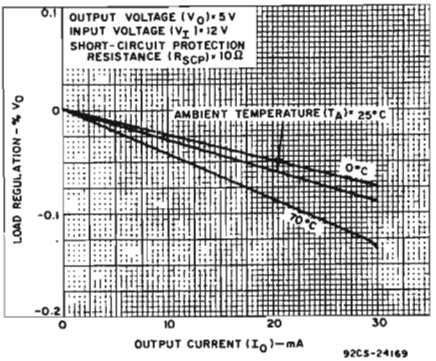


Fig. 14 — Load regulation with current limiting.

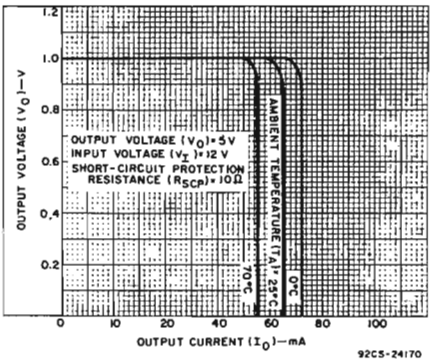


Fig. 15 — Current limiting characteristics.

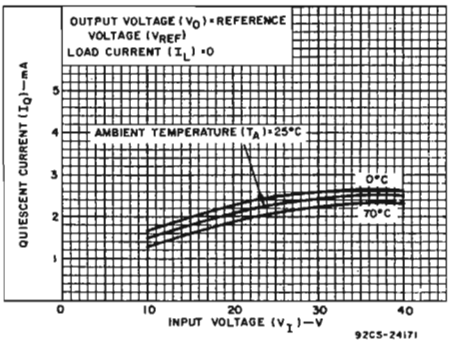


Fig. 16 — Quiescent current vs. input voltage.

TYPICAL CHARACTERISTICS CURVES FOR TYPES CA723 AND CA723C

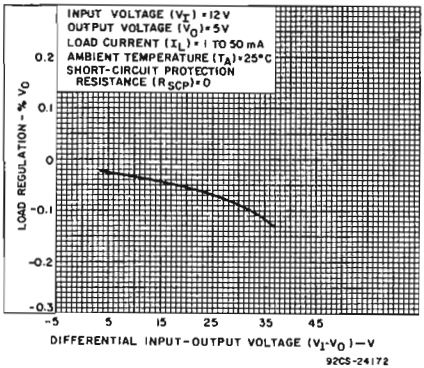


Fig.17 — Load regulation vs. differential input-output voltage.

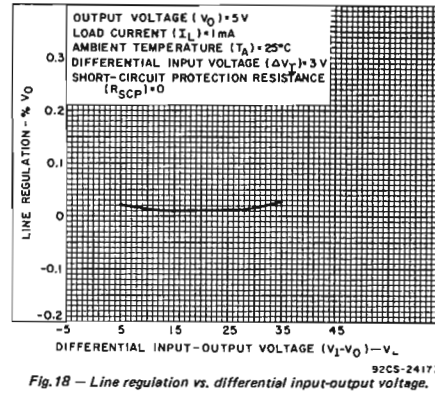


Fig.18 — Line regulation vs. differential input-output voltage.

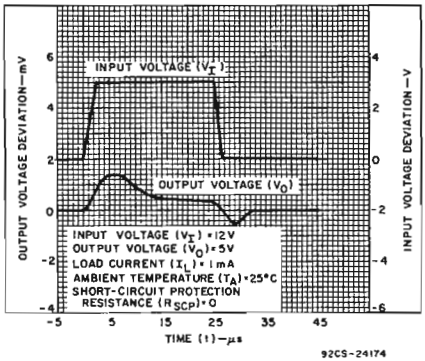


Fig.19 — Line transient response.

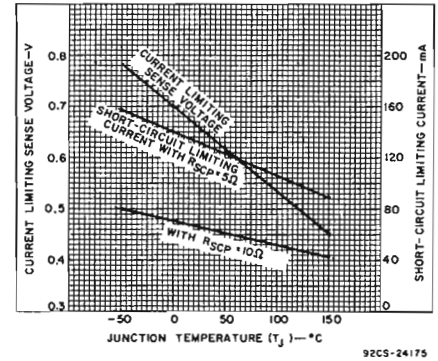


Fig.20 — Current limiting characteristics vs. junction temperature.

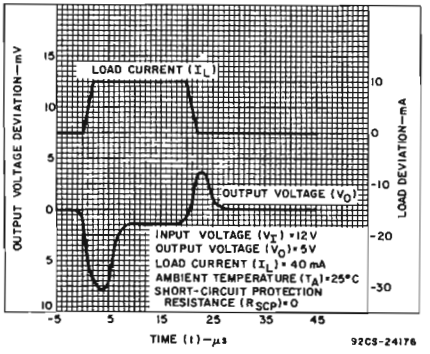


Fig.21 — Load transient response.

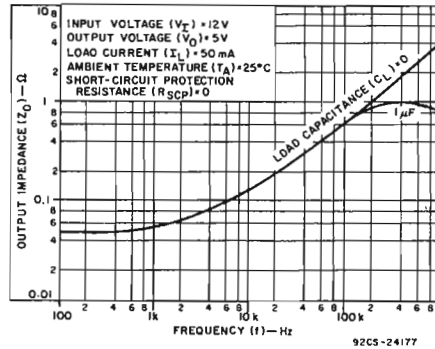
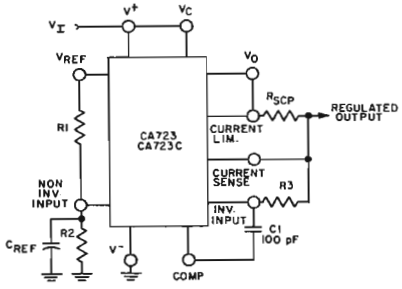


Fig.22 — Output impedance vs. frequency.

TYPICAL APPLICATION CIRCUITS

Voltage-Resistance Chart and Equations for the following Circuits are shown on pages 9 and 10.



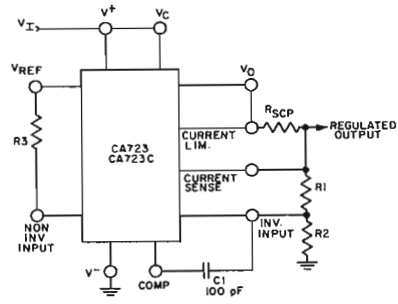
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE . . .	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 50 mA) . . .	1.5 mV

Note: $R3 = \frac{R1\ R2}{R1+R2}$ for minimum temperature drift

92C9-24178

Fig.23 – Low-voltage regulator circuit (V_O = 2 to 7 volts).



CIRCUIT PERFORMANCE DATA:

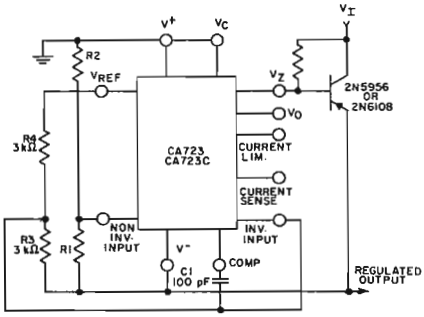
REGULATED OUTPUT VOLTAGE . . .	15 V
LINE REGULATION (ΔV_I = 3 V)	1.5 mV
LOAD REGULATION (ΔI_L = 50 mA) . .	4.5 mV

Note: $R3 = \frac{R1\ R2}{R1+R2}$ for minimum temperature drift

R3 may be eliminated for minimum component count.

92CS-24179

Fig.24 – High-voltage regulator circuit (V_O = 7 to 37 volts).



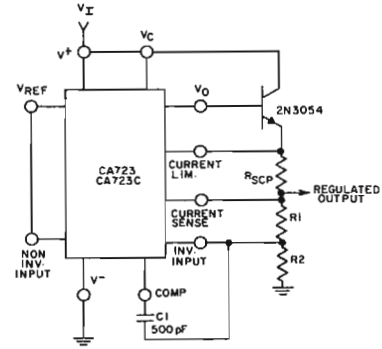
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE . . .	−15 V
LINE REGULATION (ΔV_I = 3 V)	1 mV
LOAD REGULATION (ΔI_L = 100 mA) . .	2 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24180

Fig.26 – Negative-voltage-regulator circuit.



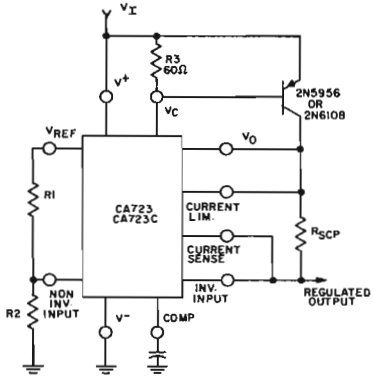
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE . . .	15 V
LINE REGULATION (ΔV_I = 3 V)	1.5 mV
LOAD REGULATION (ΔI_L = 1 A)	15 mV

92CS-24181

Fig.26 – Positive-voltage-regulator circuit (with external n-p-n pass transistor).

TYPICAL APPLICATION CIRCUITS (Cont'd)

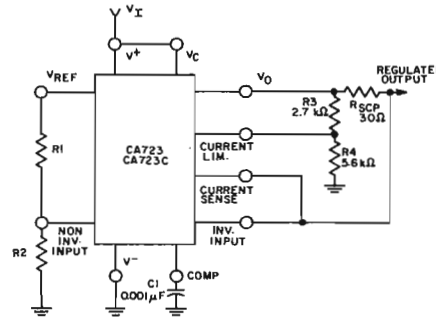


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5	V
LINE REGULATION (ΔV_I = 3 V)	0.5	mV
LOAD REGULATION (ΔI_L = 1 A)	5	mV

92CS-24182

Fig.27 — Positive voltage-regulator circuit (with external p-n-p pass transistor).

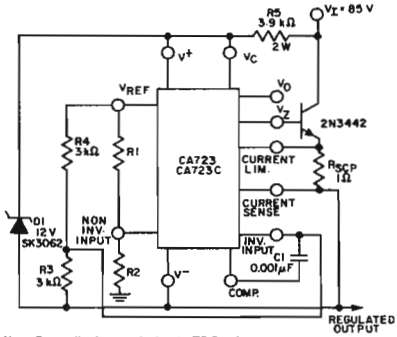


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5	V
LINE REGULATION (ΔV_I = 3 V)	0.5	mV
LOAD REGULATION (ΔI_L = 10 mA)	1	mV
SHORT-CIRCUIT CURRENT	20	mA

92CS-24183

Fig.28 — Foldback current-limiting circuit.



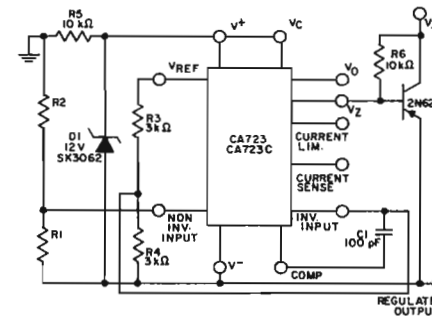
Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 8).

CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	50	V
LINE REGULATION (ΔV_I = 20 V)	15	mV
LOAD REGULATION (ΔI_L = 50 mA)	20	mV

92CS-24184

Fig.29 — Positive-floating regulator circuit.



CIRCUIT PERFORMANCE DATA:

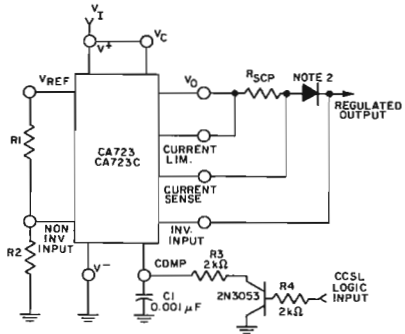
REGULATED OUTPUT VOLTAGE	−100	V
LINE REGULATION (ΔV_I = 20 V)	30	mV
LOAD REGULATION (ΔI_L = 100 mA)	20	mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24185

Fig.30 — Negative-floating regulator circuit.

TYPICAL APPLICATION CIRCUITS (Cont'd)



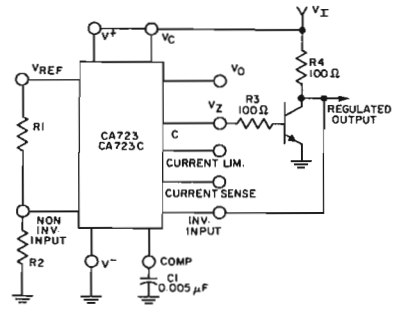
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE . . .	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 50 mA). . .	1.5 mV

Note 1: A current limiting transistor may be used for shutdown if current limiting is not required.
Note 2: Add a diode if $V_O > 10$ V.

92CS-24186

Fig.31 – Remote shutdown regulator circuit with current limiting.



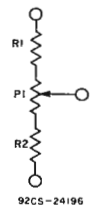
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE . . .	5 V
LINE REGULATION (ΔV_I = 10 V) . . .	0.5 mV
LOAD REGULATION (ΔI_L = 100 mA) . .	1.5 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24187

Fig.32 – Shunt regulator circuit.



92CS-24196

Fig.33 – Resistance network for adjustable output voltage.

EQUATIONS FOR DERIVING INTERMEDIATE OUTPUT VOLTAGES AND CURRENT LIMITING

1. Output Voltages from 2 to 7 Volts
   Use circuits with Fig. Nos. 21, 25, 26, 30, (24 – See Note 1)

$$V_O = V_{REF} \times \frac{R2}{R1+R2}$$

2. Output Voltages from 7 to 37 Volts
   Use circuits with Fig. Nos. 22, 24, (25, 26, 30 – See Note 1)

$$V_O = V_{REF} \times \frac{R1+R2}{R2}$$

3. Output Voltages from 4 to 250 Volts
   Use circuit with Fig. No. 27

$$V_O = \frac{V_{REF}}{2} \times \frac{R2-R1}{R1} \; ; \; R3 = R4$$

4. Output Voltages from −6 to −250 Volts
   Use circuits with Fig. Nos. 23 and 28

$$V_O = \frac{V_{REF}}{2} \times \frac{R1+R2}{R1} \; ; \; R3 = R4$$

5. Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{SCP}}$$

6. Foldback Current Limiting

$$I_{KNEE} = \frac{V_O R3}{R_{SCP} R4} + \frac{V_{SENSE}}{R_{SCP} R4}(R3+R4)$$

$$I_{SHORT\ CKT} = \frac{V_{SENSE}}{R_{SCP}} \times \frac{R3+R4}{R4}$$

RESISTANCE VALUES (Resistors R1, R2, and Potentiometer P1) FOR STANDARD OUTPUT VOLTAGES

Positive Output Voltage	Applicable Circuit Fig. No. (Note 1)	Fixed Output Resistance ±5%		Adjustable Output Resistance ±10% (Note 2)			Negative Output Voltage	Applicable Circuit Fig. No. (Note 1)	Fixed Output Resistance ±5%		5% Adjustable Output Resistance ±10%		
+V		R1 kΩ	R2 kΩ	R1 kΩ	R2 kΩ	P1 kΩ	−V		R1 kΩ	R2 kΩ	R1 kΩ	R2 kΩ	P1 kΩ
3.0	23, 27, 28 32, (26)	4.12	3.01	1.8	1.2	0.5							
3.6	23, 27, 28 32, (26)	3.57	3.65	1.5	1.5	0.5							
5.0	23, 27, 28, 32, (26)	2.15	4.99	0.75	2.2	0.5							
6.0	23, 27, 28, 32, (26)	1.15	6.04	0.5	2.7	0.5	−6.0 (Note 3)	25	3.57	2.43	1.2	0.75	0.5
9.0	24, 26 (27, 28, 32)	1.87	7.15	0.75	2.7	1.0	−9.0	25	3.48	5.36	1.2	2.0	0.5
12	24, 26, (27, 28, 32)	4.87	7.15	2.0	3.0	1.0	−12	25	3.57	8.45	1.2	3.3	0.5
15	24, 26, (27, 28, 32)	7.87	7.15	3.3	3.0	1.0	−15	25	3.65	11.5	1.2	4.3	0.5
28	24, 26, (27, 28, 32)	21.0	7.15	5.6	2.0	1.0	−28	25	3.57	24.3	1.2	10	0.5
45	29	3.57	48.7	2.2	39	10	−45	30	3.57	41.2	2.2	33	10
75	29	3.57	78.7	2.2	68	10							
100	29	3.57	102	2.2	91	10	−100	30	3.57	97.6	2.2	91	10
250	29	3.57	255	2.2	240	10	−250	30	3.57	249	2.2	240	10

Note 1 — Circuits whose Fig. Nos. are shown in parentheses may be used if divider network R1 — R2 is placed on opposite side of Error Amplifier.

Note 2 — Use the divider network shown in Fig. 31 in place of the R1 — R2 network.

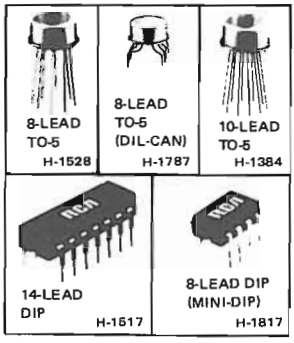
Note 3 — A supply voltage of 3 V or greater must be applied to V^+.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA741, CA741C, CA747, CA747C, CA748, CA748C, CA1458, CA1558 Types



Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers
For Military, Industrial and Commercial Applications

Applications:

- Comparator
- DC amplifier
- Integrator or differentiator
- Multivibrator
- Narrow-band or band-pass filter
- Summing amplifier

Features:

- Input bias current (all types): 500 nA max.
- Input offset current (all types): 200 nA max.

RCA-CA1458, CA1558 (dual types); CA741C, CA741 (single-types); CA747C, CA747 (dual types); and CA748C, CA748 (single types) are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated-circuit devices provide output short-circuit protection and latch-free operation. These types also feature wide common-mode and differential-mode signal ranges and have low-offset voltage nulling capability when used with an appropriately valued potentiometer. A 5-megohm potentiometer is used for offset nulling types CA748C, CA748 (See Fig. 9); a 10-kilohm potentiometer is used for offset nulling types CA741C, CA741, CA747CE, CA747E (See Fig. 8); and types CA1458, CA1558, CA747CT, CA747T have no specific terminals for offset nulling. Each type consists of a differential-input amplifier that effectively drives a gain and level-shifting stage having a complementary emitter-follower output.

This operational amplifier line also offers the circuit designer the option of operation with internal or external phase compensation. Types CA748C and CA748, which are externally phase compensated (terminals 1 and 8) permit a choice of operation for improved bandwidth and slew-rate capabilities. Unity gain with externa. phase compensation can be obtained with a single 30-pF capacitor. All the other types are internally phase-compensated.

RCA's manufacturing process makes it possible to produce IC operational amplifiers with low-burst ("popcorn") noise characteristics. Type CA6741, a low-noise version of the CA741, gives limit specifications for burst noise in the data bulletin, File No. 530. Contact your RCA Sales Representative for information pertinent to other operational amplifier types that meet low-burst noise specifications.

ORDERING INFORMATION

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a TO-5 package is desired, order CA1458T.

RCA Type No.	No. of Ampl.	Phase Comp.	Offset Voltage Null	Min. A_{OL}	Max. V_{IO} (mV)	Operating-Temperature Range (°C)	Package Type and Suffix Letter						
							TO-5			Plastic		Chip	Beam-Lead
							8L	10L	DIL-CAN	8L	14L		
CA1458	dual	int.	no	20k	6	0 to +70	T		S	E		H	
CA1558	dual	int.	no	50k	5	−55 to +125	T		S				
CA741C	single	int.	yes	20k	6	0 to +70	T		S	E		H	
CA741	single	int.	yes	50k	5	−55 to +125	T		S				L
CA747C	dual	int.	yes*	20k	6	0 to +70		T			E	H	
CA747	dual	int.	yes*	50k	5	−55 to +125		T			E		
CA748C	single	ext.	yes	20k	6	0 to +70	T		S	E		H	
CA748	single	ext.	yes	50k	5	−55 to +125	T		S				

*In the 14-lead dual-in-line plastic package only.

ELECTRICAL CHARACTERISTICS

For Equipment Design

Characteristics	Symbols	Test Conditions		LIMITS						Units
		Supply Volts: $V^+ = 15$, $V^- = -15$		CA741C, CA747C*, CA748C*, CA1458			CA741, CA747*, CA748*, CA1558			
			Ambient Temperature (T_A)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	$R_S \leq 10$ kΩ	25°C	–	2	5	–	1	5	mV
			0 to 70°C	–	–	7.5	–	–	–	
			−55 to +125°C	–	–	–	–	1	6	
Input Offset Current	I_{IO}		25°C	–	20	200	–	20	200	nA
			−55°C	–	–	–	–	85	500	
			+125°C	–	–	–	–	7	200	
			0 to 70°C	–	–	300	–	–	–	
Input Bias Current	I_{IB}		25°C	–	80	500	–	80	500	nA
			−55°C	–	–	–	–	300	1500	
			+125°C	–	–	–	–	30	500	
			0 to 70°C	–	–	800	–	–	–	
Input Resistance	R_I		25°C	0.3	2	–	0.3	2	–	MΩ
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C	20,000	200,000	–	50,000	200,000	–	
			0 to 70°C	15,000	–	–	–	–	–	
			−55 to +125°C	–	–	–	25,000	–	–	
Common-Mode Input Voltage Range	V_{ICR}		25°C	±12	±13	–	–	–	–	V
			−55 to +125°C	–	–	–	±12	±13	–	
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10$ kΩ	25°C	70	90	–	–	–	–	dB
			−55 to +125°C	–	–	–	70	90	–	
Supply Voltage Rejection Ratio	V_{RR}	$R_S \leq 10$ kΩ	25°C	–	30	150	–	–	–	μV/V
			−55 to +125°C	–	–	–	–	30	150	
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10$ kΩ	25°C	±12	±14	–	–	–	–	V
			−55 to +125°C	–	–	–	±12	±14	–	
		$R_L \geq 2$ kΩ	25°C	±10	±13	–	–	–	–	
			0 to 70°C	±10	±13	–	–	–	–	
			−55 to +125°C	–	–	–	±10	±13	–	
Supply Current			25°C	–	1.7	2.8	–	1.7	2.8	mA
			−55°C	–	–	–	–	2	3.3	
			+125°C	–	–	–	–	1.5	2.5	
Device Dissipation	P_D		25°C	–	50	85	–	50	85	mW
			−55°C	–	–	–	–	60	100	
			+125°C	–	–	–	–	45	75	

*Values apply for each section of the dual amplifiers.

ELECTRICAL CHARACTERISTICS

Typical Values Intended Only for Design Guidance

Characteristics	Symbols	Test Conditions Supply Volts: $V^+ = 15$, $V^- = -15$	LIMITS CA741C CA747C* CA748C* CA1458	LIMITS CA741 CA747* CA748* CA1558	Units
Input Capacitance	C_I		1.4	1.4	pF
Offset Voltage Adjustment Range			±15	±15	mV
Output Resistance	R_O		75	75	Ω
Output Short-Circuit Current			25	25	mA
Transient Response Risetime	t_r	Unity Gain V_I = 20 mV R_L = 2 kΩ $C_L \leq$ 100 pF	0.3	0.3	μs
Overshoot			5.0	5.0	%
Slew Rate: Closed Loop	SR	$R_L \geq 2$ kΩ	0.5	0.5	V/μs
Open Loop▲			40	40	

▲Open-loop slew rate applies only for types CA748C and CA748.

*Values apply for each section of the dual amplifiers.

MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^oC$

DC Supply Voltage (between V^+ and V^- terminals):
- CA741C, CA747C▲, CA748C, CA1458▲ . . . . . 36 V
- CA741, CA747▲, CA748, CA1558▲ . . . . . 44 V

Differential Input Voltage . . . . . ±30 V

DC Input Voltage* . . . . . ±15 V

Output Short-Circuit Duration . . . . . Indefinite

Device Dissipation:
- Up to 70°C (CA741C, CA748C) . . . . . 500 mW
- Up to 75°C (CA741, CA748) . . . . . 500 mW
- Up to 30°C (CA747) . . . . . 800 mW
- Up to 25°C (CA747C) . . . . . 800 mW
- Up to 30°C (CA1558) . . . . . 680 mW
- Up to 25°C (CA1458) . . . . . 680 mW

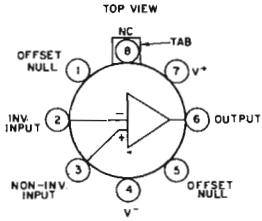
For Temperatures Indicated Above . . . . . Derate linearly 6.67 mW/°C

Voltage between Offset Null and V^- (CA741C, CA741, CA747CE) . . . . . ±0.5 V

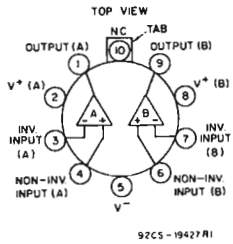
Ambient Temperature Range:
- Operating – CA741, CA747E, CA748, CA1558 . . . . . −55 to +125 °C
- CA741C, CA747C, CA748C, CA1458 . . . . . 0 to +70 °C
- Storage . . . . . −65 to +150 °C

Lead Temperature (During Soldering):
- At distance 1/16±1/32 inch (1.59±0.79 mm) from case for 10 seconds max. . . . . 265°C

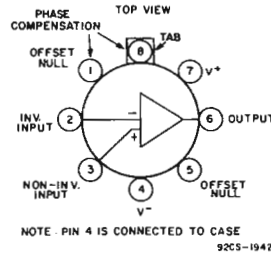
▲Voltage values apply for each of the dual operational amplifiers.



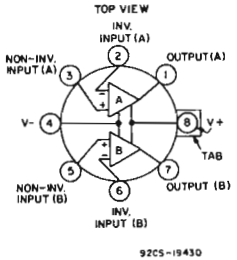
1a. – CA741CS, CA741CT, CA741S, & CA741T with internal phase compensation.



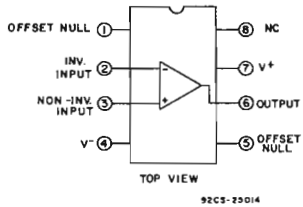
1b. – CA747CT and CA747T with internal phase compensation.



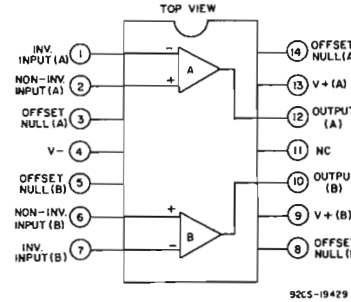
1c. – CA748CS, CA748CT, CA748S, and CA748T with external phase compensation.



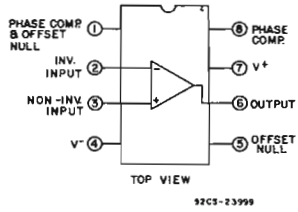
1d. – CA1458S, CA1458T, CA1558S, and CA1558T with internal phase compensation.



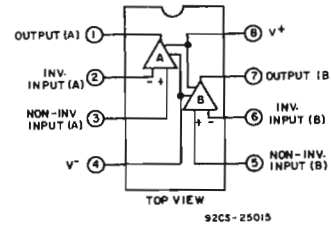
1e. – CA741CE with internal phase compensation.



1f. – CA747CE and CA747E with internal phase compensation.



1g. – CA748CE with external phase compensation.



1h. – CA1458E with internal phase compensation.

Fig. 1 – Functional diagrams.

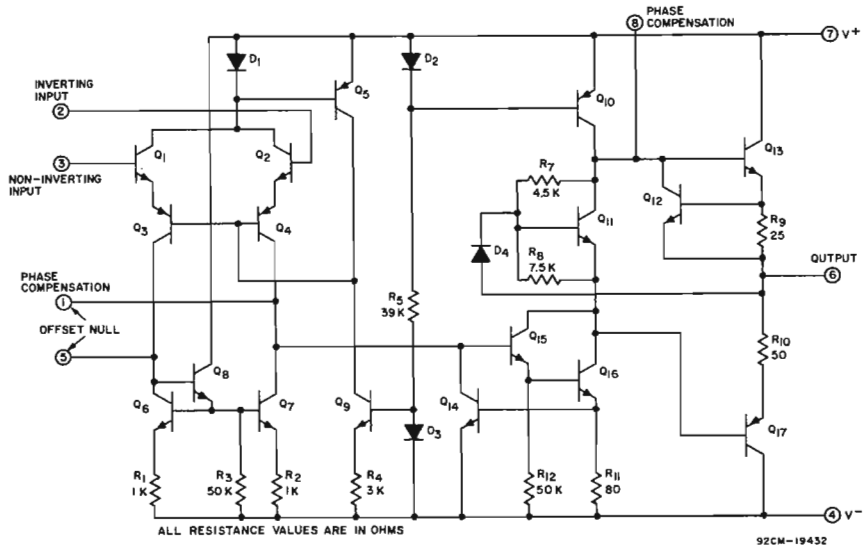


Fig.2—Schematic diagram of operational amplifier with external phase compensation for CA748C and CA748.

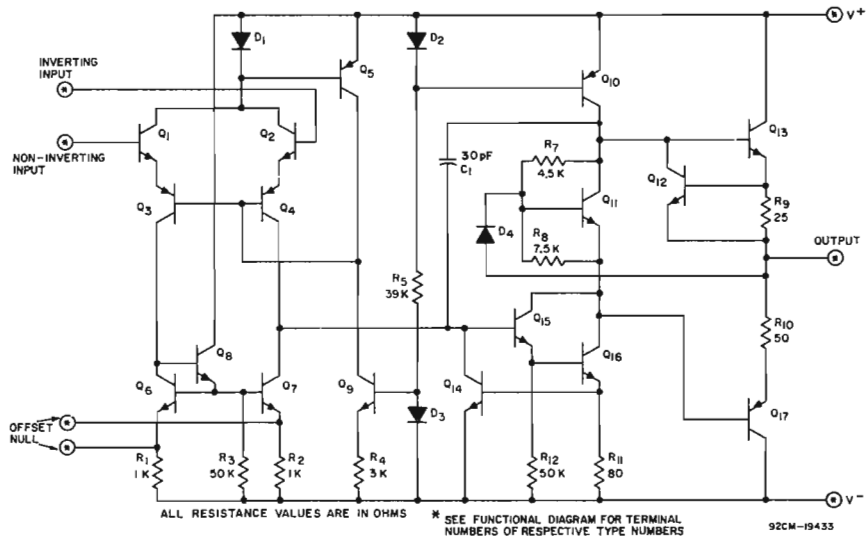


Fig.3—Schematic diagram of operational amplifiers with internal phase compensation for CA741C and CA741 and for each amplifier of the CA747C, CA747, CA1458, and CA1558.

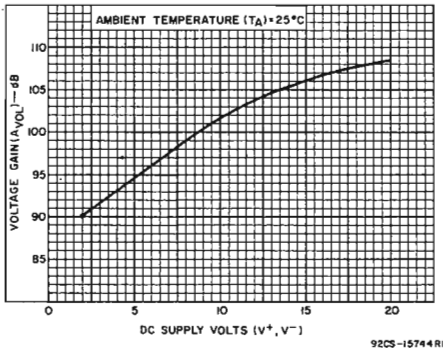


Fig. 4 — Open-loop voltage gain vs. supply voltage for all types except CA748 and CA748C.

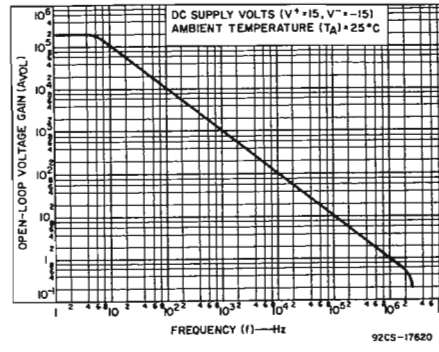


Fig. 5 — Open-loop voltage gain vs. frequency for all types except CA748 and CA748C.

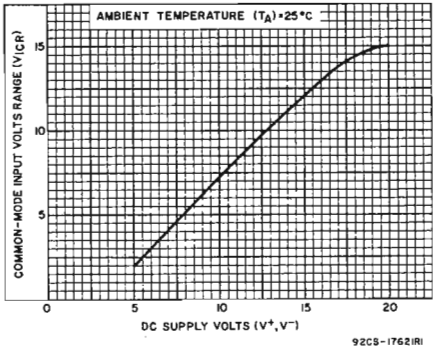


Fig. 6 — Common-mode input voltage range vs. supply voltage for all types.

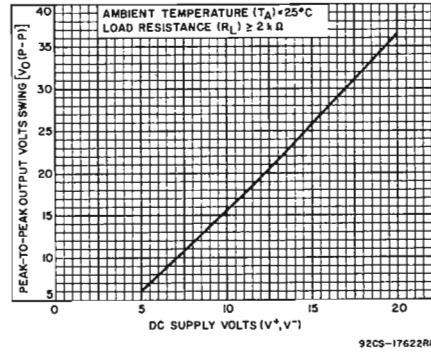


Fig. 7 — Peak-to-peak output voltage vs. supply voltage for all types except CA748 and CA748C.

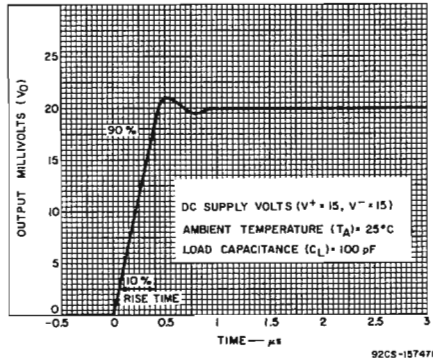


Fig. 8 — Output voltage vs. transient response time for CA741C and CA741.

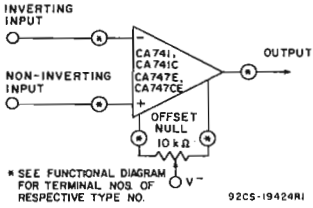


Fig. 9 – Voltage-offset null circuit for CA741C, CA741, CA747CE and CA747E.

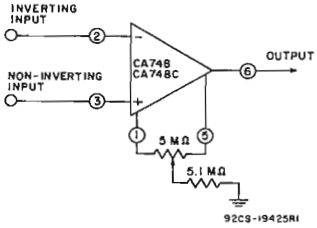


Fig. 10 – Voltage-offset null circuit for CA748C and CA748.

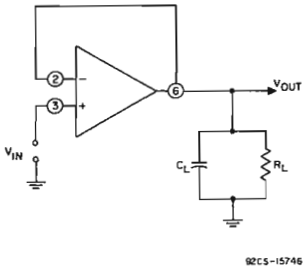


Fig. 11 – Transient response test circuit for all types.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA758E

16-Lead Dual-in-Line
Plastic Package

H-1622

RC Phase-Lock-Loop Stereo Decoder

For FM Multiplex Systems

Features:

- Low distortion (THD): 0.4% (typ.)
- Excellent SCA rejection: 70 dB typ.
- RC oscillator
- High-audio-channel separation: 45 dB
- Power supply range: 10 to 16 V dc
- Requires only one adjustment for complete alignment
- Low-impedance outputs
- Stereo indicator lamp drive: 150 mA typ.

RCA-CA758E is a monolithic silicon integrated circuit RC phase-lock loop stereo decoder intended for FM solid-state stereo multiplex systems.

The CA758E is pin compatible and electrically equivalent to industry types μA758, MC1311P, LM1800, and ULX2244.

The CA758E decodes the multiplexed stereo input signal into left and right channel audio output signals. The decoder also suppresses SCA (storecast) transmissions when present in the composite stereo signal.

The decoder uses a minimum of external components, and requires one adjustment (oscillator frequency) for complete alignment. In addition, the CA758E provides automatic mono-stereo mode switching and energizes a stereo indicator lamp.

The CA758E is supplied in a 16-lead dual-in-line plastic package and operates over an ambient temperature range of −40 to +85°C.

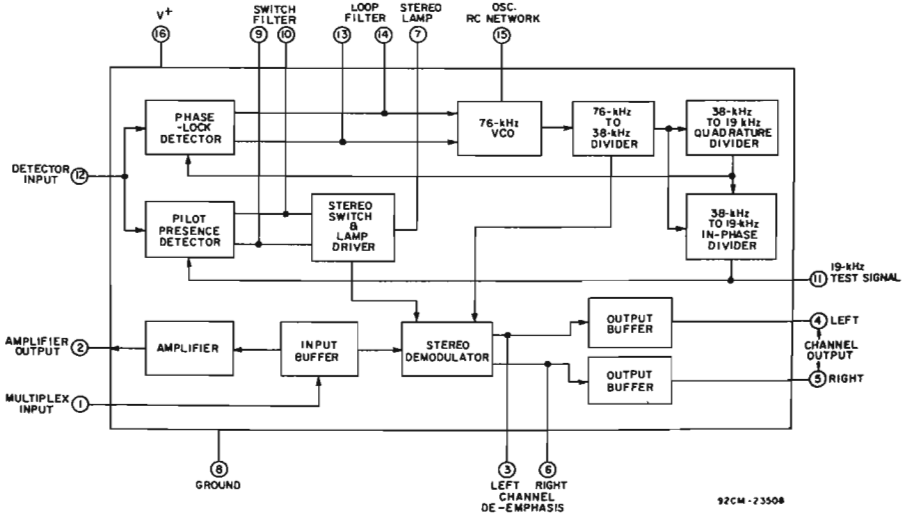


Fig. 1 — Functional block diagram of the CA758E.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DC Supply Voltage	+18 V
DC Supply Voltage (for ≤a 15-second period)	+22 V
DC Voltage at Term. 7 (Lamp Driver Circuit with Lamp "OFF")	+22 V
Device Dissipation:	
Up to $T_A = 70^oC$	730 mW
Above $T_A = 70^oC$ derate linearly	9.1 mW/°C
Ambient Temperature Range:	
Operating	−40 to +85°C
Storage	−65 to +150°C
Lead Temperature (During soldering):	
At a distance not less than 1/32" (0.79 mm)	
from case for 10 s max.	+265°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (Referenced to Fig. 3 unless otherwise specified) $V^+ = 12$ V, $T_A = 25^oC$ Multiplex Input Signal (L=R, pilot "OFF") = 300 mV RMS 19-kHz Pilot Level = 30 mV RMS f (modulation) = 400 Hz or 1 kHz	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Static Characteristics					
Total Current	Lamp "OFF"	–	26	35	mA
Maximum Available Lamp Current		75	150	–	mA
DC Voltage at Term. 7 (Lamp Driver)	I (Lamp) = 50 mA	–	1.3	1.8	V
DC Voltage Shift at either Term. 4 or 5 (Output)	Stereo-to-Mono Operation	–	30	150	mV
Dynamic Characteristics					
Power Supply Ripple Rejection	For a 200-Hz, 200-mV RMS Signal	35	45	–	dB
Input Resistance		20	35	–	kΩ
Output Resistance		0.9	1.3	2.0	kΩ
Channel Separation (Stereo)	At f = 100 Hz	–	40	–	dB
	f = 400 Hz	30	45	–	dB
	f = 10 kHz	–	45	–	dB
Channel Balance (Monaural)		–	0.3	1.5	dB
Voltage Gain	At f = 1 kHz	0.5	0.9	1.4	V/V
Pilot Input Level:					
19-kHz Input	Lamp "ON"	–	15	20	mV RMS
19-kHz Input	Lamp "OFF"	2.0	7.0	–	mV RMS
Hysteresis	Lamp "OFF"	3.0	7.0	–	dB
Capture Range (Deviation from 76-kHz Center Frequency)		±2.0	±4.0	±6.0	%
Total Harmonic Distortion	Multiplex Input Signal = 600 mV RMS (Pilot "OFF")	–	0.4	1.0	%
19-kHz Rejection		25	35	–	dB
38-kHz Rejection		25	45	–	dB
SCA (Storecast) Rejection	Measured Composite Signal: 80% Stereo, 10% Pilot, 10% SCA	–	70	–	dB
Voltage-Controlled Oscillator (VCO) Tuning Resistance	Total Resistance (Term. 15 to 8) required to set f_{REF} = 19 kHz ± 10 Hz (Term. 11)	21.0	23.3	25.5	kΩ
Voltage-Controlled Oscillator	$0^o \leq T_A \leq 25^oC$	–	+0.1	±2	%
Frequency Drift	$25^o \leq T_A \leq 70^oC$	–	−0.4	±2	%

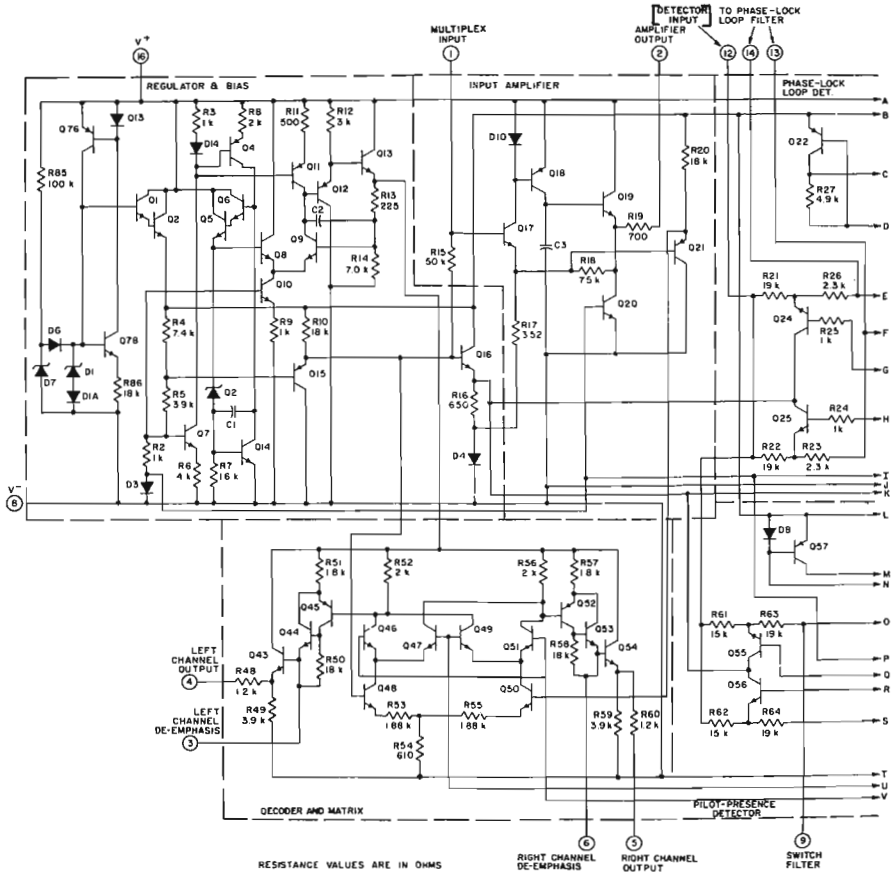


Fig. 2 – Schematic diagram of the CA758E.

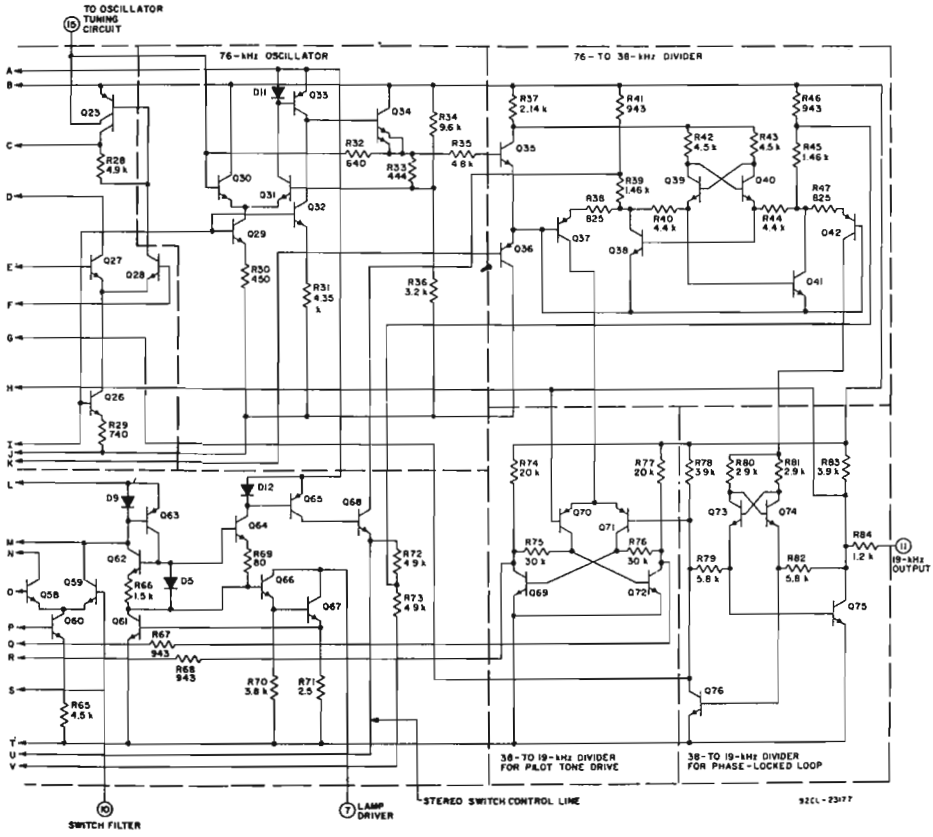


Fig.2 – Schematic diagram of the CA758E (Cont'd).

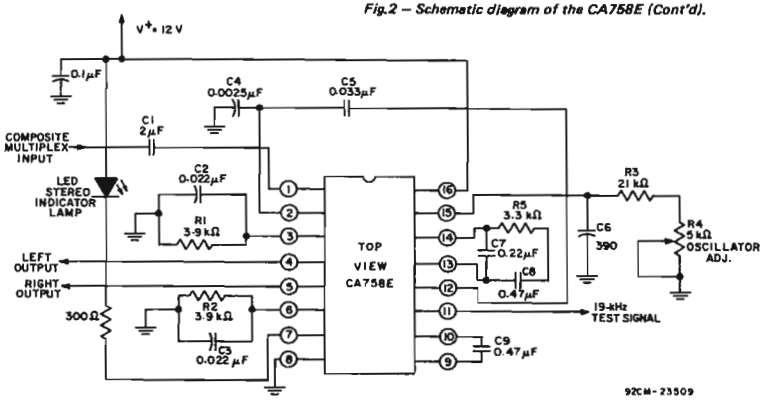


Fig. 3 – Test circuit for measurement of dynamic characteristics.

NOTES:

Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified.

C_1 = +100%, –20%

C_6 = ±1% in test circuit and ±5% in typical application.

R_3 = ±1%

R_4 = ±10%

R_1 and R_2 = ±1% in test circuit and ±5% in typical application.

TYPICAL PERFORMANCE CHARACTERISTICS (Referenced to Fig. 3)

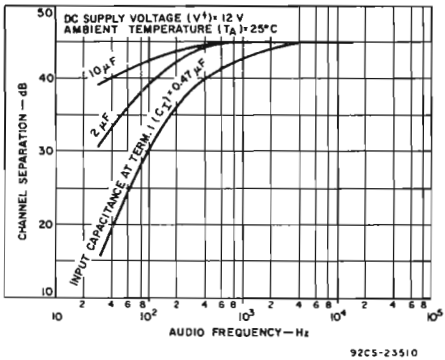


Fig. 4 — Channel separation vs. audio frequency.

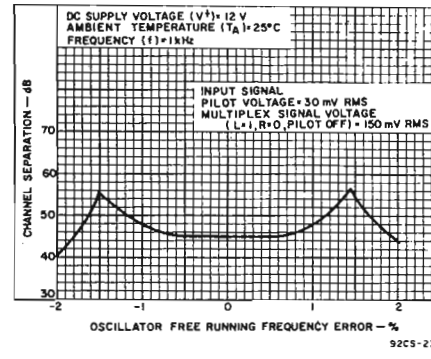


Fig. 5 — Channel separation vs. oscillator free running frequency error.

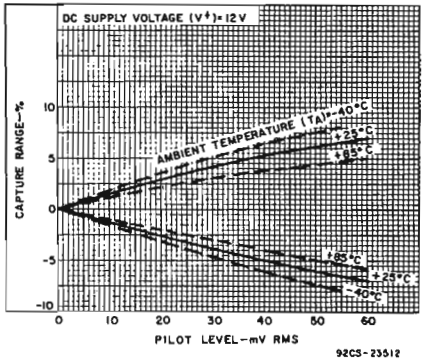


Fig. 6 — Capture range vs. pilot level.

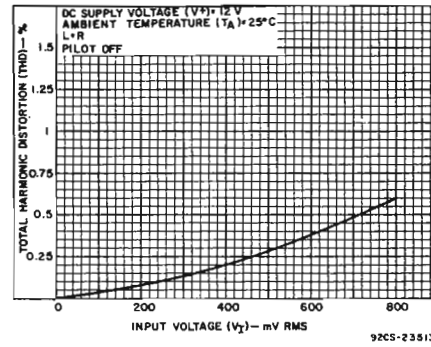


Fig. 7 — Total harmonic distortion vs. input level.

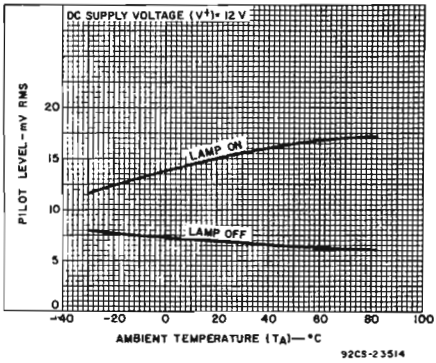


Fig. 8 — Lamp turn-on and turn-off sensitivity vs. ambient temperature.

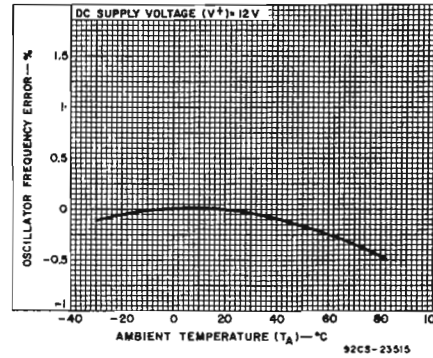


Fig. 9 — Oscillator free running frequency error vs. ambient temperature.

RCA
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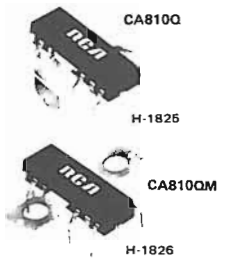
Linear Integrated Circuits

Monolithic Silicon

CA810Q
CA810QM

Preliminary Data



Modified 16-lead quad-in-line plastic packages with wing tabs

7-Watt Audio Power Amplifier With Thermal Shut-Down

Features

- Power output — 7 W with 4Ω load
- Supply voltage range — 4 to 20 V
- Peak output current — 2.5 A (max.)
- Very low harmonic and cross-over distortion

The RCA-CA810Q and CA810QM are monolithic audio amplifiers intended for class B operation. They are specifically designed for mobile equipment operating from 12-V battery supplies. They operate over a wide range of supply voltages (4 to 20 V) with very low harmonic and crossover distortion. The maximum repetitive peak output current is 2.5 A, and an integral thermal limiting circuit shuts the device down in case of output overload or excessive package temperature.

The CA810Q and CA810QM are supplied in modified 16-lead quad-in-line plastic packages ("Q" suffix) with integral wing-tab heat sinks. The tabs on the CA810Q are bent down for p.c. board insertion, and on the CA810QM they are flat and pierced for easy attachment to an external heat sink.

The CA810Q and CA810QM are electrically and mechanically equivalent to types TBA810S and TBA810AS, respectively. It should be noted that pin-numbering conventions for these devices may differ from manufacturer to manufacturer, however the devices are pin compatible and interchangeability is not affected.

MAXIMUM RATINGS, *Absolute Maximum Values at $T_A = 25^{\circ}C$*

SUPPLY VOLTAGE			20 V
PEAK OUTPUT CURRENT (non-repetitive)			3.5 A
PEAK OUTPUT CURRENT (repetitive)			2.5 A
DEVICE DISSIPATION:			
At $T_A = 70^{\circ}C$			1 W
At $T_{tab} = 100^{\circ}C$			5 W
AMBIENT TEMPERATURE RANGE:			
Operating			$-40^{\circ}C$ to (Refer to Fig. 7 for typical high-temperature limit)
Storage			-40 to $+150^{\circ}C$
THERMAL RESISTANCE:	CA810Q	CA810QM	
Junction to tab	12	10	$^{\circ}C/W$
Junction to ambient	70*	80	$^{\circ}C/W$

*Value obtained with tabs soldered to printed-circuit board

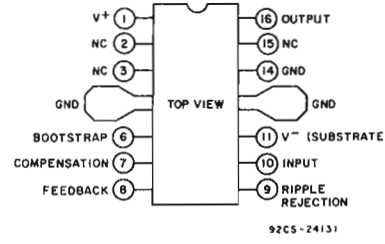


Fig. 1 — Terminal diagram of CA810Q and CA810QM. The wing tabs on the CA810Q are bent down, and on the CA810QM they are flat and pierced.

ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS CA810Q CA810QM			UNIT
		Supply Voltage (V^+) = 14.4 V Unless Otherwise Specified		MIN.	TYP.	MAX.	
Supply Voltage	V^+			4	–	20	V
Input Voltage	V_I			–	–	220	mV
Input Sensitivity	e_I	P_O=6 W, R_L=4 Ω, R1 = 56 Ω, f = 1 kHz		–	80	–	mV
Quiescent Output Voltage	V_O			6.4	7.2	8	V
Quiescent Current Drain	I_O			–	12	20	mA
Input Noise Voltage	e_N	R_g=0, BW (–3 dB) =20 to 20,000 Hz		–	2	–	μV
Bias Current	I_{IB}			–	0.4	–	μA
Output Power	P_O	f=1 kHz, R_L=4Ω, THD = 10%	V^+= 14.4 V	–	6	–	W
			V^+= 6 V	–	1	–	
Input Resistance	R_I			–	5	–	MΩ
Total Harmonic Distortion	THD	P_O=50 mW to 3W, R_L 4 Ω, f = 1 kHz		–	0.3	–	%
Open-Loop Voltage Gain	A_{OL}	R_L = 4 Ω, f = 1 kHz		–	80	–	dB
Closed-Loop Voltage Gain	A	R_L = 4 Ω, f = 1 kHz, R1 = 56 Ω		34	37	40	dB
Efficiency	η	P_O = 5 W, R_L = 4 Ω, f = 1 kHz		–	70	–	%

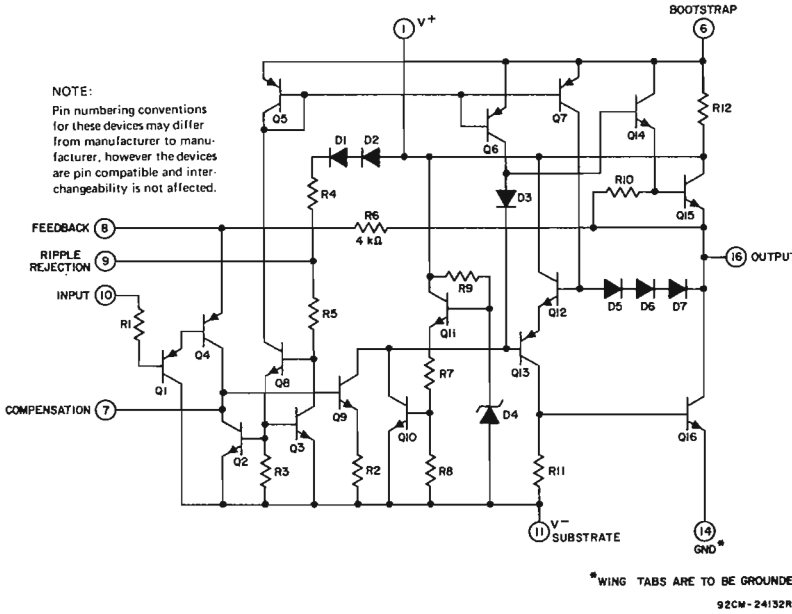


Fig. 2 – Schematic diagram of CA810Q, CA810QM.

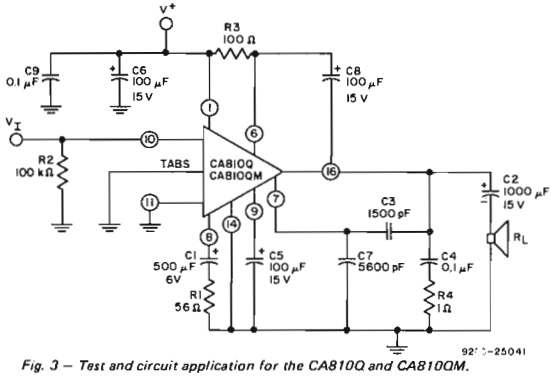


Fig. 3 – Test and circuit application for the CA810Q and CA810QM.

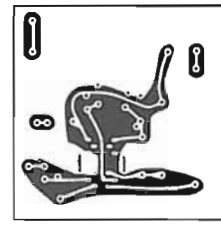
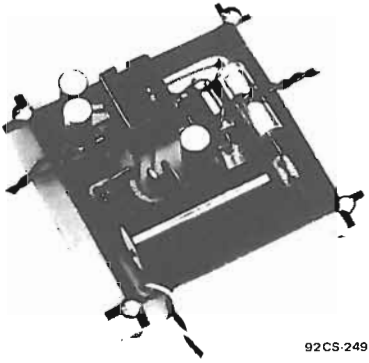
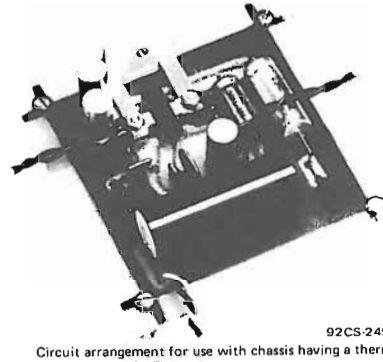


Fig. 4 – Bottom view of printed-circuit boards shown in Figs. 5 and 6.



Circuit heat is dissipated by a combination of free air and printed-circuit board foil.

Fig. 5 – Component view of printed-circuit board for CA810Q.



Circuit arrangement for use with chassis having a thermal resistance of $\leq 5^{\circ}C/W$. Vertical bracket should make good thermal contact to chassis.

Fig. 6 – Component view of printed-circuit board for CA810QM.

The thermal-limiting network incorporated in the CA810 Series circuits provides protection against damage due to excessive semiconductor temperatures that may result from high ambient temperatures and/or excessive dissipation, e.g., as encountered in sustained overloads. As indicated in Fig. 7, the thermal-limiting feature automatically reduces the supply current (and output power) at the higher temperatures.

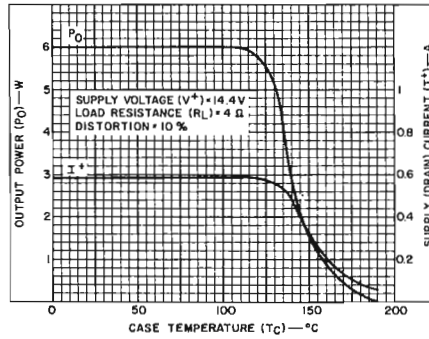


Fig. 7 — Typical output power and drain current vs. case temperature.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA1310E

14-Lead Dual-in-Line Plastic Package H-1517

RC Phase-Lock-Loop Stereo Decoder

For FM Multiplex Systems

Features:

- Low distortion (THD): 0.3% typ.
- Excellent SCA (storecast) rejection: 75 dB typ.
- RC oscillator
- High audio channel separation: 40 dB
- Operates from a wide range of power supplies: 8 to 14 V dc
- Requires only one adjustment for complete alignment
- Drives a stereo indicator lamp up to 75 mA — surge current limiting

RCA-CA1310E is a monolithic silicon integrated circuit RC phase-lock-loop stereo decoder intended for FM solid-state stereo multiplex systems.

The CA1310E is a direct replacement for industry types MC1310P, LM1310, and SN76115N.

This decoder uses a minimum of external components. In addition the stereo decoder requires only one adjustment (oscillator frequency) for complete alignment.

The CA1310E is supplied in a 14-lead dual-in-line plastic package and operates over an ambient temperature range of −40 to +85°C.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DC Supply Voltage	14 V
Current (Lamp) at Term. 6	75 mA
Device Dissipation:	
Up to $T_A = 25^oC$	625 mW
Above $T_A = 25^oC$ derate linearly	5 mW/°C
Ambient Temperature Range:	
Operating	−40 to +85°C
Storage	−65 to +150°C
Lead Temperature (During soldering):	
At distance not less than 1/32" (0.79 mm) from case for 10 s max.	+265°C

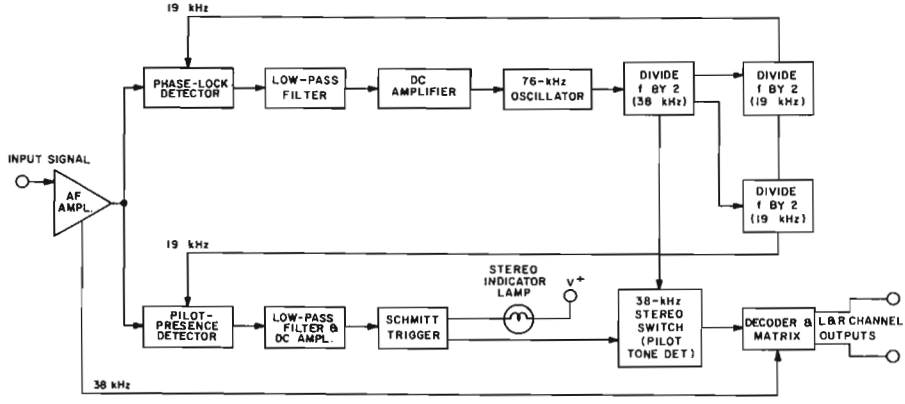


Fig. 1 — Functional block diagram system using the CA1310E.

92CS-23500

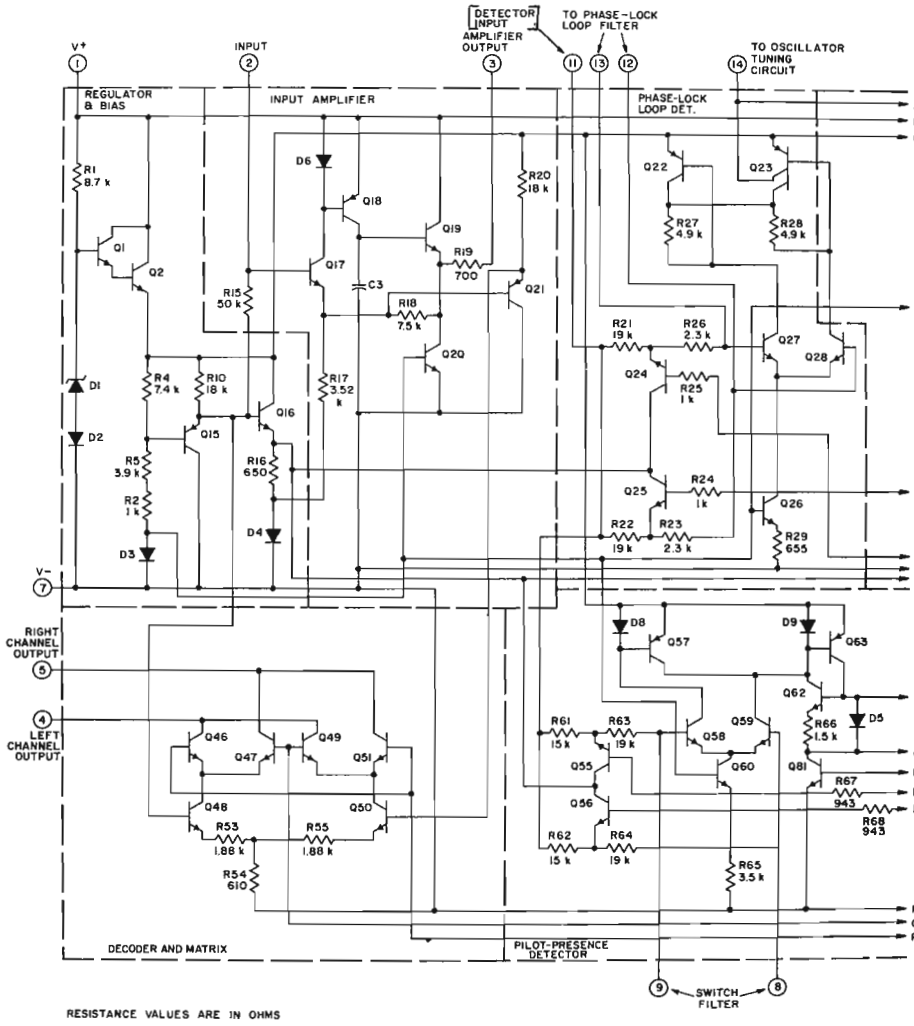


Fig. 2 – Schematic diagram of the CA1310E.

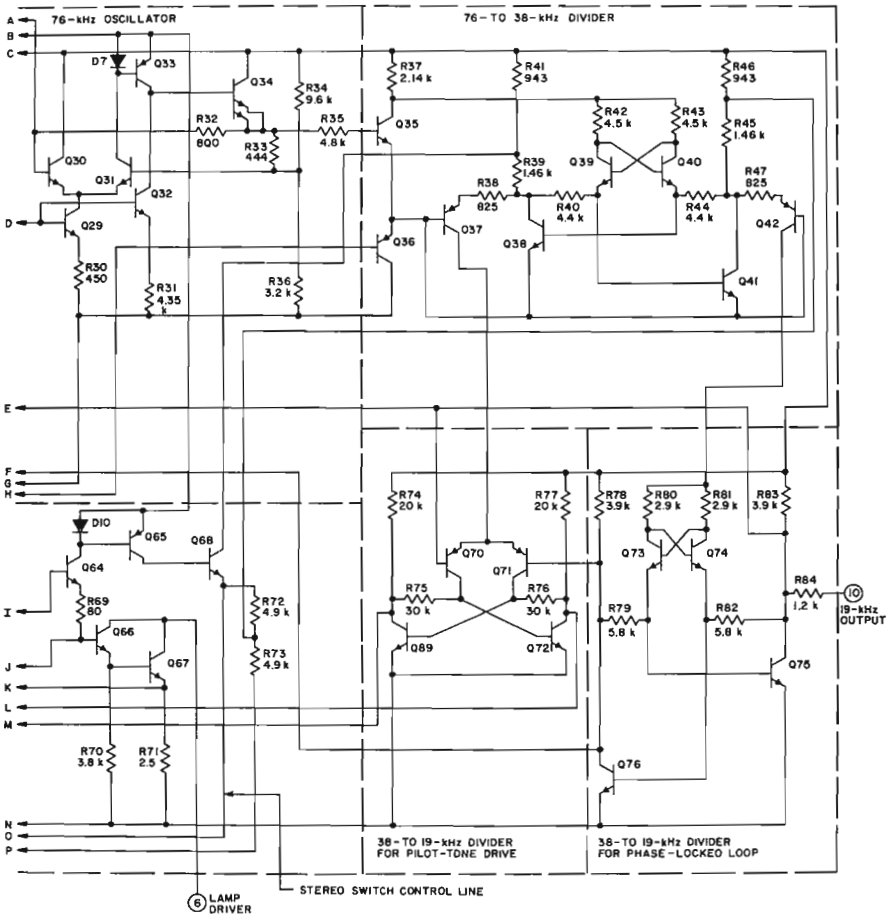
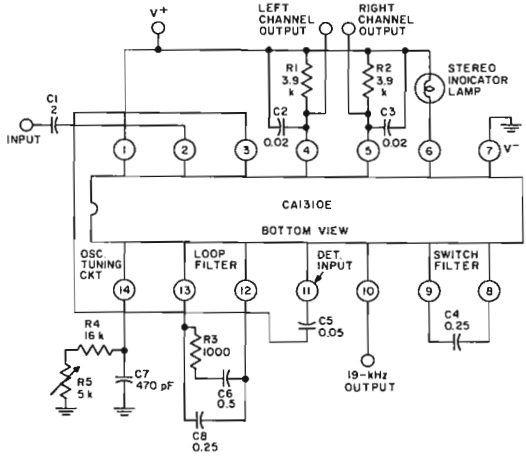


Fig. 2 – Schematic diagram of the CA1310E (Cont'd).

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (Referenced to Fig. 3) $V^+ = 12$ V $T_A = 25^oC$ Composite Multiplex Input Signal = 560 mV RMS (2.8 V p-p) Only L or R Channel modulated; and with 100-mV RMS (10%) Pilot Level	LIMITS			UNITS
		Min.	Typ.	Max.	
Static Characteristics					
DC Supply Voltage	For 8-V operation, reduce load to 2.7 kΩ	8	–	14	V
Total Current	Lamp "OFF"	–	13	–	mA
Dynamic Characteristics					
Input Impedance		20	50	–	kΩ
Channel Separation (Stereo)	50 Hz – 15 kHz	30	40	–	dB
Audio Output Voltage (For any one channel)		–	485	–	mV RMS
Channel Balance (Monaural)	Pilot Tone "OFF"	–	–	1.5	dB
Capture Range (Permissible tuning error of internal oscillator)		–	±3.5	–	%
Total Harmonic Distortion		–	0.3	–	%
Ultrasonic Frequency Rejection: 19 kHz		–	34.4	–	dB
38 kHz		–	45	–	dB
SCA (Storecast) Rejection	f = 67 kHz, 9-kHz beat note measured with 1-kHz modulation "OFF"	–	75	–	dB
Stereo Switch Level: 19-kHz Input Level (For lamp on)		–	–	20	mV RMS
19-kHz Input Level (For lamp off)		5	–	–	mV RMS
Maximum Composite (Stereo) Input	0.5% THD	2.8	–	–	V p-p
Maximum Monaural Input	1% THD	2.8	–	–	V p-p



RESISTANCE VALUES ARE IN OHMS.
CAPACITANCE VALUES ARE IN MICROFARADS.

92CS-23501

NOTES

A buffered 3-volt positive-going square wave is available at Term. 10. The alignment of the free-running oscillator frequency may be checked at this point with a frequency counter.

C1: A lower value input coupling capacitor may be used in place of the 2-μF value if reduced separation at low frequencies is acceptable.

C4: The time constant for the stereo switch level detector circuit is calculated by C4 x 53,000 ohms ±30% with a maximum dc voltage drop across C4 of 0.25 volt (Term. 8 positive) and a pilot level voltage of 100 mV RMS. Signal voltage across C4 is negligible.

C5: The recommended 0.05-μF capacitor provides a 1.75° phase lead at 19 kHz.

R1, R2: Load resistance values are related to supply voltage as follows:

Minimum Supply Voltage	8	10	12	V
Maximum Load Resistance	2.7	4.3	6.2	kΩ

R3, C6, C8: C8 may be omitted, R3 = 100 ohms and C6 = 0.25 μF, if relaxed circuit performance is acceptable.

R4, R5, C7: If a capture range greater than ±3% typ. is required, reduce value of C7 and increase values of R4, R5 proportionally. However, beat-note distortion is increased at high signal levels because of oscillator-phase jitter. R4, C7 = ±1% in test circuit and ±5% in typical application.

Fig. 3 — Test circuit for measurement of dynamic characteristics.

Preliminary Data

14-Lead Dual-In-Line Plastic Package

H-1517

TV Video Amplifier

With AGC and Keyer Circuit

Features

- High 45-MHz gain — 53 dB (typ.)
- High-gain gated AGC system — with either positive- or negative-going sync.
- Adjustable rf AGC delay to tuner
- AGC gain reduction — 68 dB (typ.)

The RCA-CA1352E is a monolithic integrated circuit designed for use as an if amplifier in monochrome or color TV receivers. It features a high-gain gated AGC system with a 68-dB range (typ.). A delayed forward AGC output is adjustable by means of a potentiometer. Either positive- or negative-going sync may be used for this system.

MAXIMUM RATINGS, *Absolute-Maximum Values*
At T_A = 25

SUPPLY VOLTAGE:
- Between terminals 4 and 11 ..... 18 V
- Between terminals 7 or 8 and 4 ..... 18 V

INPUT VOLTAGE (terminal 1 or 2) ..... 10 V p-p
AGC INPUT VOLTAGE (terminal 6 or 10) ..... 6 V
DEVICE DISSIPATION:
- Up to T_A = 55°C ..... 750 mW
- Above T_A = 55°C derate linearly at ..... 7.9 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... −40 to +85°C
- Storage ..... −65 to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

The CA1352E is supplied in the 14-lead dual-in-line plastic package, and is directly interchangeable with the industry type 1352 in similar packages.

TYPICAL STATIC CHARACTERISTICS
at T_A = 25°C, V^+ = 12 V

Total Current ($I_7 + I_8 + I_{11}$) ..... 27 mA
Output Stage Current ($I_7 + I_8$) ..... 5.7 mA

TYPICAL DYNAMIC CHARACTERISTICS
at T_A = 25°C, V^+ = 12 V

AGC Range ..... 68 dB
Power Gain ..... 53 dB
Minimum rf AGC Range (term. 12) ..... 0.2 V
Maximum rf AGC Range (term. 12) ..... 7 V

SYNC POLARITY	* VOLTAGE AT TERMINAL 6	* VOLTAGE AT TERMINAL 10	* VALUE OF R1−Ω
NEGATIVE	5.5 V, −2 V, 0 V	1 TO 4 V NOM•2 V	0
POSITIVE	1 TO 8 V NOM•4.5	4.5 V, 0 V	3.9k

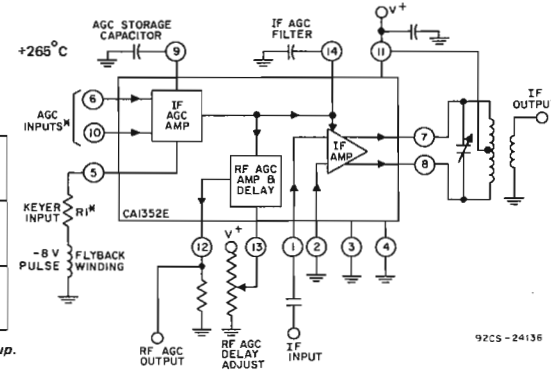


Fig. 1 — CA1352E block diagram and typical AGC test set-up.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA1398E

14-Lead Dual-In-Line Plastic Package H-1517

Television Chroma Processor

Features

- Minimum number of external components required
- Injection-lock oscillator with internal feedback
- DC chroma gain control and hue control circuits
- Low-impedance internal voltage regulation

RCA-CA1398E is a monolithic silicon integrated-circuit chroma processor containing chroma-amplifier and gain-control, color-killer, color subcarrier oscillator, hue control, and ACC circuitry. It has been designed for interchangeability with other "1398"-type chroma-processor devices. It functions compatibly with the RCA-CA3125E Chroma Demodulator as well as other commercially available chroma demodulators in color-TV receivers. Fig. 2 shows a functional block diagram of a 2-package TV chroma system incorporating the CA1398E and CA3125E. The CA1398E is supplied in a 14-lead dual-in-line plastic package.

Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25^\circ C$

Peak Horizontal-Pulse Input Current	250 μA
Supply Current (Terminal 14)	35 mA
Ambient Temperature Range:	
Operating	−40 to +85°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

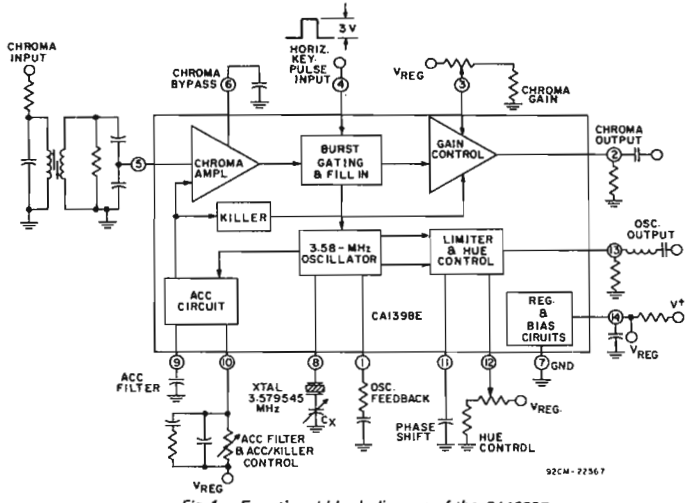


Fig. 1 – Functional block diagram of the CA1398E.

ELECTRICAL CHARACTERISTICS at T_A = 25°C and Referenced to Test Circuit (Fig. 4)

CHARACTERISTIC	TERMINAL MEASURED AND SYMBOL	TEST CONDITIONS						LIMITS			UNITS
		SWITCH POSITION (S1)	CONTROL SETTING CHROMA	HUE	KILLER	V_{BURST} mV p-p	V_{CHROMA} mV p-p	MIN.	TYP.	MAX.	
Static Characteristics											
Regulated Supply Voltage	V_{14}	2	max.	max.	max.	0	0	8.9	9.5	11.5	V
Chroma Output Bias	V_{14} to V_2	2	max.	max.	max.	6	0	1.2	2.4	3.6	V
Regulator Impedance	See Note 1	2	max.	max.	max.	0	0	–	12	25	Ω
Dynamic Characteristics (Refer to Test Set-Up Procedure for Oscillator)											
Max. Chroma Gain	V_2	1	max.	max.	See Note 2	6	5	310	425	–	mV p-p
Min. Chroma Gain	V_2	1	min.	max.		6	5	–	–	7	mV p-p
ACC Action	V_2 (dB up from gain test)	1	max.	max.		50	50	2	7	11	dB
Killer Function: Kill	V_2	2	max.	max.		0	5	–	–	7	mV p-p
Unkill	V_2	1	max.	max.		15	5	100	–	–	mV p-p
Oscillator Lock-Up: Voltage	V_{13}	1	max.	max.		6	0	250	340	390	mV p-p
Phase (Referenced to burst)	ϕ_{13}	1	max.	max.		6	0	–20	0	+20	degrees
Hue Control Range: Voltage	V_{13}	1	max.	min.		6	0	250	340	390	mV p-p
Phase (Referenced to burst)	ϕ_{13}	1	max.	min.		6	0	95	110	140	degrees

Note 1 – Measure V_{14} at I_{SUPPLY} = 38 mA and 18 mA. Calculate the regulator impedance:
$Z_{reg.} = [V_{14}$ (at 38 mA) $- V_{14}$ (at 18 mA)$]/0.02$

Note 2 – Increase the killer potentiometer resistance from minimum until the circuit unkills. This condition is evidenced by a shift in bias voltage at Term. 2 Maintain this potentiometer setting for all the dynamic tests.

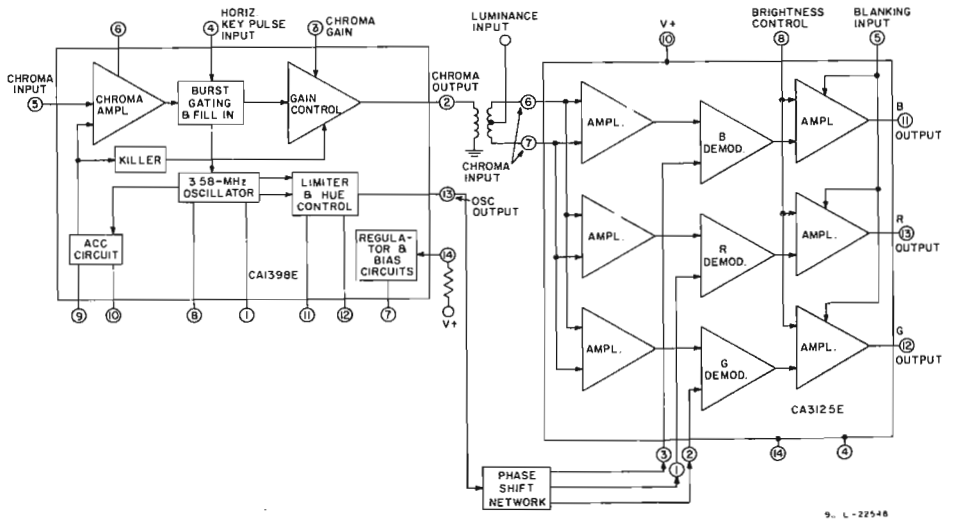


Fig. 2 – TV chroma system functional block diagram.

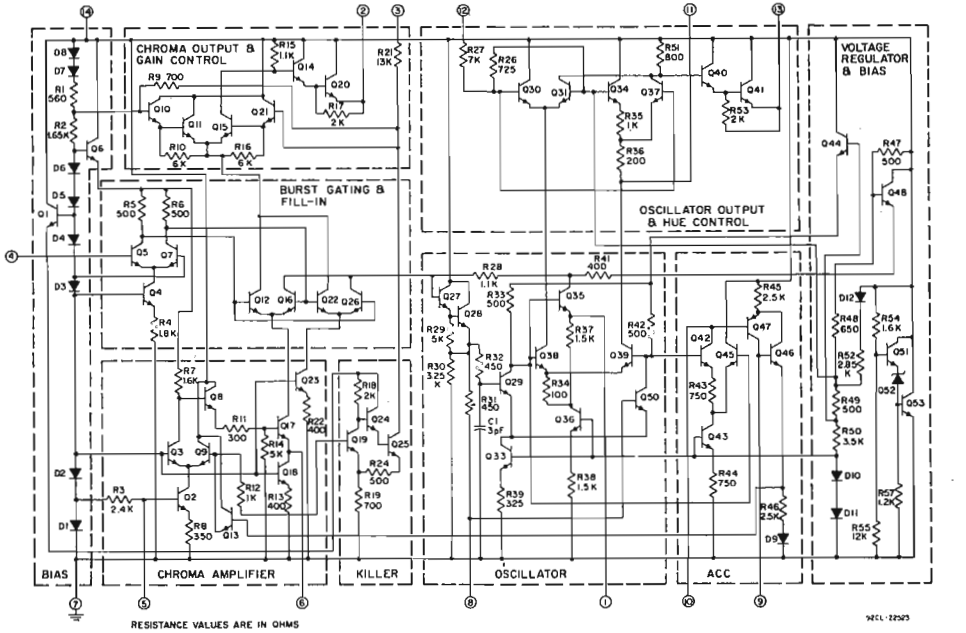


Fig. 3 – Schematic diagram of the CA1398E.

TEST SET-UP PROCEDURE FOR OSCILLATOR

Remove the horizontal keying and chroma inputs and adjust C_X to obtain a free-running oscillator frequency of 3.579545 MHz ±10 Hz. Under the same Test Conditions described in the Electrical Characteristics Chart for Oscillator Lock-Up, vary L1 (approx. 20 μH) and/or C1 (approx. 1000 pF) to obtain the initial conditions for amplitude and phase oscillator lock-up.

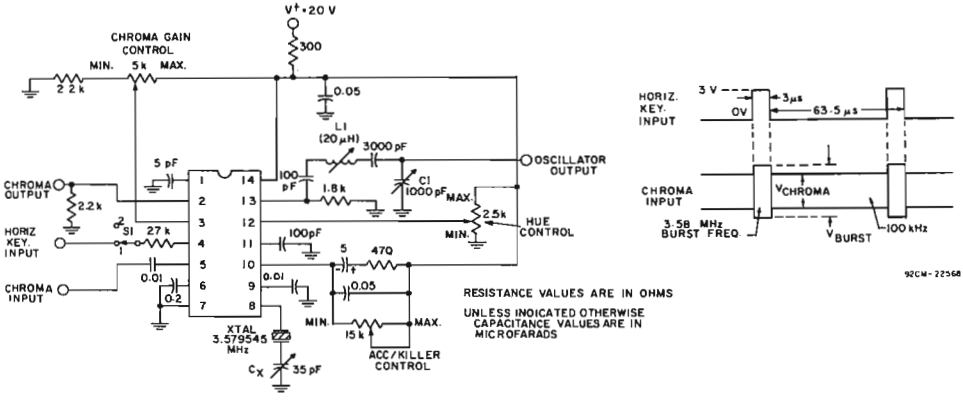


Fig. 4 – Typical static and dynamic characteristics test circuit for the CA1398E.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA1541D

14-Lead Dual-In-Line
Ceramic Package H-1553

Dual-Input Memory Sense Amplifier

Features

- Complete dual input core memory sense amplifier
- Two available outputs: —Saturated logic output
  —Linear output (positive output for either polarity input)
- Nominal threshold voltage: 17 mV
- Adjustable threshold: 10 to 35 mV
- Low threshold uncertainty range: ±3 mV
- Fast overload recovery time: —Differential-Mode: 15 ns typ.
  —Common-Mode: 30 ns typ.
- Independent channel gate and strobe terminals compatible with saturated logic levels
- Suitable for core memories having cycle times ≥ 0.4 μs
- Input offset voltage: 6 mV max.

RCA-CA1541D*, a monolithic silicon integrated circuit, is a dual-input memory sense amplifier intended for core memory applications.

The sense amplifier, consisting of two differential input amplifiers, a common second stage amplifier, and an output logic gate (See Fig. 1), converts low-level core-memory "1" pulses to saturated logic-level output pulses. Either one of the input amplifiers may be gated ON with a saturated logic signal so that an incoming "1" pulse of positive or negative polarity can be detected from either of two sense lines.

The CA1541D features an external switching threshold adjustment, plus its gate and strobe inputs are compatible with saturated logic levels. The sense amplifier is suitable for operation with core memories having cycle times equal to or greater than 0.4 μs and is unilaterally interchangeable with industry types 1541L and 1441.

The CA1541D is supplied in 14-lead dual-in-line ceramic package and is rated for operation over the full military temperature range of −55°C to +125°C.

*Formerly Developmental Type TA5820.

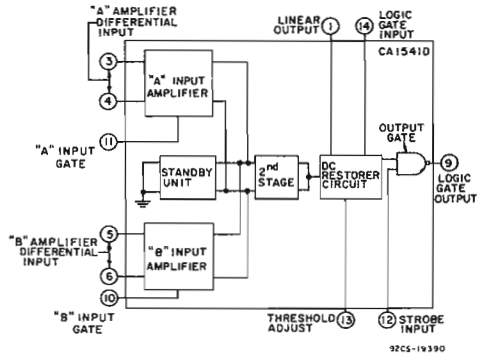


Fig. 1 — Functional block diagram of the CA1541D.

MAXIMUM RATINGS, Absolute Maximum Values, at T_A = 25°C

Except for Differential Input Voltage, all voltages are measured with respect to ground (Term. 8).

DC Supply Voltage:	
V^+ (Term. 2)	+10 V
V^- (Term. 7)	−10 V
Differential Input Voltage	±5 V
Common-Mode Input Voltage	±5 V
"A" or "B"-Gate Input Voltage*	V^- to V^+
Strobe Terminal Voltage	V^- to +6V
Output Terminal Load Current	±25 mA
Device Dissipation:	
Up to T_A = 75°C	750 mW
Above T_A = 75°C	Derate Linearly 8 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125 °C
Storage	−65 to +150 °C
Lead Temperature (during soldering):	
At distance not less than 1/32 inch (0.79 mm) from case for 10 seconds max.	+265°C

*Note: The "A" or "B"-Gate Input Voltage is also referred to, as the Channel-Gate Input Voltage.

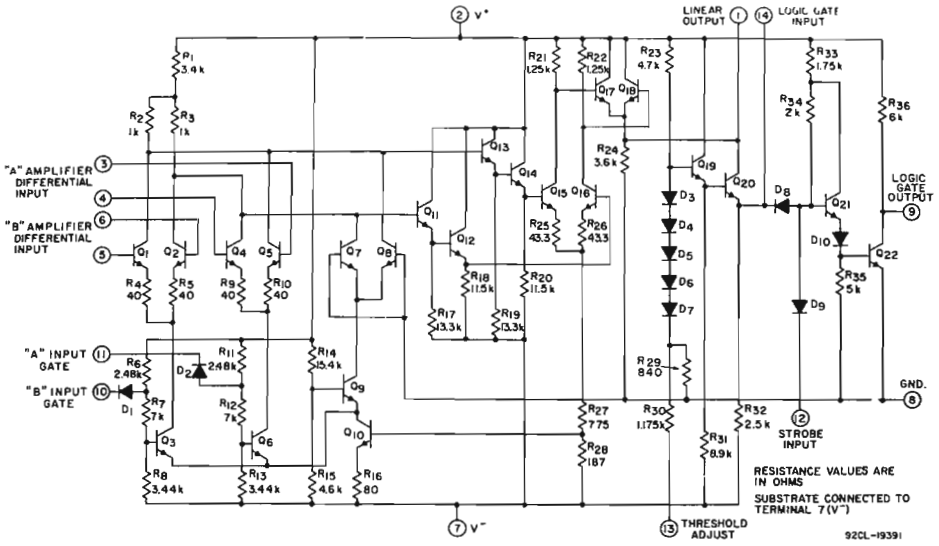


Fig. 2 — Schematic diagram of the CA1541D.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS			UNITS
		$V^+ = 5V$, $V^- = -5V$, V_{TH} ADJ. = −5V ± 1%, (Term. 13) $C_{EXT} = 0.01\ \mu F$	$T_A = 25^oC$ (unless indicated otherwise)	MIN.	TYP.	MAX.	
Static (DC) Characteristics							
Power Dissipation	P_D			–	140	180	mW
Input Offset Current	I_{IO}			–	1	2	μA
Input Bias Current:							
$T_A = 25^oC$	I_{IB}		$V_5 = V_6 = V_3 = V_4 = 0$	–	5	25	μA
$T_A = -55^oC$				–	–	50	
Output Voltage:							
High	V_{OH}	$I_{OM} = 200\ \mu A$		3	–	–	V
Low —		$V_{14} = 5$ V, $I_9 = 10$ mA					
$T_A = 25^oC$	V_{OL}			–	–	350	mV
$T_A = 125^oC$				–	–	400	
Strobe Load Current	I_S	$V_{12} = 0$		–	–	1.5	mA
Strobe Reverse Current:							
$T_A = 25^oC$	I_{SR}	$V_{12} = 5V$		–	–	2	μA
$T_A = 125^oC$				–	–	25	
Input Gate Load Current	I_G	$V_{10} = V_{11} = 0$		–	–	2.5	mA
Input Gate Reverse Current:							
$T_A = 25^oC$	I_{GR}	$V_{10} = V_{11} = 5V$		–	–	2	μA
$T_A = 125^oC$				–	–	25	
Switching Characteristics							
Input Threshold Voltage:							
$T_A = 25^oC$	V_{TH}			14	17	20	mV
$T_A = -55$ to 125^oC				12	17	22	
Input Offset Voltage	V_{IO}			–	1	6	mV
Input Gate Voltage:							
High	V_{GH}	$V_3 = V_5 = 25$ mV,		–	1.6	—	V
Low	V_{GL}	$V_4 = V_6 = 0$		–	0.7	–	
Common-Mode Range:							
Input Gate High	V_{CM}			–	±1.5	–	V
Input Gate Low				–	±1.5	–	
Differential-Mode Range:							
Input Gate High	V_{DH}			–	±600	–	mV
Input Gate Low	V_{DL}			–	±1.5	–	V
Propagation Delay:							
Input to Amplifier Output	t_{IA}	$V_3 = 25$ mV (pulsed),		–	10	15	ns
Input to Output	t_{IO}	$V_{12} = 2V$		–	20	30	
Strobe to Output	t_{SO}	$V_3 = V_4 = V_5 = V_6 = 0$, $V_{12} = 2V$ (pulsed)		–	15	20	
Gate Input to Amplifier Output	t_{GA}	$V_{11} = 2V$ (pulsed)		–	10	15	
Gate Input to Amplifier Input	t_{GI}	$V_3 = 25$ mV		–	30	35	
Common-Mode Recovery Time:							
Input Gate High	t_{CMR}	$V_3 = V_5 = 1.5$ V		–	15	30	ns
Input Gate Low				–	15	30	
Differential-Mode Recovery Time:							
Input Gate High	t_{DR}	$V_3 = V_5 = 400$ mV		–	30	–	ns
Input Gate Low				–	0	–	

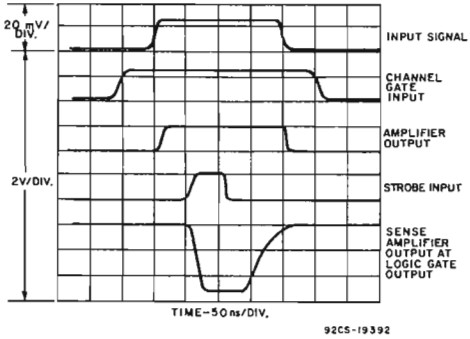


Fig. 3 – Typical operational wave forms.

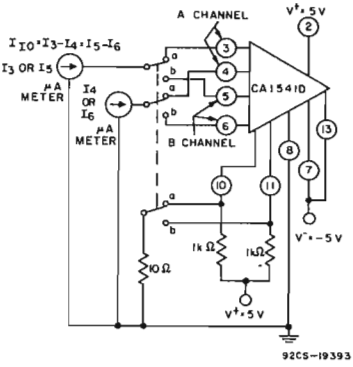


Fig. 4 – Input bias (I_{IB}) and input-offset current (I_{IO}) test circuit.

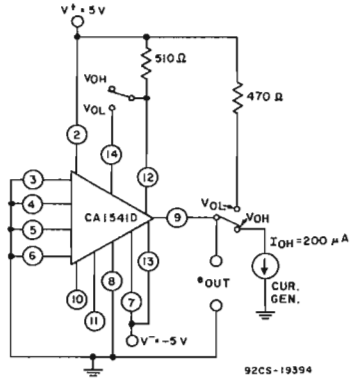


Fig. 5 – Test circuit for measurement of low (V_{OL}) and high (V_{OH}) output voltage levels.

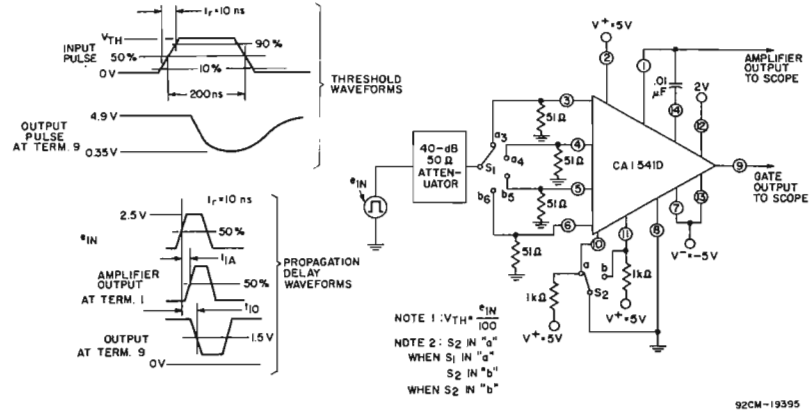


Fig. 6 – Threshold propagation delay, gate and input-offset test circuit with associated pulse wave forms.

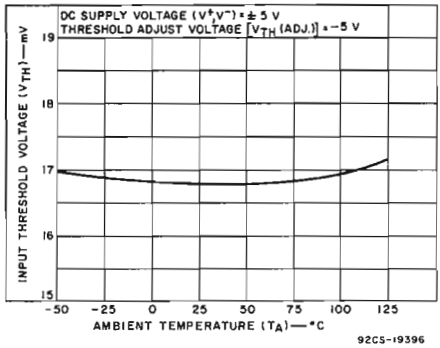


Fig. 7a – Input V_{TH} vs. T_A.

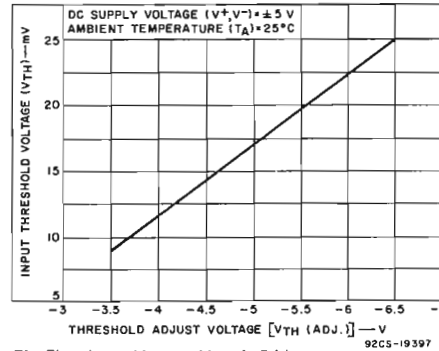


Fig. 7b – Input V_{TH} vs. V_{TH} (ADJ.).

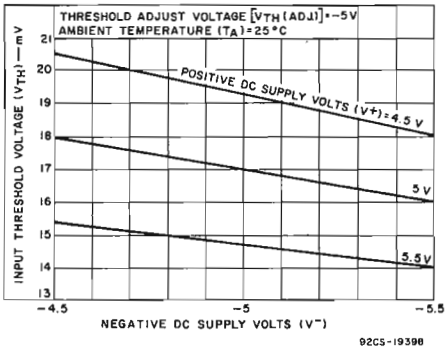


Fig. 7c – Input V_{TH} vs V^-.

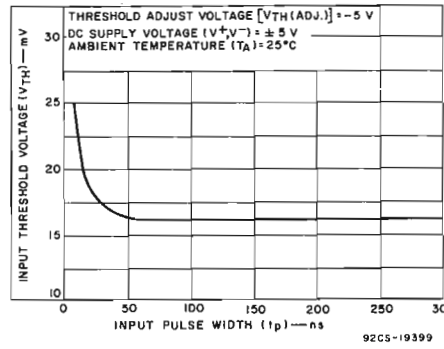
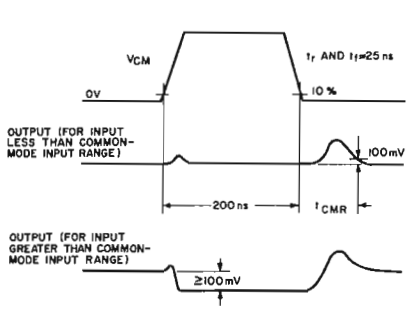


Fig. 7d – Input V_{TH} vs. input pulse width.



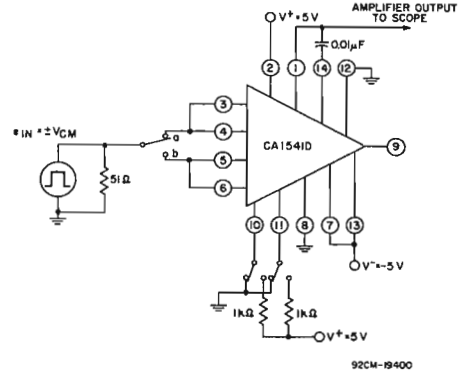


Fig. 8 – Common-mode input range test circuit with associated pulse wave forms.

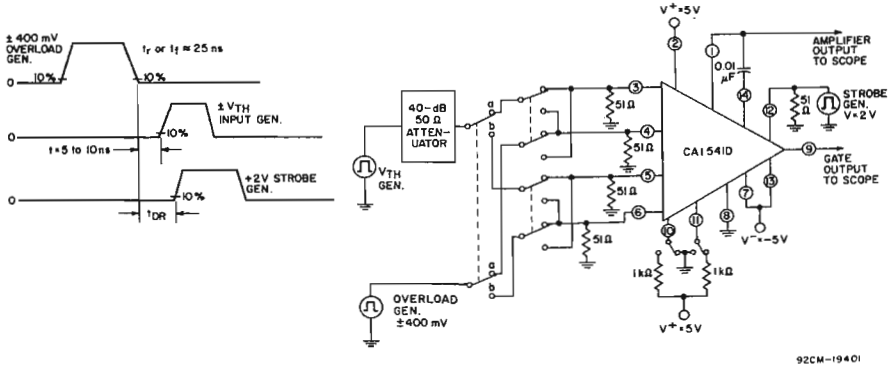


Fig. 9 – Differential-mode input range and recovery test circuit with associated pulse wave forms.

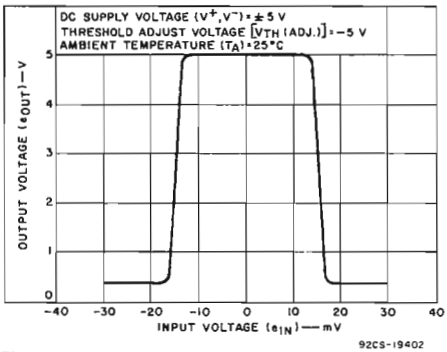


Fig. 10 – Input-output transfer characteristics.

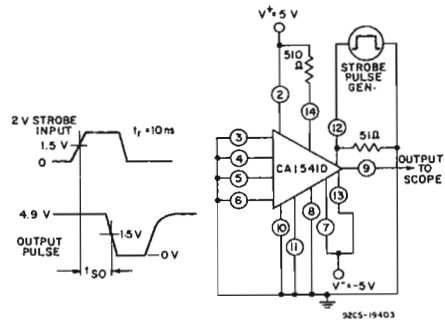
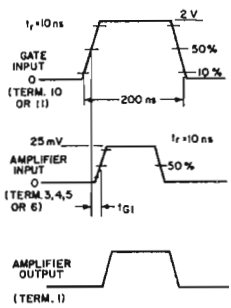
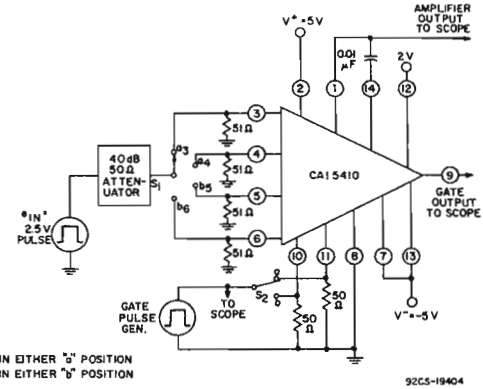


Fig. 11 – Strobe to output test circuit with associated pulse wave-forms.





NOTE: S_2 IN "a" POSITION WHEN S_1 IN EITHER "a" POSITION
S_2 IN "b" POSITION WHEN S_1 IN EITHER "b" POSITION

Fig. 12 – Gate input to amplifier input (t_{GI}) test circuit with associated pulse wave forms.

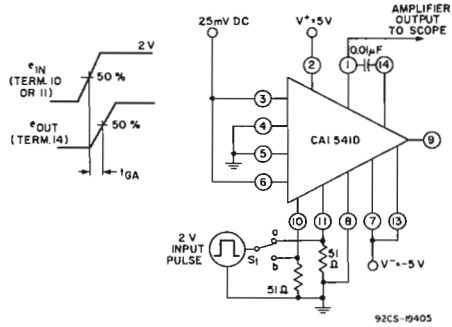


Fig. 13 – Gate input to amplifier output (t_{GA}) with associated pulse wave forms.

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Monolithic Silicon

CA2111AE
CA2111AQ

H-1517

14-Lead dual-in-line plastic package

H-1596

14-Lead quad-in-line plastic package

FM IF Amplifier-Limiter and Quadrature Detector

For FM IF and TV Sound IF Applications

Features:

- Direct replacement for ULN2111A and MC1357
- Good sensitivity: Input limiting voltage (knee) (400 μV typ. at 10.7 MHz; 250 μV typ. at 4.5 MHz and 5.5 MHz)
- Excellent AM rejection (45 dB typ. at 10.7 MHz)
- Provision for output from 3-stage IF amplifier section
- Low harmonic distortion
- Quadrature detection permits simplified single-coil tuning
- Extremely low AFC voltage drift over full operating-temperature range
- Minimum number of external parts required

The CA2111A, on a single monolithic chip, provides a multi-stage wideband amplifier-limiter, a quadrature detector, and an emitter-follower output stage. This device is designed for use in FM receivers and in the sound IF sections of TV receivers. In addition, an output terminal is provided which allows the use of the amplifier-limiter as a straight 60-dB wideband amplifier.

The amplifier-limiter features the excellent limiting characteristics of 3 cascaded differential amplifiers.

The quadrature detector requires only one coil in the associated outboard circuit and therefore, tuning is a simple procedure.

A unique feature of the CA2111A is its exceptionally low AFC voltage drift over the full operating-temperature range.

This device can be supplied in either dual-in-line or quad-in-line 14-lead plastic packages (CA2111AE and CA2111AQ, respectively).

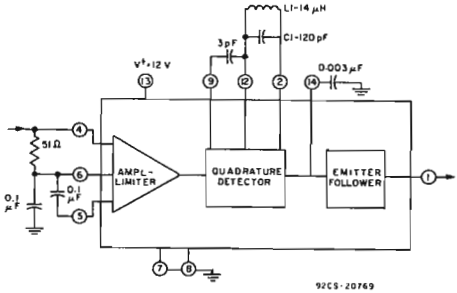


Fig. 1—Block diagram of CA2111A and associated outboard components.

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$

DC Supply Voltage [between terminals 13 (V^+) and 7 (V^-)]	16	V
Device Dissipation:		
Up to $T_A = 60°C$	600	mW
Above $T_A = 60°C$	derate linearly 6.7	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max.	+265	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
DC Voltage:		V^+ = 12V	–	5.4	–	V
At Terminal 1	V_1	= 8V	–	3.7	–	
At Terminals 4, 5, 6, 10	$V_{4,5,6,10}$	V^+ = 8V	–	1.35	–	
At Terminals 2, 12	$V_{2,12}$		–	3.5	–	
DC Current (into Terminal 13)						mA
At V^+ = 8V			–	14	–	
At V^+ = 12V	I_{13}		–	16	–	
Amplifier Input Resistance	R_4	f_o = 10.7 MHz	–	7	–	kΩ
Amplifier Input Capacitance	C_4		–	11	–	pF
Detector Input Resistance	R_{12}		–	70	–	kΩ
Detector Input Capacitance	C_{12}		–	2.7	–	pF
Amplifier Output Resistance	R_{10}		–	60	–	Ω
Detector Output Resistance	R_1		–	200	–	Ω
De-Emphasis Resistance	R_{14}		–	8.8	–	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C
FM Modulation Frequency = 400 Hz, Source Resistance = 50Ω

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						UNITS	TEST CIRCUIT OR CHARACTERISTIC CURVES FIG. NO.
		f_o = 10.7 MHz, Δf = ± 75 KHz				f_o = 4.5 MHz, Δf = ± 25 KHz	f_o = 5.5 MHz, Δf = ± 50 KHz		
		V^+ = 12V		V^+ = 8V		V^+ = 12V	V^+ = 12V		
		LIMITS							
		TYP.	MAX.	TYP.	MAX.	TYP. MAX.	TYP.	MAX.	
AMPL-LIMITER									
Input Limiting Threshold Voltage	V_i(lim) (4)	400	600	400	600	250 400	250	400	V (RMS)	3, 7, 8, 9
AM Rejection‡ *	AMR(1)	45	–	37	–	36 –	40	–	dB	3, 4, 5, 6
Ampl. Voltage Gain▲	A_V(10)	55	–	55	–	60 –	60	–	dB	3
DETECTOR									
Recovered Audio‡ Output Voltage	V_o(AF) (1)	0.48	–	0.3	–	0.72 –	1.2	–	V (RMS)	3, 7, 8, 9
Total Harmonic‡ Distortion	THD(1)	1	–	1	–	1.5 –	3	–	%	3

‡V_i = 10 mV (RMS) ▲$V_i \leq 50\ \mu V$ (rms) *100% FM, 30% AM

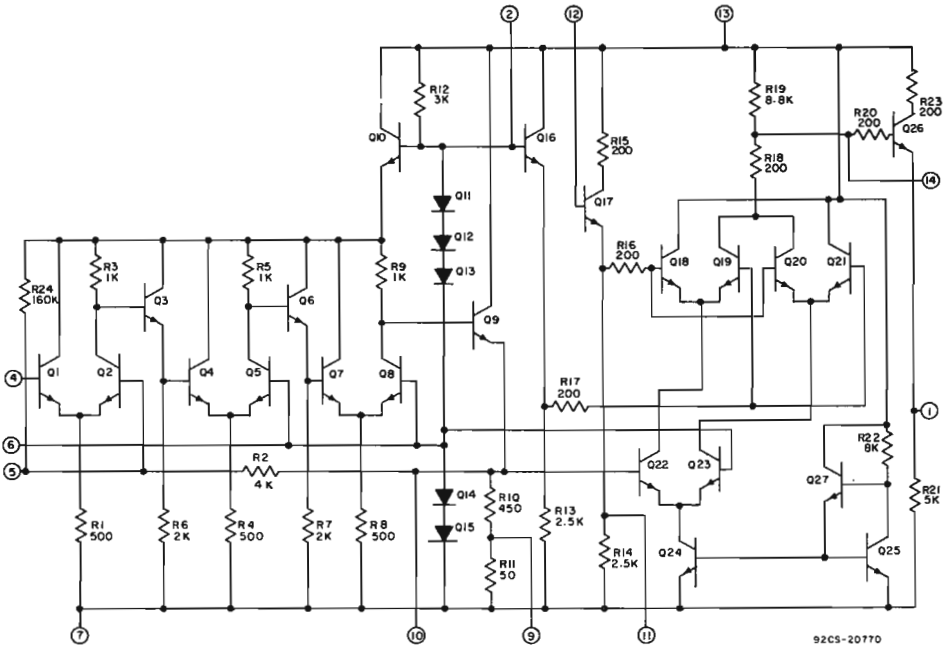
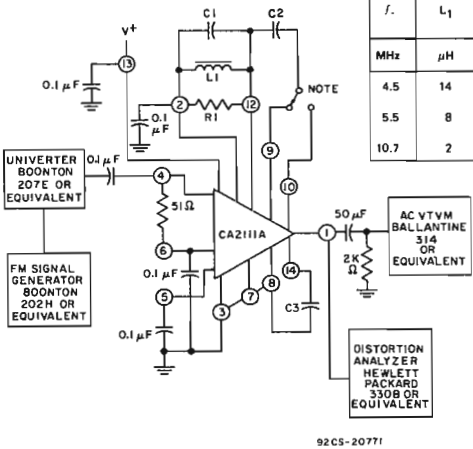


Fig. 2—Circuit schematic—CA2111A



COMPONENT VALUES							DETECTOR TRANSFER CHARACTERISTICS	
f_o	L_1	C_1	R_1	Q	C_2	C_3	UPPER PEAK	LOWER PEAK
MHz	μH	pF	KΩ	–	pF	μF	MHz	MHz
4.5	14	120	20	30	3	0.003	4.58	4.42
5.5	8	100	20	30	3	0.003	5.63	5.37
10.7	2	120	3.9	20	4.7	0.01	10.9	10.6

NOTE:
Input to the quadrature coil can be from either terminal 9 or terminal 10. Terminal 9 is normally used because it lessens the possibility of overloads during tuning. The use of terminal 10 increases the limiting sensitivity significantly and has been used successfully in these tests.

Fig. 3—Test circuit.

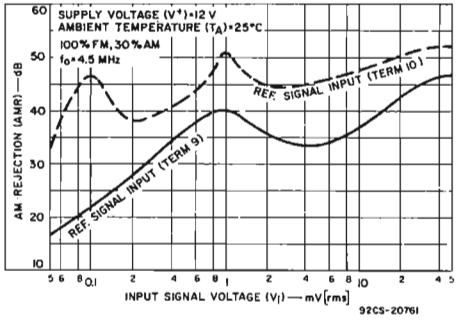


Fig. 4—AM rejection vs input voltage (4.5 MHz).

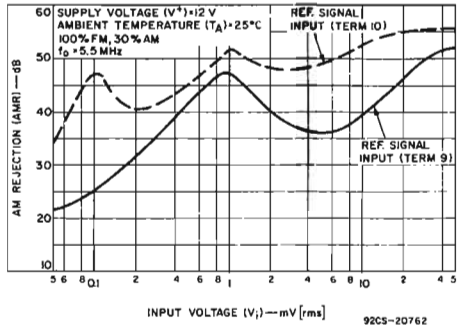


Fig. 5—AM rejection vs input voltage (5.5 MHz).

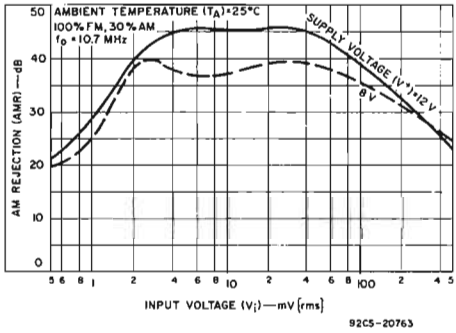


Fig. 6—AM rejection vs input voltage (10.7 MHz).

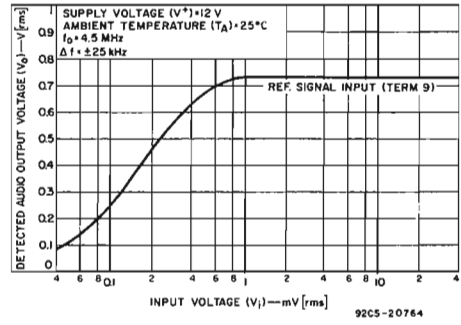


Fig. 7—Detected audio output vs input voltage (4.5 MHz).

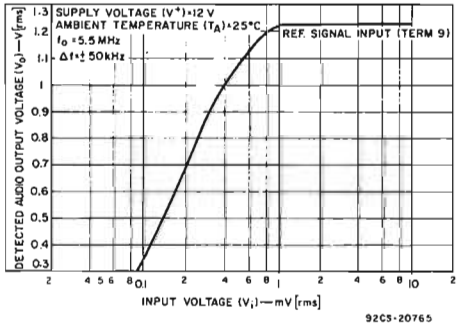


Fig. 8—Detected audio output vs input voltage (5.5 MHz).

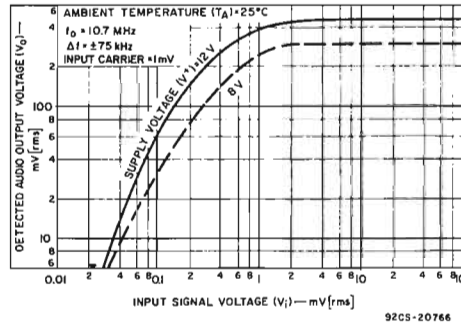


Fig. 9—Detected audio output voltage vs input voltage (10.7 MHz)

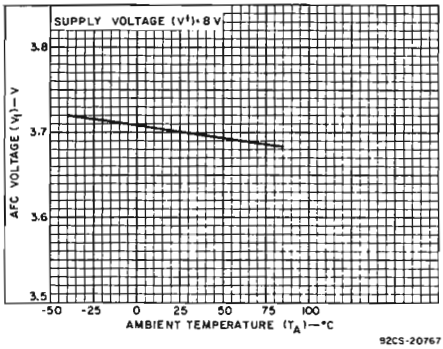


Fig. 10—AFC voltage vs ambient temp.

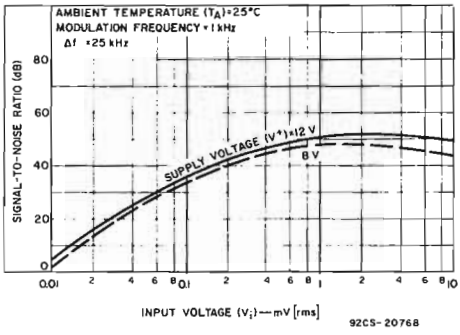


Fig. 11—Signal-to-noise ratio vs input voltage.

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CA3000

DC Amplifier

Monolithic Silicon

- Designed for use in Communication, Telemetry, Instrumentation, and Data-Processing Equipment
- Balanced differential-amplifier configuration with controlled constant-current source to provide outstanding versatility
- Built-in temperature stability for operation from -55°C to +125°C
- Companion Application Note, ICAN 5030 "Applications of RCA CA3000 Integrated Circuit DC Amplifier" covers characteristics of different operating modes, frequency considerations, 10 MHz narrow band tuned amplifier design, crystal oscillator design, and many other application aids

HIGHLIGHTS

- Input Impedance . . . . . 195 KΩ typ.
- Voltage Gain. . . . . 30 dB typ.
- Common-Mode Rejection Ratio . . . 98 dB typ.
- Input Offset Voltage. . . . . 1.4 mV typ.
- Push-Pull Input and Output
- Frequency Capability
  DC to 30 MHz (with external C and R)
- Wide AGC Range. . . . . 90 dB typ.

APPLICATIONS

- Schmitt Trigger
- RC-Coupled Feedback Amplifier
- Mixer
- Comparator
- Modulator
- Crystal Oscillator
- Sense Amplifier

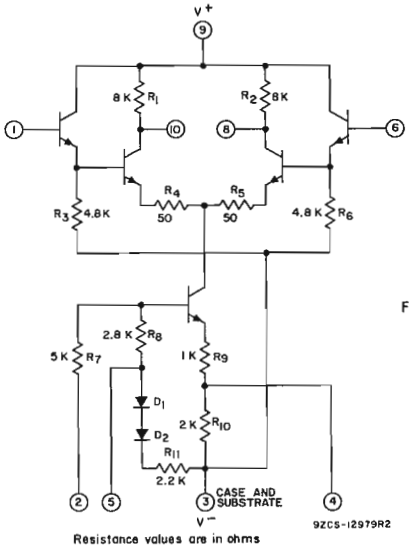


Fig. 1 SCHEMATIC DIAGRAM

Resistance values are in ohms

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Indicated voltage limits for each terminal can be used under specified voltage conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2	+2	2	0
			3	-6
			6	0
			9	+6
2	-8	0	1	0
			3	-8
			6	0
			9	+6
3	-10	0	1	0
			2	0
			6	0
			9	+6
4	-8	0	1	0
			2	0
			6	0
			9	+6
5	-6	0	1	0
			2	0
			3	-6
			6	0
			9	+6
6	-2	+2	1	0
			2	0
			3	-6
			9	+6
7	NO CONNECTION			
8	0	+6	1	0
			2	0
			3	-6
			6	0
9	0	+10	1	0
			2	0
			3	-6
			6	0
10	0	+6	1	0
			2	0
			3	-6
			6	0
CASE	Internally Connected to Terminal No. 3 (Substrate) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . −55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . −65°C to +150°C

LEAD-TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE . . ±4 V

MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE . . ±2 V

MAXIMUM DEVICE DISSIPATION:

From −55°C to 85°C. . . . . 450 mW

Above 85°C . . . . . Derate 5 mW/°C

STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3000

INPUT OFFSET VOLTAGE AND CURRENT vs TEMPERATURE

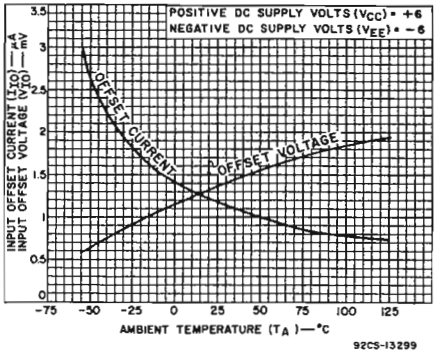


Fig. 2

INPUT BIAS CURRENT vs TEMPERATURE

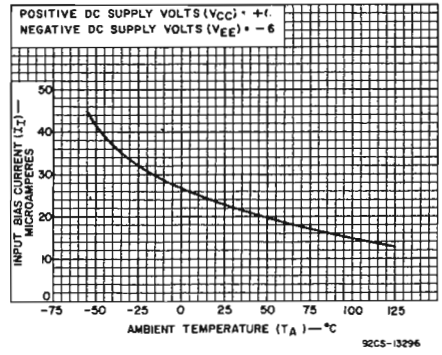


Fig. 3

ELECTRICAL CHARACTERISTICS, at T_{FA} = 25°C, V_{CC} = +6V, V_{EE} = -6V, unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 & No.5 Not Connected Unless Specified		TEST CIRCUITS	LIMITS TYPE CA3000				TYPICAL CHARACTERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}				-	1.4	5	mV	2
Input Offset Current	I_{IO}				-	1.2	10	μA	2
Input Bias Current	I_{IB}				-	23	36	μA	3
Quiescent Operating Voltage	V_8 or V_{IO}	TERMINALS							
		4	5						
		NC	NC		-	2.6	-	V	4
		NC	VEE		-	4.2	-	V	4
		VEE	NC		-	-1.5	-	V	4
		VEE	VEE		-	0.6	-	V	4
Device Dissipation	P_D	NC	NC		-	30	-	mW	NONE
DYNAMIC CHARACTERISTICS									
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single-Ended Output f = 1 kHz		9	28	32	-	dB	5
		Double-Ended Output f = 1 kHz		9	-	38	-	dB	5
Bandwidth at -3 dB Point	BW	V_I = 10 mV, R_s = 1 kΩ			-	650	-	kHz	7
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	f = 1 kHz		9	-	6.4	-	V(P-P)	NONE
Common-Mode Rejection Ratio	CMRR	f = 1 kHz		13	70	98	-	dB	8
Single-Ended Input Impedance	Z_{IN}	f = 1 kHz		15	70K	195K	-	Ω	10
Single-Ended Output Impedance	Z_{OUT}	f = 1 kHz		17	5.5K	8K	10.5K	Ω	12
Total Harmonic Distortion	THD	R_S=1kΩ f = 1 kHz V_O=42V_{p-p}			-	0.2	5	%	14
AGC Range (Maximum Voltage Gain to Complete Cutoff)	AGC	f = 1 kHz		20	80	90	-	dB	NONE

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

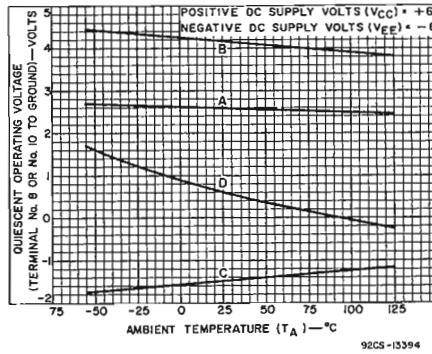


Fig.4

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT FOR TYPE CA3000

DIFFERENTIAL VOLTAGE GAIN vs TEMPERATURE

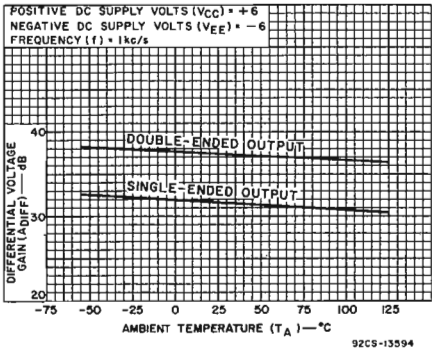


Fig.5

DIFFERENTIAL VOLTAGE GAIN AND MAXIMUM OUTPUT VOLTAGE SWING TEST CIRCUIT

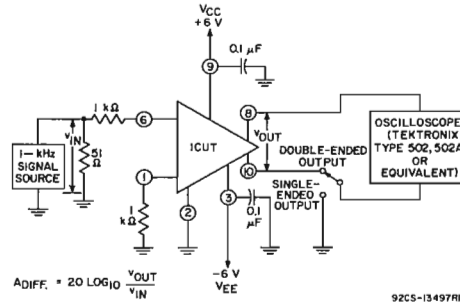


Fig.6

BANDWIDTH AT -3 dB POINT vs TEMPERATURE

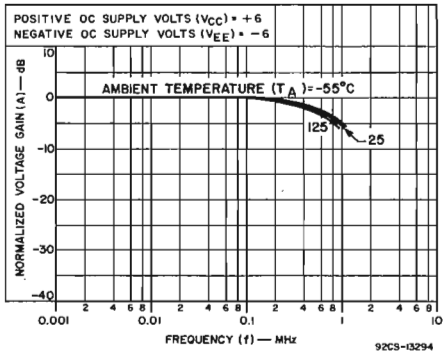


Fig.7

COMMON-MODE REJECTION RATIO vs TEMPERATURE

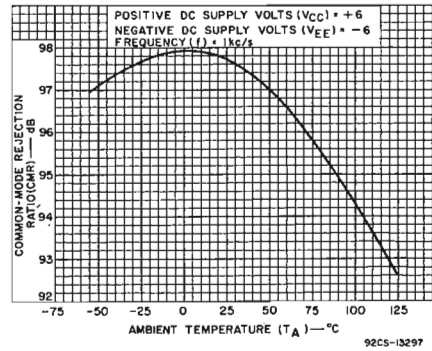
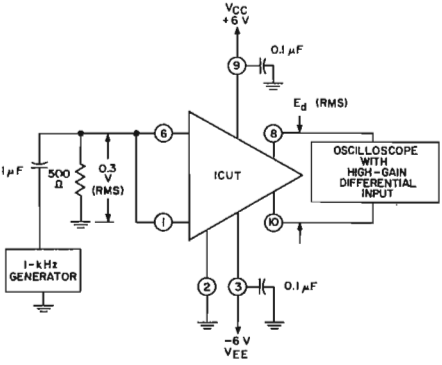


Fig.8

COMMON-MODE REJECTION RATIO TEST CIRCUIT



COMMON-MODE REJECTION RATIO (CMR) = 20 log $\frac{(A^*)(2)(0.3)}{E_d(RMS)}$

*A = SINGLE-ENDED VOLTAGE GAIN AS MEASURED IN CIRCUIT SHOWN IN FIG. 6B

92CS-12983R2

Fig.9

SINGLE-ENDED INPUT IMPEDANCE vs TEMPERATURE

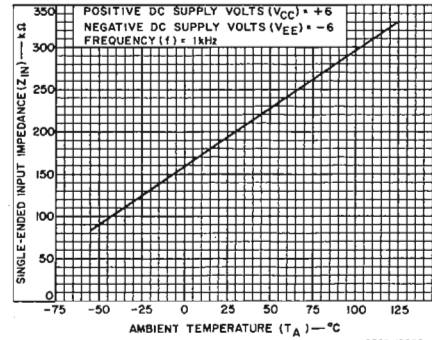


Fig.10

DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3000

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

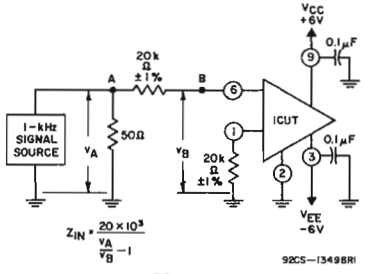


Fig. 11

SINGLE-ENDED OUTPUT IMPEDANCE vs TEMPERATURE

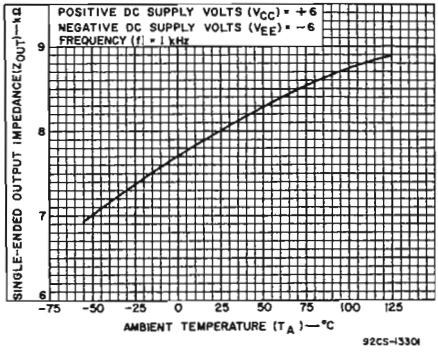


Fig. 12

SINGLE-ENDED OUTPUT IMPEDANCE TEST CIRCUIT

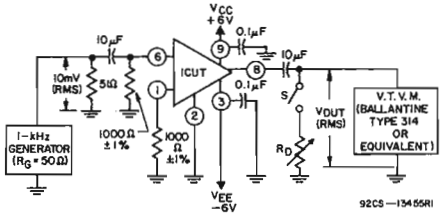


Fig. 13

TOTAL HARMONIC DISTORTION vs TEMPERATURE

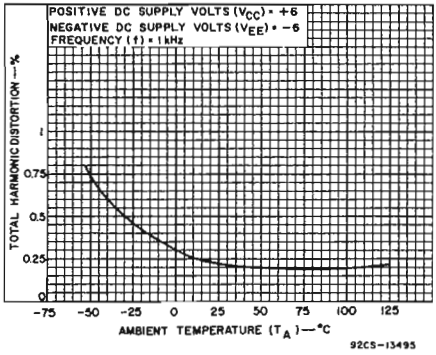


Fig. 14

AGC RANGE TEST CIRCUIT

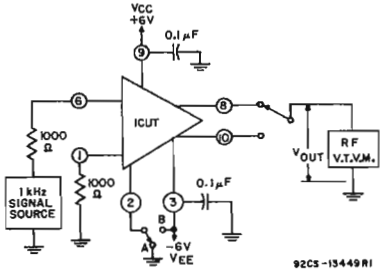


Fig. 15

RCA
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Linear Integrated Circuits

CA3001

Video and Wide-band Amplifier

Monolithic Silicon

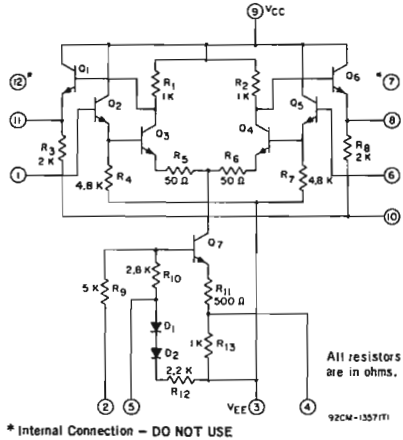
- Designed for use in Video Systems and Communication Equipment
- Balanced differential amplifier configuration with controlled constant-current source provides outstanding versatility
- Built-in temperature stability for operation from -55°C to +125°C
- Emitter follower input & output
- Companion Application Note ICAN5038 "Application of the RCA-CA3001 Integrated-Circuit Video Amplifier", covers different operating modes, gain control, distortion, swing capability, 3 stage amplifier design, and a Schmitt trigger study.

APPLICATIONS

- Schmitt Trigger
- Mixer
- Modulator
- DC, IF, & Video Amplifier

HIGHLIGHTS

- Push-Pull Input & Output
- AGC Range . . . . . 60 dB typ.
- Bandwidth. . . . . 29 MHz
- Input Resistance . . . . . 150 kΩ typ.
- Output Resistance . . . . . 45 Ω typ.
- Voltage Gain. . . . . 19 dB typ.
- Input Offset Voltage . . . . 1.5 mV typ.



* Internal Connection – DO NOT USE

Fig.1 - Schematic Diagram.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS at T_A = 25°C

Indicated voltage or current limits for each terminal can be applied under the specified conditions for other terminals. All Voltages are with respect to ground (common terminal of Positive and Negative DC Supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2, 6 3, 10 9	0 -6 +6
2	-8.5	0	1, 6 3, 10 9	0 -8.5 +6
3	-10	0	1, 2, 6 9 10	0 +6 -6
4	-8.5	0	1, 2, 6 9 10	0 +6 -6
5	-6	0	1, 2, 6 3, 10 9	0 -6 +6
6	-2.5	+2.5	1, 2 3, 10 9	0 -6 +6
7	INTERNAL CONNECTION DO NOT USE			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.8 & No.10	0 -6 +6
9	0	+10	1, 2, 6, 10 3	0 -6
10	-10	0	1, 2, 6 3 9	0 -6 +6
11	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.10 & No.11	0 -6 +6
12	INTERNAL CONNECTION DO NOT USE			
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

OPERATING TEMPERATURE RANGE	-55°C to +125°C
STORAGE TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	± 4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	± 2.5 V
MAXIMUM DEVICE DISSIPATION:	
-55 to 85°C	450 mW
Above 85°C	Derate linearly 5 mW/°C

ELECTRICAL CHARACTERISTICS, AT T_A = 25°C, V_{CC} = +6 V, V_{EE} = −6 V

CHARACTERISTICS (See Page 2 for Definitions of Terms)	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Not Connected Unless Specified	TEST CIRCUITS	LIMITS TYPE CA3001				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS:								
Input Offset Voltage	V_{IO}		4	-	1.5	-	mV	2
Input Offset Current	I_{IO}		5	-	1	10	μA	2
Input Bias Current	I_I		5	-	16	36	μA	3
Output Offset Voltage	V_{OO}	R_S = 1 kΩ		-	54	300	mV	6
Quiescent Operating Voltage	V_8 OR V_{11}	TERMINALS MODE A: 4 = NC, 5 = NC		3.8	4.4	5	V	7
		MODE B: 4 = NC, 5 = V_{EE}		-	4.8	-	V	7
		MODE C: 4 = V_{EE}, 5 = NC		-	2.7	-	V	7
		MODE D: 4 = V_{EE}, 5 = V_{EE}		-	4	-	V	7
Device Dissipation	P_D	A: 4 = NC, 5 = NC		60	78	120	mW	8
		B: 4 = NC, 5 = V_{EE}		-	71	-	mW	8
		C: 4 = V_{EE}, 5 = NC		-	110	-	mW	8
		D: 4 = V_{EE}, 5 = V_{EE}		-	86	-	mW	8
DYNAMIC CHARACTERISTICS:								
Differential Voltage Gain (Single-ended input and output)	A_{DIFF}	f = 1.75 MHz f = 20 MHz		16 10	19 14	- -	dB dB	9 A, 9 B 9 B
Bandwidth at -3 dB Point	BW	R_S = 50Ω		16	29	-	MHz	NONE
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	R_S = 50Ω f = 1.75 MHz		-	5	-	V_{P-P}	NONE
Noise Figure	NF_I	f = 1.75 MHz, R_S = 1 KΩ	14	-	5	8	dB	10
		f = 11.7 MHz, R_S = 1 KΩ	14	-	7.7	-	dB	10
Common-Mode Rejection Ratio	CMRR	f = 1 KHz	16	70	88	-	dB	12
Input Impedance Components:								
Parallel Input Resistance	R_{IN}	f = 1.75 MHz		50	140	-	KΩ	14
Parallel Input Capacitance	C_{IN}	f = 1.75 MHz		-	3.4	7	pF	14
Output Resistance	R_{OUT}	f = 1.75 MHz		-	45	70	Ω	NONE
AGC Range (Maximum voltage gain to complete cutoff)	AGC	f = 1.75 MHz	19	55	60	-	dB	NONE

TYPICAL STATIC CHARACTERISTICS

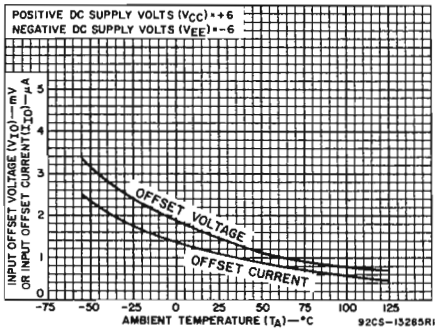


Fig.2 - Input offset voltage and current vs. temperature.

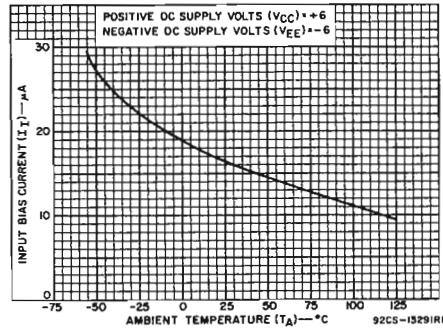
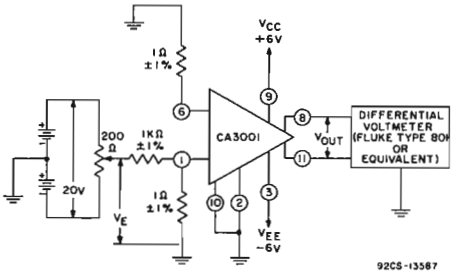


Fig.3 - Input bias current vs. temperature.

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS



1. Adjust V_E for $V_{OUT(DC)} = 0 \pm 0.1$ V 2. Measure V_E and record input offset voltage (V_{IO}) in mV as $V_{IO} = \frac{V_E}{1000}$

Fig.4 - Input offset voltage test circuit.

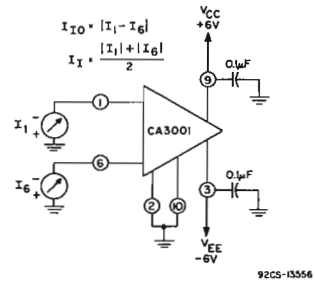


Fig.5 - Input offset current and input bias current test circuit.

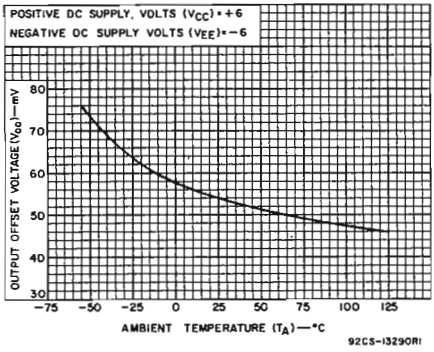


Fig.6 - Output offset voltage vs. temperature.

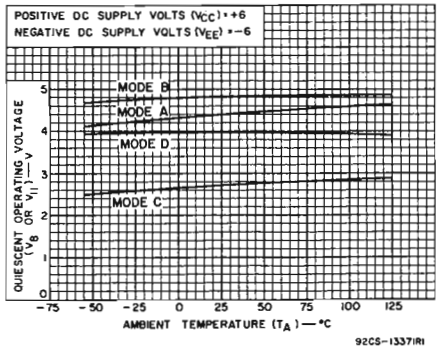


Fig.7 - Quiescent operating voltage vs. temperature.

TYPICAL STATIC CHARACTERISTICS

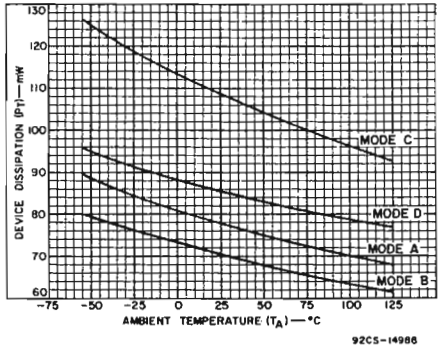


Fig.8 - Device dissipation vs. temperature.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

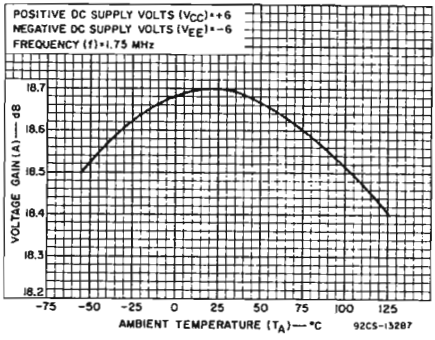


Fig.9a - Differential voltage gain vs. temperature.

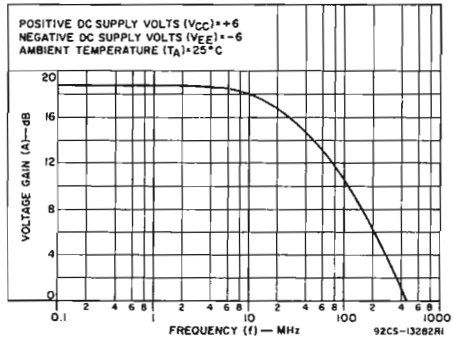


Fig.9b - Differential voltage gain vs. frequency.

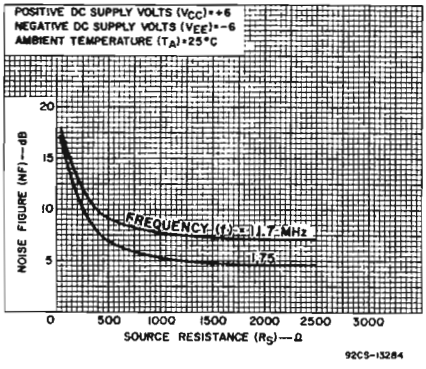
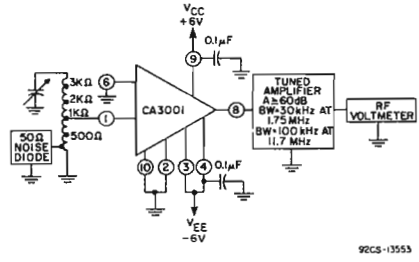


Fig.10 - Noise figure vs. source resistance and frequency.



* Separate tuned input circuits are used for 1.75 MHz and 11.7 MHz. Source-resistance matching taps adjusted with circuit tuned to resonance and with 50-ohm resistor connected to simulate noise diode.

Fig.11. Noise figure test circuit.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUIT

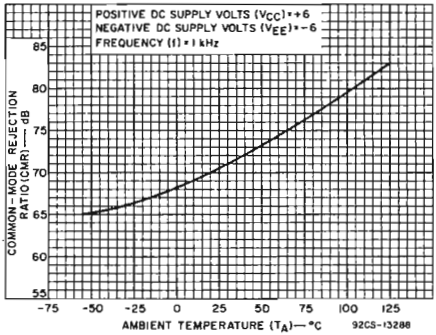


Fig.12 - Common-mode rejection ratio vs. temperature.

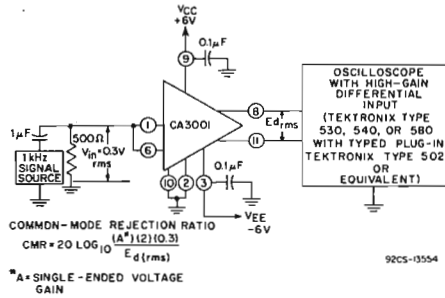


Fig.13 - Common-mode rejection ratio test circuit.

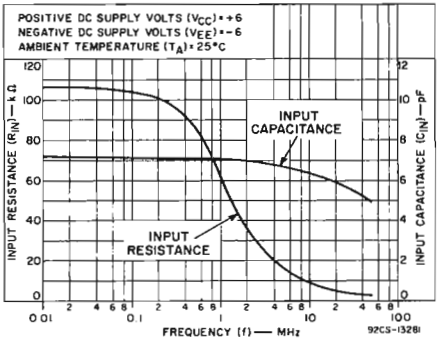


Fig.14 - Input impedance components vs. frequency.

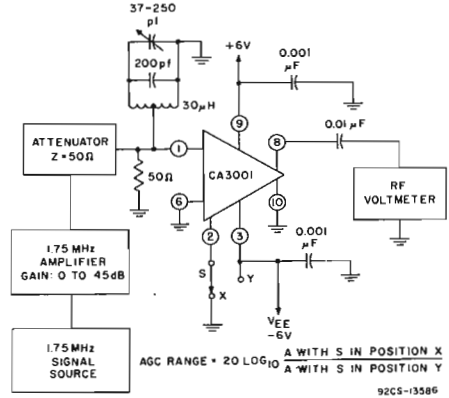


Fig.15 - AGC range test circuit.

RCA
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CA3002

IF Amplifier

- Designed for use in Communication Equipment
- Balanced differential amplifier configuration with controlled constant-current source provides outstanding versatility
- Built-in temperature stability for operation from -55°C to +125°C
- Companion Application Note ICAN-5036 "Application of the RCA-3002 Integrated-Circuit IF Amplifier" covers different operating modes, cross modulation, gain control, 4-stage amplifier design, and an envelope and product detector analysis.

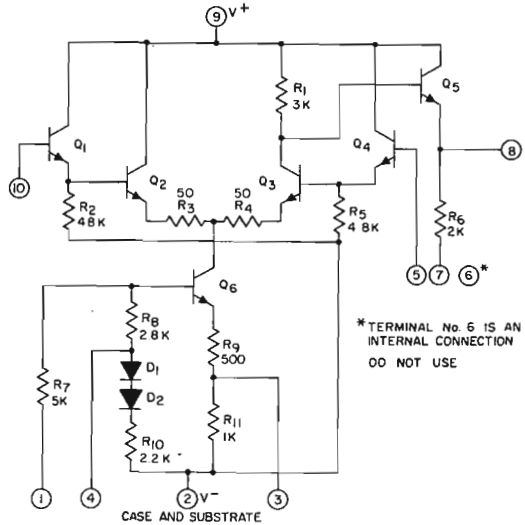
APPLICATIONS

- Product Detector
- AM Detector
- IF & Video Amplifier
- Schmitt Trigger

HIGHLIGHTS

- Input Resistance . . . . . 100 kΩ typ.
- Output Resistance . . . . . 70 Ω typ.
- Voltage Gain . . 24 dB typ. @ 1.75 MHz
- Push-Pull Input, Single-Ended Output
- -3 dB Bandwidth . . . . . 11 MHz typ.
- AGC Range . . . . . 80 dB typ.
- Useful Frequency Range DC to . . 15 MHz

SCHEMATIC DIAGRAM



ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, at $T_A = 25^oC$

Indicated voltage or current limits for each terminal can be applied under the specified operating conditions for other terminals.

All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$,)or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-8 V	0 V	2, 7 5, 10 9	-8 0 +6
2	-10 V	0 V	1, 5, 10 9	0 +6
3	-8.5 V	0 V	1, 5, 10 7 9	0 -6 +6
4	-8 V	0 V	1, 5, 10 2, 7 9	0 -8 +6
5	-3.5 V	+3.5 V	1, 10 2, 7 9	0 -6 +6
CASE	INTERNALLY CONNECTED TO TERMINAL No.2 (SUBSTRATE) DO NOT GROUND			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
6	INTERNAL CONNECTION DO NOT USE			
7	-12 V	0 V	1, 5, 10 2 9	0 -6 +6
8	20 mA		1, 5, 7, 10 2 9 200 Ω Resistor Between Terminals 7 & 8	0 -6 +6
9	0 V	+10 V	1, 5, 10 2, 3, 7	0 -6
10	-3.5 V	+3.5 V	1, 5 2, 7 9	0 -6 +6

OPERATING-TEMPERATURE RANGE ..... -55^oC to $+125^oC$

STORAGE-TEMPERATURE RANGE ..... -65^oC to $+150^oC$

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)

from case for 10 seconds max. ..... $+265^oC$

MAXIMUM INPUT-SIGNAL VOLTAGE ..... ± 4 V

MAXIMUM DEVICE DISSIPATION:

-55 to 85^oC ..... 450 mW

Above 85^oC ..... Derate linearly 5 mW/^oC

STATIC CHARACTERISTICS AND TEST CIRCUITS

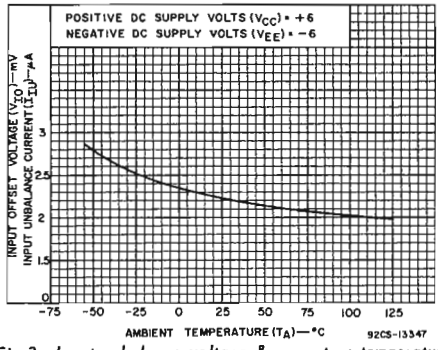


Fig.2 - Input unbalance voltage & current vs temperature.

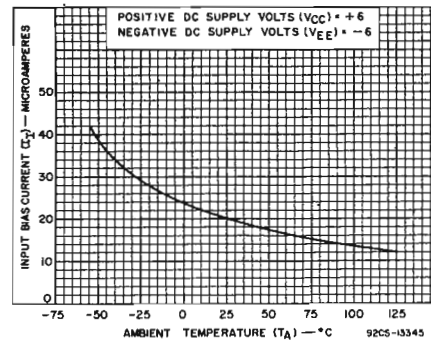


Fig.3 - Input bias current vs temperature.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V_{CC} = +6 V, V_{EE} = -6 V

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS TERMINALS No.3 & No.4 NOT CONNECTED UNLESS OTHERWISE NOTED	TEST CIRCUITS	LIMITS CA3002				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS:								
Input Offset Voltage	V_{IO}		4	-	2.2	-	mV	2
Input Unbalance Current	I_{IU}			-	2.2	10	μA	2
Input Bias Current	I_I			-	20	36	μA	3
Quiescent Operating Voltage		MODE / TERMINAL 2 / TERMINAL 4						
		A / V_{EE} / NC		-	2.8	-	V	4
		B / V_{EE} / V_{EE}		-	3.9	-	V	4
Device Dissipation	P_T			-	55	-	mW	None
DYNAMIC CHARACTERISTICS:								
Differential Voltage Gain (Single-Ended Input and Output)	A_{DIFF}	V_{IN} = 10 mV, f = 1.75 MHz, R_S = 50Ω		19	24	-	dB	5 & 15
Bandwidth at -3 dB Point	BW	R_S = 50Ω, V_{IN} = 10 mV		-	11	-	MHz	6
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	-		-	5.5	-	V_{P-P}	None
Noise Figure	NF	f = 1.75 MHz R_S = 1 kΩ	12	-	4	8	dB	7
Input Impedance Components: Parallel Input Resistance	R_{IN}	f = 1.75 MHz	None	-	100k	-	Ω	None
Parallel Input Capacitance	C_{IN}	f = 1.75 MHz	None	-	4	-	pF	None
Output Resistance	R_{OUT}	f = 1.75 MHz	14	-	70	-	Ω	9a & 9b
AGC Range (Maximum Voltage Gain to Complete Cutoff	AGC	f = 1.75 MHz	18	60	80	-	dB	12

STATIC CHARACTERISTICS AND TEST CIRCUITS

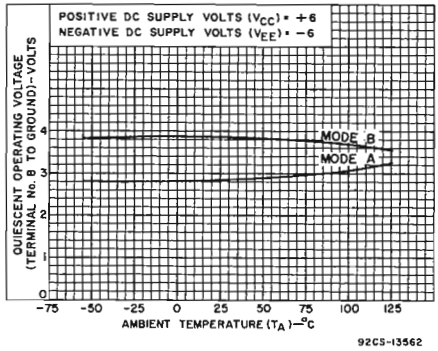


Fig.4 – Quiescent operating voltage vs temperature.

DYNAMIC CHARACTERISTICS

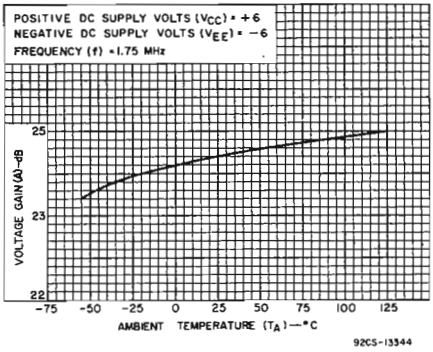


Fig. 5a - Differential voltage gain vs temperature.

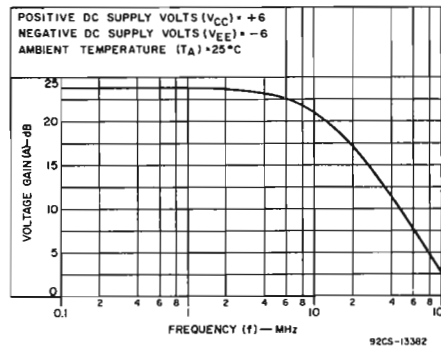


Fig. 5b - Differential voltage gain vs frequency.

DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

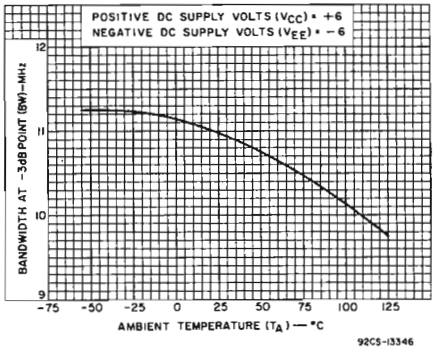


Fig. 6 - Bandwidth at -3 dB point vs temperature.

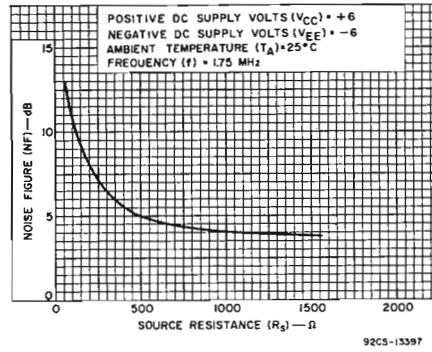
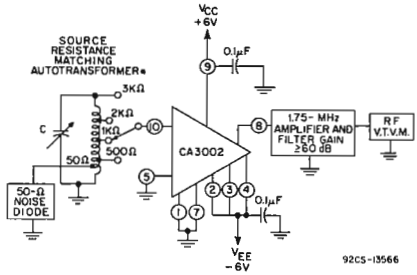


Fig. 7 - Noise figure vs source resistance.



*Taps are adjusted to provide indicated equivalent values of R_S with tank tuned to resonance at 1.75 MHz, and a 50-Ω resistor connected to simulate the noise diode.

Fig. 8 - Noise figure.

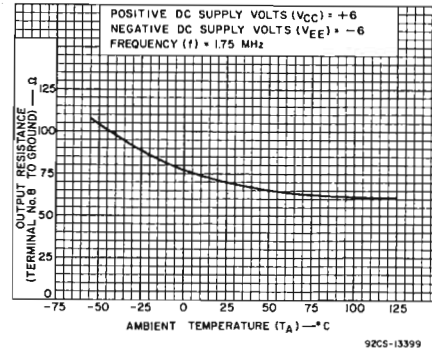


Fig. 9a - Output resistance vs temperature.

DYNAMIC CHARACTERISTIC AND TEST CIRCUIT

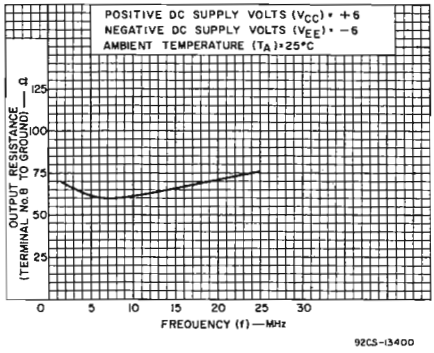


Fig. 9b - Output resistance vs frequency.

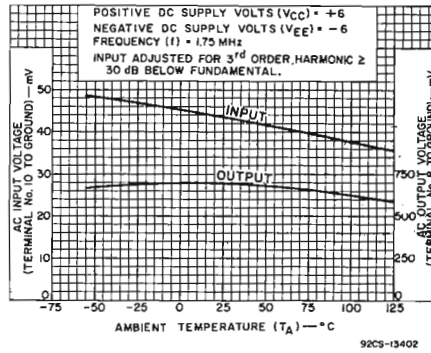
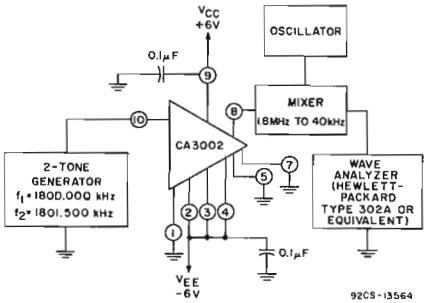


Fig. 10 - Input level for − 30 dB intermodulation vs. temperature



1) Increase both input-signal tones until the $2f_2$-$f1$ and $2f_1$-$f2$ output-signal voltages are 30 dB below the f_1 and f_2 output-signal voltages.
2) Measure rms values of the input and output signal voltages.
3) The measured input signal voltage is that value when the 3rd-harmonic intermodulation products are 30 dB below the fundamental outputs.

Fig. 11 - Intermodulation Test Circuit.

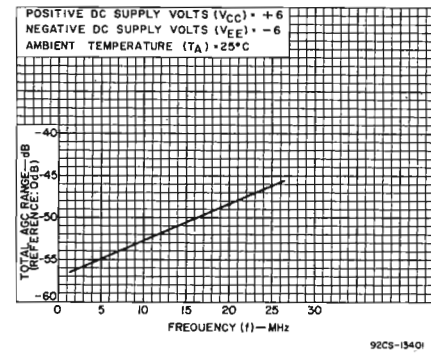


Fig. 12 - AGC range vs frequency.

1) Set attenuator at 80 dB attenuation.
2) Set variable dc supply voltage at 0 V.
3) Increase signal input voltage until RF V.T.V.M. indicates 5 mV output.
4) Set variable dc supply voltage at -6 V.
5) Adjust attenuator until RF V.T.V.M. again indicates 5 mV output.
6) Change in attenuator setting in dB is total AGC Range.

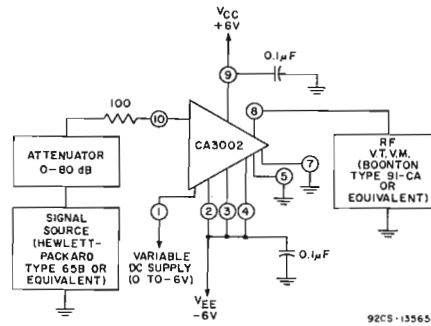


Fig. 13 - AGC range.

RCA
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Linear Integrated Circuits

CA3004

RF Amplifier

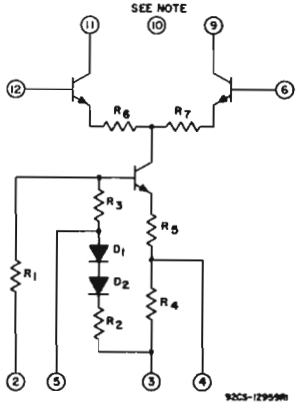
Monolithic Silicon

- Designed for use in Communications Equipment
- Balanced Differential-Amplifier Configuration with Controlled Constant-Current Source Provides Unexcelled Versatility

- Push-Pull Input and Output
- Wide and Narrow-Band Amplifier
- AGC
- Detector
- Operation from DC to 100 Mc/s
- Mixer
- Limiter
- Modulator
- RF, IF, and Video Frequency Capability

- Built-in Temperature Stability for Operation from -55° C to +125° C
- Similar to RCA CA3005 and CA3006, plus Emitter-Degeneration Resistors to Provide More Linear Transfer Characteristic and Increased Input-Signal Handling Capability
- Companion Application Note ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC, limiter, detector, and amplifier design considerations.

SCHEMATIC DIAGRAM FOR CA3004



NOTE: Connect Terminal No. 10 to most positive dc supply voltage used for circuit.

Fig. 1

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated circuit conditions for other terminals. All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	NO CONNECTION			
2	-9.5	0	6	0
			12	0
			3	-9.5
			9	+6
			10	+6
			11	+6
3	-12	0	2	0
			6	0
			9	+6
			10	+6
			11	+6
			12	0
4	-12	0	2	0
			6	0
			9	+6
			10	+6
			11	+6
			12	0
5	-6	0	2,6,12	0
			3	-6
			9	+6
			10	+6
			11	+6
6	-3.5	+3.5	2	0
			3	-6
			9	+6
			10	+6
			11	+6
			12	0

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
7	NO CONNECTION			
8	NO CONNECTION			
9	0	+12	2	0
			3	-6
			6	0
			10	+6
			11	+6
			12	0
10	0	+12	2	0
			3	-6
			6	0
			9	+6
			11	+6
			12	0
11	0	+12	2	0
			3	-6
			6	0
			10	+6
			11	+6
			12	0
12	-3.5	+3.5	2	0
			3	-6
			6	0
			9	+6
			10	+6
			11	+6
CASE	INTERNALLY CONNECTED TO TERMINAL NO.3 (SUBSTRATE) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±3.5 V

MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . -2.5 V, +3.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

ELECTRICAL CHARACTERISTICS, at $T_{FA} = 25^0$ C, $V_{CC} = +6V$, $V_{EE} = -6$ V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Open Unless Otherwise Specified		TEST CIRCUIT	LIMITS TYPE CA3004				TYPICAL CHARACTERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}			Fig.4	–	1.7	5	mV	Fig.2
Input Offset Current	I_{IO}			Fig.5	–	0.125	5	μA	Fig.2
Input Bias Current	I_I			Fig.5	–	21	40	μA	Fig.3
Quiescent Operating Current	I_9 or I_{11}	TERMINALS 4	5						
		NC	NC	Fig.8	–	1	–	mA	Fig.6
		V_{EE}	NC	Fig.8	–	2.7	–	mA	Fig.6
		NC	V_{EE}	Fig.8	–	0.45	–	mA	Fig.6
		V_{EE}	V_{EE}	Fig.8	–	1.25	–	mA	Fig.6
Quiescent Operating Current Ratio	I_9/I_{11}			Fig.8	–	1.1	–	–	Fig.7
Device Dissipation	P_T			Fig.8	–	26	–	mW	NONE
DYNAMIC CHARACTERISTICS									
Power Gain	G_P	f = 100 Mc/s		Fig.11	10	12	–	dB	Fig.9
Noise Figure	NF	f = 100 Mc/s		Fig.11	–	6.3	9	dB	Fig.10
Common Mode Rejection Ratio	CMR	f = 1 Kc/s		Fig.13	–	98	–	dB	Fig.12
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 Mc/s		Fig.14	-60	–	–	dB	NONE

DEFINITIONS OF TERMS

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

Quiescent Operating Current Ratio

The ratio of the Quiescent operating currents in the two output terminals.

Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Common-Mode Rejection Ratio

The ratio of the full differential voltage gain to the common-mode voltage gain.

Common-Mode Voltage Gain

The ratio of the signal voltages developed between the two output terminals to the signal voltage applied to the two input terminals connected in parallel for ac.

Differential Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3004

INPUT OFFSET VOLTAGE AND CURRENT VS TEMPERATURE

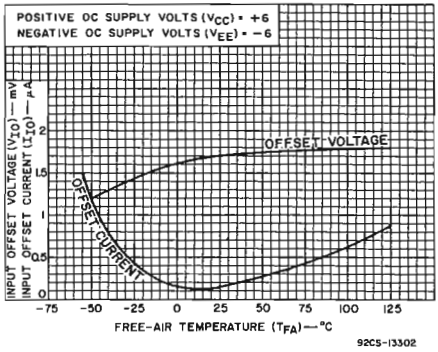


Fig.2

INPUT BIAS CURRENT VS TEMPERATURE

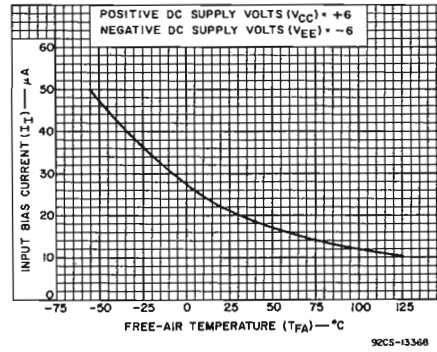


Fig.3

INPUT OFFSET VOLTAGE TEST CIRCUIT

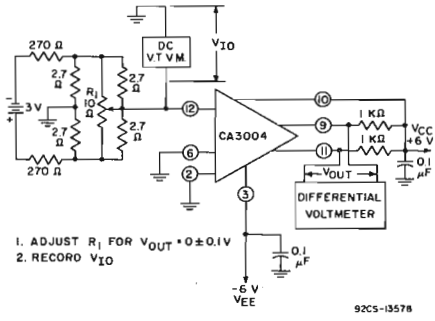


Fig.4

INPUT OFFSET CURRENT AND BIAS CURRENT TEST CIRCUIT

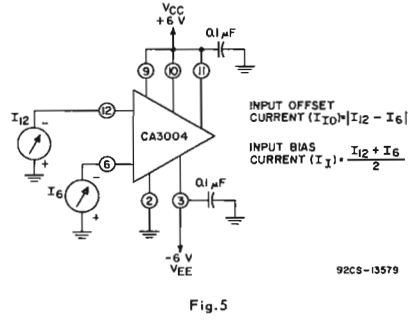


Fig.5

QUIESCENT OPERATING CURRENT VS TEMPERATURE

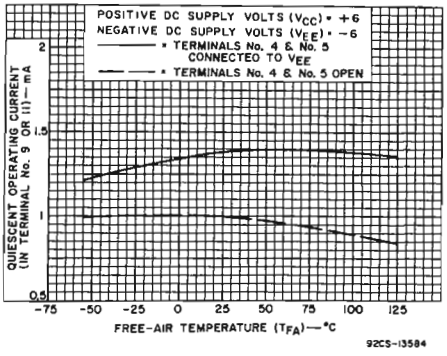


Fig.6

QUIESCENT OPERATING CURRENT RATIO VS TEMPERATURE

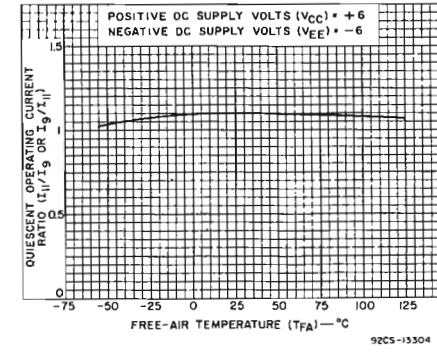
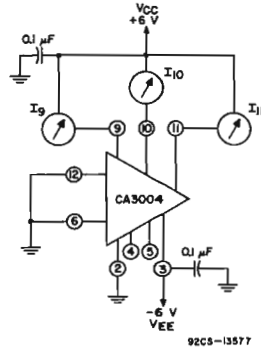


Fig.7

TEST CIRCUIT FOR TYPE CA3004

QUIESCENT OPERATING CURRENT, QUIESCENT OPERATING CURRENT RATIO, AND DEVICE DISSIPATION TEST CIRCUIT



$$P_T = V_{CC}(I_9 + I_{10} + I_{11}) + V_{EE} I_3$$

Fig.8

TYPICAL DYNAMIC CHARACTERISTICS FOR TYPE CA3004

POWER GAIN VS FREQUENCY

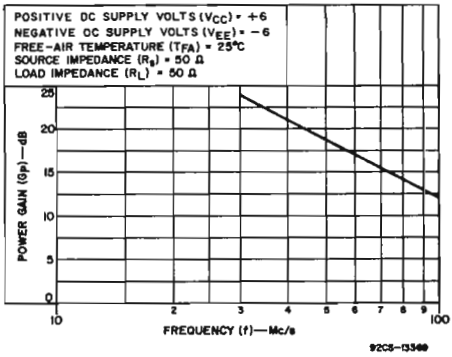


Fig.9

NOISE FIGURE VS FREQUENCY

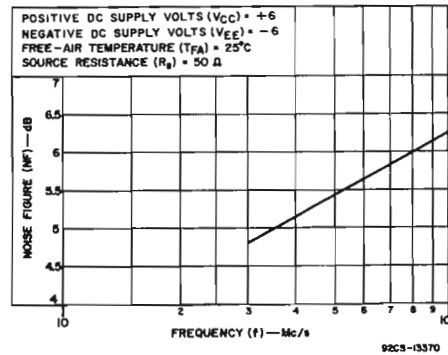


Fig.10

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3004

100 Mc/s POWER GAIN AND NOISE FIGURE TEST CIRCUIT

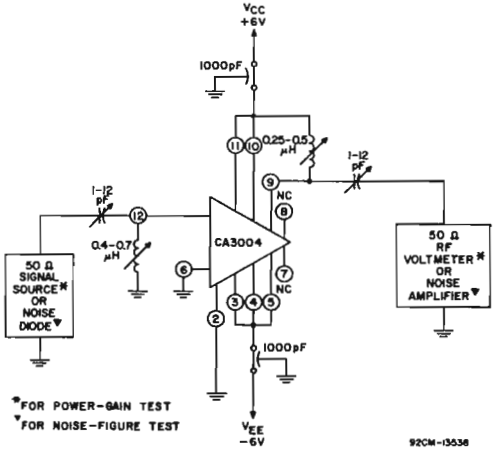


Fig. 11

COMMON-MODE REJECTION RATIO VS TEMPERATURE

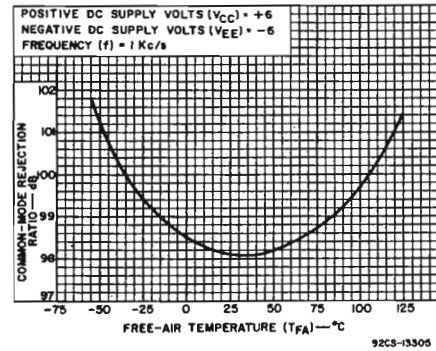


Fig. 12

COMMON-MODE REJECTION RATIO TEST CIRCUIT

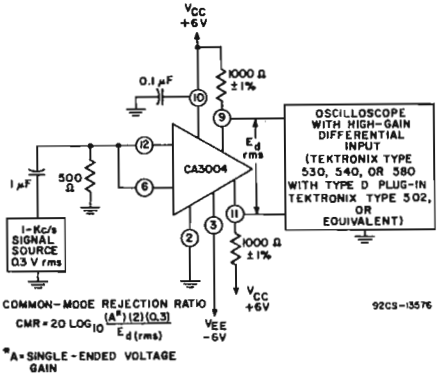


Fig. 13

AGC RANGE TEST CIRCUIT

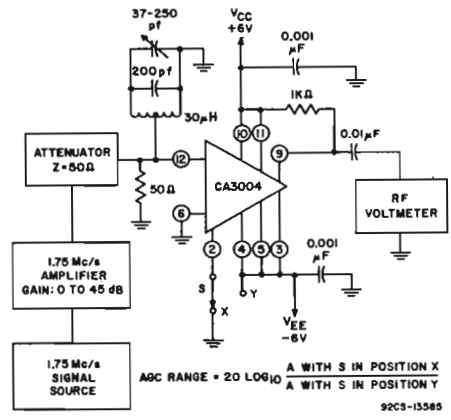


Fig. 14

RCA
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Linear Integrated Circuits

CA3005
CA3006

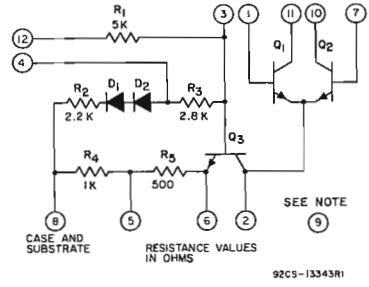
RF Amplifiers
Monolithic Silicon

- Designed for use in Communications Equipment
- Balanced Differential Amplifier Configuration with Controlled Constant-Current Source to Provide Unexcelled Versatility

- Push-Pull Input and Output
- Wide and Narrow Band Amplifier
- AGC
- Detector
- RF, IF, and Video Frequency Capability
- Operation from DC to 100 MHz
- Mixer
- Limiter
- Modulator
- Cascode Amplifier

- Built-in Temperature Stability for Operation from -55° C to +125° C
- Companion Application Note, ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC limiter, detector, and amplifier design considerations.

SCHEMATIC DIAGRAM FOR CA3005 AND CA3006



NOTE: Connect Terminal No.9 to most positive dc supply voltage used for circuit.

Fig.1

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated voltage conditions for other terminals.
All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3.5	+3.5	7	0
			8	-6
			9	+6
			10	+6
			11	+6
			12	0
2	TEST POINT: DO NOT APPLY VOLTAGE FROM EXTERNAL SOURCE			
3	-9.5	0	1	0
			7	0
			8	-9.5
			9	+6
			10	+6
			11	+6
			12	0
4	-6	0	1	0
			7	0
			8	- 6
			9	+6
			10	+6
			11	+6
			12	0
5	-12	0	1	0
			7	0
			9	+6
			10	+6
			11	+6
			12	0
6	-6	0	1	0
			7	0
			9	+6
			10	+6
			11	+6
			12	-6
7	-3.5	+3.5	1	0
			8	-6
			9	+6
			10	+6
			11	+6
			12	0

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	-12	0	1	0
			7	0
			9	+6
			10	+6
			11	+6
			12	0
9	0	+12	1	0
			7	0
			8	-6
			10	+6
			11	+6
			12	0
10	0	+12	1	0
			7	0
			8	-6
			9	+6
			11	+6
			12	0
11	0	+12	1	0
			7	0
			8	-6
			9	+6
			10	+6
			12	0
12	-9.5	0	8	-9.5
			9	+6
			10	+6
			11	+6
CASE	Internally connected to Terminal No.8 (substrate) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±3.5 V

MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . -2.5 V, +3.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, V_{CC} = +6V, V_{EE} = -6V

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.3,4,5, and 6 Not Connected Except Where Noted	TEST CIRCUITS	LIMITS TYPE CA3005 Min.	Typ.	Max.	LIMITS TYPE CA3006 Min.	Typ.	Max.		TYPICAL CHARACTERISTICS CURVES
			Fig.								Fig.
STATIC CHARACTERISTICS											
Input Offset Voltage	V_{IO}		Fig.3	–	2.6	5	–	0.8	1	mV	Fig.2
Input Offset Current	I_{IO}		Fig.4	–	1.4	–	–	1.4	–	μA	Fig.2
Input Bias Current	I_{IB}		Fig.4	–	19	40	–	19	40	μA	Fig.5
Quiescent Operating Current	I_{10} or I_{11}	TERMINALS 4: NC	Fig.8	–	1	–	–	1	–	mA	Fig.6
		TERMINALS 4: NC, 5: -V_{EE}	Fig.8	–	2.7	–	–	2.7	–	mA	NONE
		TERMINALS 4: -V_{EE}, 5: NC	Fig.8	–	0.45	–	–	0.45	–	mA	NONE
		TERMINALS 4: -V_{EE}, 5: -V_{EE}	Fig.8	–	1.25	–	–	1.25	–	mA	Fig.6
Quiescent Operating Current Ratio	$\frac{I_{10}}{I_{11}}$		Fig.8	–	1.05	–	–	1.05	–	–	Fig.7
Device Dissipation	P_T		Fig.8	–	26	–	–	26	–	mW	NONE
DYNAMIC CHARACTERISTICS											
Power Gain	G_p	f = 100 MHz, Cascode Configuration	Fig.10	16	20	–	16	20	–	dB	Fig.9
		f = 100 MHz, Differential-Ampl. Configuration	Fig.12	14	16	–	14	16	–	dB	Fig.11
Noise Figure	NF	f = 100 MHz, Cascode Configuration	Fig.10	–	7.8	9	–	7.8	9	dB	Fig.13
		f = 100 MHz, Differential Ampl. Configuration	Fig.12	–	7.8	9	–	7.8	9	dB	Fig.14
Common-Mode Rejection Ratio	CMR	f = 1 kHz	Fig.16	–	101	–	–	101	–	dB	Fig.15
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 MHz	Fig.17	-60	–	–	-60	–	–	dB	NONE

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA3005 AND CA3006

INPUT OFFSET VOLTAGE AND CURRENT

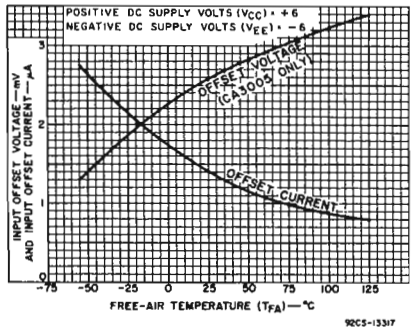


Fig.2

INPUT OFFSET VOLTAGE TEST CIRCUIT

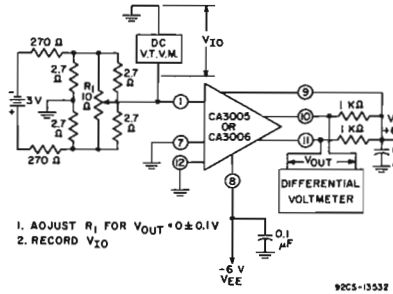


Fig.3

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA3005 AND CA3006

INPUT BIAS CURRENT

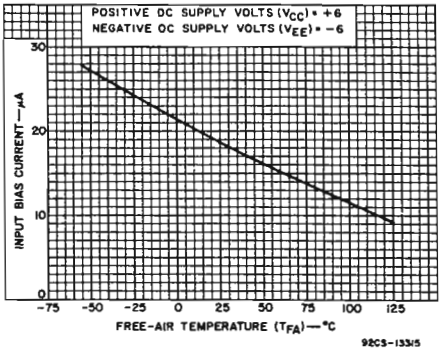


Fig.4

QUIESCENT OPERATING CURRENT

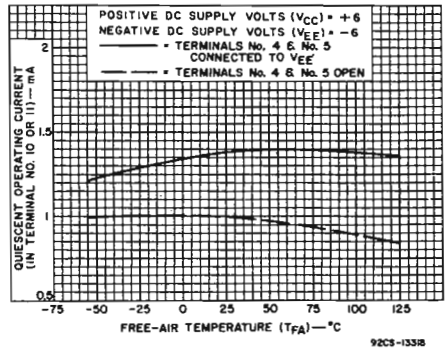


Fig.5

QUIESCENT OPERATING CURRENT RATIO

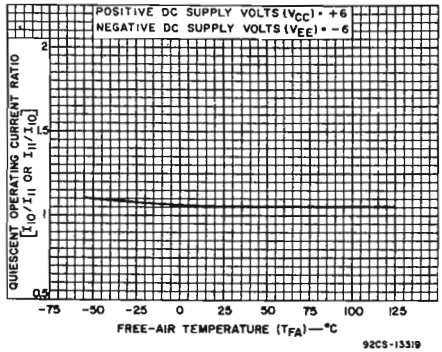


Fig.6

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA3005 AND CA3006

POWER-GAIN (CASCODE CONFIGURATION)

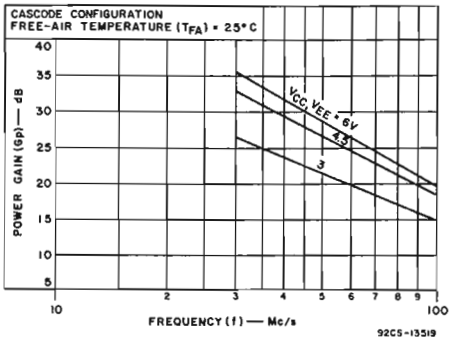


Fig.7

POWER-GAIN (DIFFERENTIAL-AMPLIFIER CONFIGURATION)

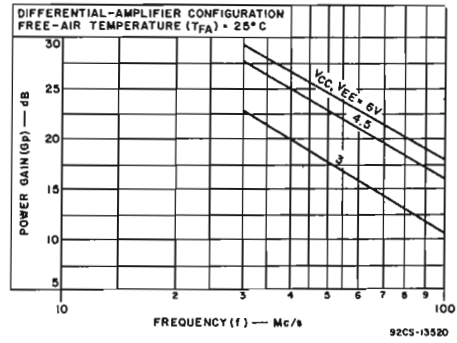
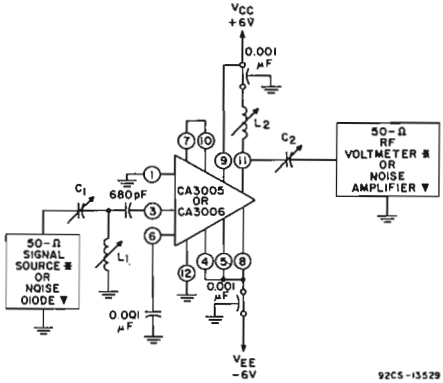


Fig.9

NOISE FIGURE AND POWER GAIN TEST CIRCUIT (CASCODE CONFIGURATION)



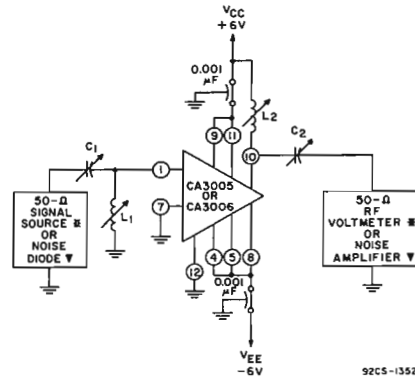
f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	14-150	5-40	0.3-0.6	0.8-1.4
100	5-40	5-40	0.07-0.12	0.15-0.3

* FOR POWER-GAIN TEST

▼ FOR NOISE-FIGURE TEST

Fig.8

NOISE FIGURE AND POWER-GAIN TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION)



f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	5-40	1.5-20	1.2-2	1.2-2
100	1-12	1-12	0.4-0.7	0.25-0.5

* FOR POWER-GAIN TEST

▼ FOR NOISE-FIGURE TEST

Fig. 10

TYPICAL DYNAMIC CHARACTERISTICS FOR TYPES CA3005 AND CA3006

100-Mc/s NOISE FIGURE VS. V_{EE} (CASCODE CONFIGURATION)

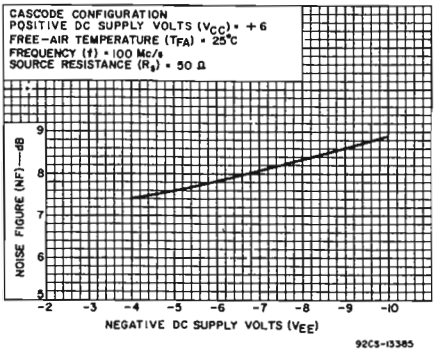


Fig. 11

100 Mc/s NOISE FIGURE VS. V_{EE} (DIFFERENTIAL AMPLIFIER CONFIGURATION)

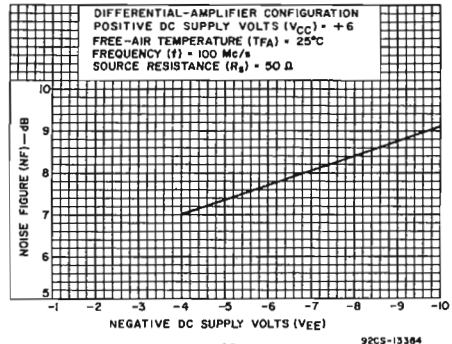


Fig. 12

COMMON-MODE-REJECTION RATIO

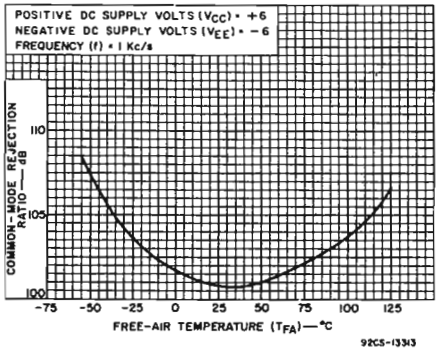


Fig. 13

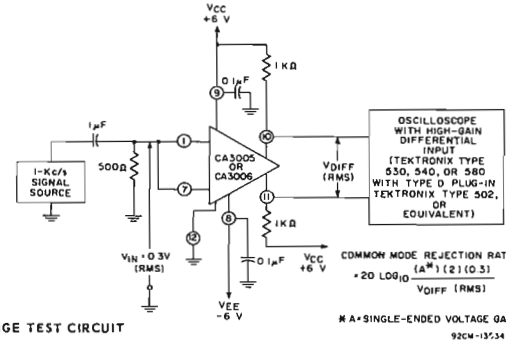


Fig. 14

AGC RANGE TEST CIRCUIT

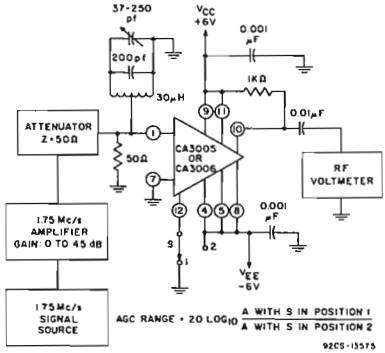


Fig. 15

RCA
Solid State
Division

Linear Integrated Circuits

CA3007

AF Amplifier

- Designed for use in Sound Systems and Communication Equipment
- Balanced differential-amplifier configuration with controlled constant-current source provides for both audio amplification and phase inversion
- Built-in temperature stability for operation from -55°C to +125°C
- Eliminates need for audio driver transformer
- Companion Application Note, ICAN 5037 "Application of the RCA-CA3007 Integrated Circuit Audio Driver" covers design of a dual supply audio driver in a direct-coupled audio amplifier, and a single supply audio driver in a capacitor-coupled audio amplifier

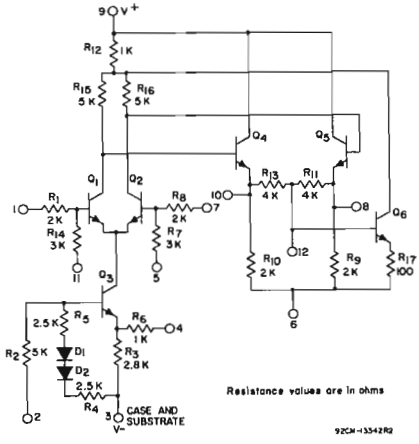
HIGHLIGHTS

- Input Impedance. . . . 4 kΩ typ.
- Output Impedance . . . 60 Ω typ.
- Power Gain . . . . . 22 dB typ.
- Push-Pull Input & Output
- Direct Coupling to Class B Audio Output Stage

APPLICATIONS

- Audio Amplifier
- Audio Driver

SCHEMATIC DIAGRAM



ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified operating conditions for other terminals. All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$, or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
2	-8	0	3	-8
			6	0
			7	0
			9	+6
			11	0
3	-10	0	6	0
			7	0
			9	+6
			11	0
4	-8.5	0	6	0
			7	0
			9	+6
			11	0
5	-2.5	+2.5	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
6	-3	0	2	0
			3	-6
			7	0
			9	+6
			11	0
7	-2.5	+2.5	1	0
			2	0
			3	-6
			5	0
			6	0
			9	+6
8	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
9	0	+10	2	0
			3	-6
			6	0
			7	0
			11	0
10	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
11	-2.5	+2.5	1	0
			2	0
			3	-6
			6	0
			7	0
			9	+6
12	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±2.5 V

MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . ±2.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

ELECTRICAL CHARACTERISTICS, at $T_{FA} = 25^{o}C$, $V_{CC} = +6$ V, $V_{EE} = -6$ V,

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Pin 4 Not Connected Unless Otherwise Noted	TEST CIRCUITS	LIMITS TYPE CA3007				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS								
Input Unbalance Voltage	V_{IU}		3	–	0.57	5	mV	2
Input Unbalance Current	I_{IU}		3	–	0.57	5	μA	2
Input Bias Current	I_I		3	–	11	34	μA	4
Quiescent Operating Voltage	V_8 or V_{10}		3	–	0.87	–	V	5
Device Dissipation	P_T		3	–	30	–	mW	NONE
DYNAMIC CHARACTERISTICS								
Power Gain	G_P	f = 1 Kc/s	6	20	22	–	dB	NONE
Total Harmonic Distortion	THD	f = 1 Kc/s	6	–	0.28	–	%	NONE
Input Impedance	Z_{IN}	f = 1 Kc/s	7	–	4K	–	Ω	NONE
Common-Mode Rejection Ratio	CMR	f = 1 Kc/s	9(A) 9(B)	–	77	–	dB	8

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUIT FOR CA3007

INPUT UNBALANCE VOLTAGE AND CURRENT vs TEMPERATURE

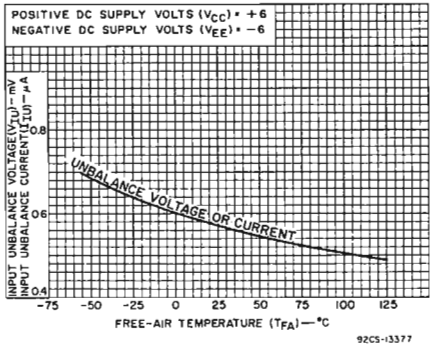
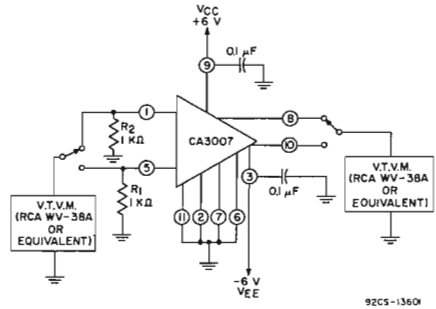


Fig.2

INPUT UNBALANCE VOLTAGE & CURRENT, INPUT BIAS CURRENT, QUIESCENT OPERATING VOLTAGE, AND DEVICE DISSIPATION TEST CIRCUIT



R_1 and R_2 matched to ±1%.

$P_T = V_{CC}I_9 + V_{EE}I_3$

I_9 = Direct Current into Terminal No.9

I_3 = Direct Current out of Terminal No.3

Fig.3

INPUT BIAS CURRENT vs TEMPERATURE

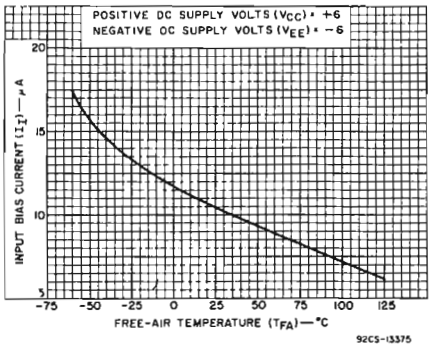


Fig.4

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

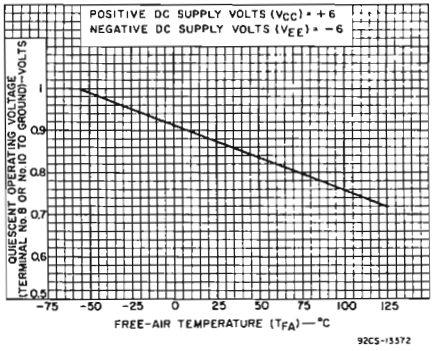
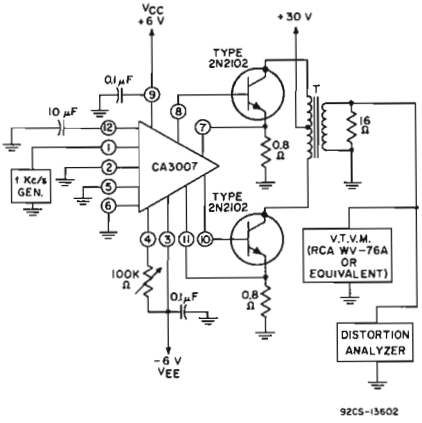


Fig.5

TYPICAL DYNAMIC TEST CIRCUITS FOR CA3007

POWER GAIN AND TOTAL HARMONIC DISTORTION TEST CIRCUIT



T (Output Transformer):
Primary Impedance = 2000 Ω C.T.
Secondary Impedance = 16 Ω
Efficiency = 45% approx.
(STANCOR TYPE TA-10 OR EQUIVALENT)

Fig.6

INPUT IMPEDANCE TEST CIRCUIT

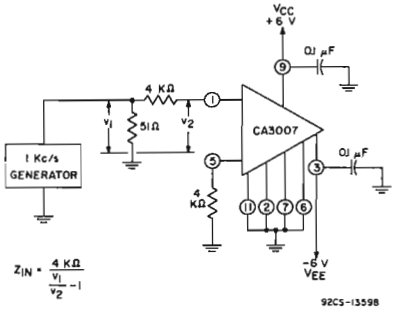


Fig.7

TYPICAL DYNAMIC CHARACTERISTIC AND TEST CIRCUITS FOR CA3007

COMMON-MODE REJECTION RATIO vs TEMPERATURE

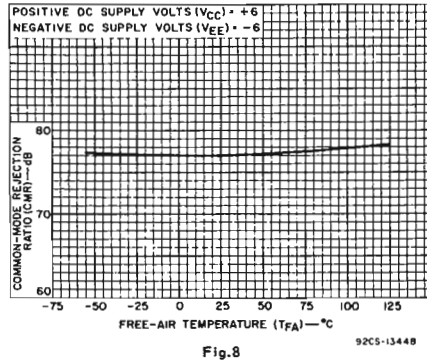
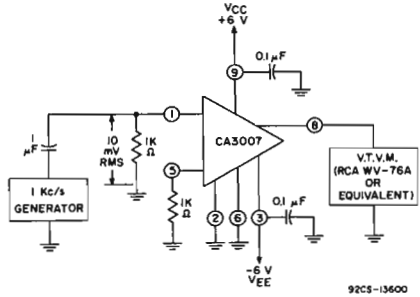
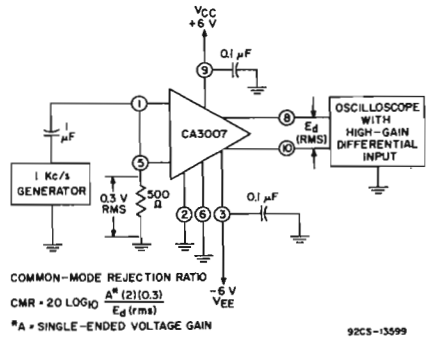


Fig.8

COMMON-MODE REJECTION-RATIO TEST CIRCUITS



(A) Single-Ended Differential Voltage Gain



(B) Common-Mode Voltage Gain

Fig.9

RCA
Solid State
Division

Linear Integrated Circuits

CA3008 CA3015 CA3030
CA3010 CA3016 CA3037
CA3029 CA3038

Operational Amplifiers

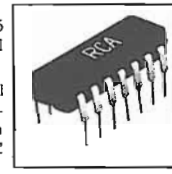
Monolithic Silicon

6-VOLT TYPES	12-VOLT TYPES	PACKAGE
CA3008	CA3016	14-Lead Flat Pack
CA3010	CA3015	12-Lead TO-5 Style
CA3029	CA3030	14-Lead Plastic Dual In-Line (TO-116)
CA3037	CA3038	14-Lead Ceramic Dual In-Line (TO-116)

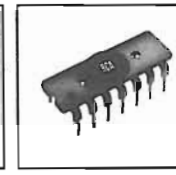
CA3008
CA3016

CA3010
CA3015

- All types are electrically identical within their voltage groups
- Designed for use in Telemetry, Data-Processing, Instrumentation, and Communication Equipment
- Built-in temperature stability from -55°C to +125°C for flatpack, TO-5 style, and ceramic dual in-line packages; 0°C to +70°C for plastic dual in-line package
- Companion Application Notes ICAN-5290, "Integrated Circuit Operational Amplifiers"; ICAN-5213, "Application of the RCA-CA3015, CA3016 Integrated Circuit Operational Amplifiers"; and ICAN-5015, "Application of the RCA-CA3008, CA3010 Integrated Circuit Operational Amplifiers"



CA3029, CA3030



CA3037, CA3038

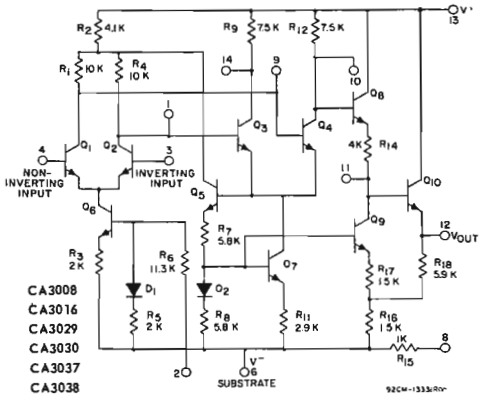
HIGHLIGHTS

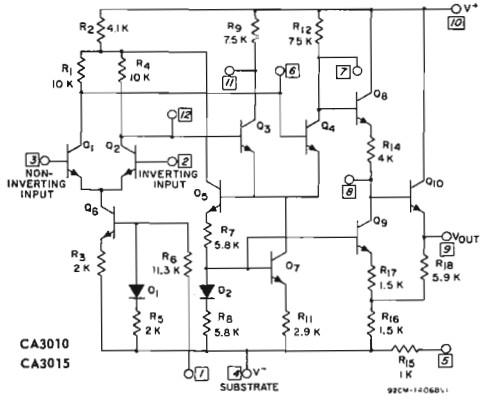
	6 V Types	12 V Types	
• Open-Loop Voltage Gain	60	70	dB typ.
• Common-Mode Rejection Ratio	94	103	dB typ.
• Output Impedance	200	92	Ω typ.
• Input Offset Voltage	1	1	mV typ.
• Static Power Drain at ± 12 V	-	175	mW typ.
± 6 V	30	30	mW typ.
± 3 V	7	7	mW typ.

APPLICATIONS

- Narrow-Band and Band-pass Amplifier
- Operational Functions
- Feedback Amplifier
- DC and Video Amplifier
- Multivibrator
- Oscillator
- Comparator
- Servo Driver
- Scaling Adder
- Balanced Modulator-Driver

SCHEMATIC DIAGRAMS





ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010	CA3008 CA3029 CA3037	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010	CA3008 CA3029 CA3037	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 (CA3008, CA3029, CA3037) 4 & 9 (CA3010)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.4, CA3010 (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015	CA3016 CA3030 CA3038	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015	CA3016 CA3030 CA3038	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 (CA3016, CA3030, CA3038) 4 & 9 (CA3015)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.4, CA3015 (Substrate) DO NOT GROUND				

	CA3008 CA3016 CA3037 CA3038	CA3010 CA3015	CA3029 CA3030
OPERATING TEMPERATURE RANGE	-55°C to +125°C		-40°C to +85°C
STORAGE TEMPERATURE RANGE	-65°C to +150°C		-65°C to +150°C

	CA3016 CA3030 CA3038	CA3015	CA3008 CA3029	CA3010 CA3037
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V		-4 V to +1 V	
MAXIMUM DEVICE DISSIPATION	600 mW		300 mW	

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 (CA3008, CA3016, CA3029, CA3030, CA3037, CA3038) Terminal No.5 (CA3010, CA3015) Not Connected Unless Otherwise Specified	Test Circuit Fig.	CA3008 CA3010 CA3029 CA3037 Min.	Typ.	Max.	CA3016 CA3015 CA3030 CA3038 Min.	Typ.	Max.	Units	Typical Characteristic Curves Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	1.08 -	5 -	- -	- 1.37	- 5	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.54 -	5 -	- -	- 1.07	- 5	μA	2
Input Bias Current	I_{IB}	= +6V = -6V = +12V = -12V	5	- -	5.3 -	12 -	- -	- 9.6	- 24	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_D	= +6 V = -6 V = +12V = -12V	4	- -	30 -	- -	- -	- 175	- -	mW	none
		[5] shorted to [9] V_{CC} = +6V, V_{EE} = -6V 8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		- -	102 -	- -	- -	- 500	- -		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Common-Mode Rejection Ratio	CMRR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	10 -	14 -	- -	- 5	- 7.8	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	200 -	- -	- -	- 92	- -	Ω	16
Common-Mode Input-Voltage Range	V_{ICR}	= +6V = -6V = +12V = -12V	11	0.5 to -4 -	- -	- -	- 0.65 to -8	- -	- -	V	none

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

INPUT OFFSET VOLTAGE AND CURRENT

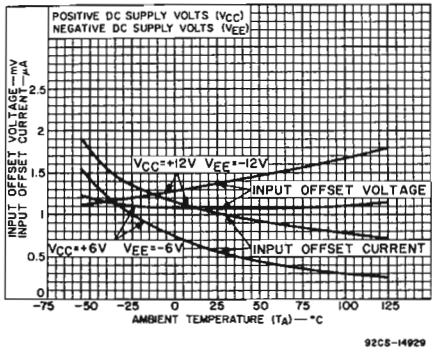


Fig.2

INPUT BIAS CURRENT

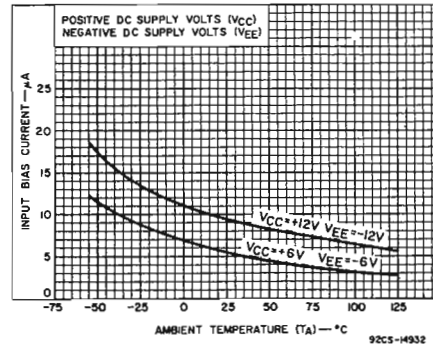


Fig.3

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

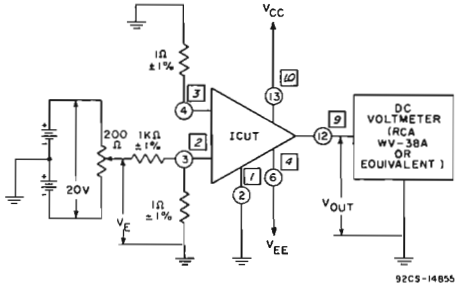


Fig.4

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

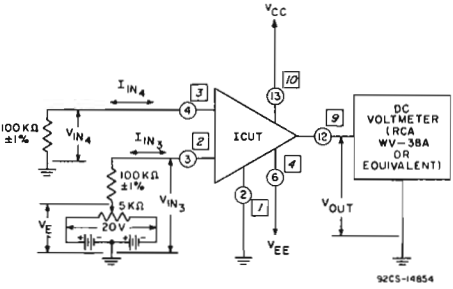


Fig.5

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal (13) or [10]

I_E = Direct Current out of Terminal (6) or [4]

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}.
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

OPEN-LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3008, CA3010, CA3015, CA3016, CA3037, CA3038

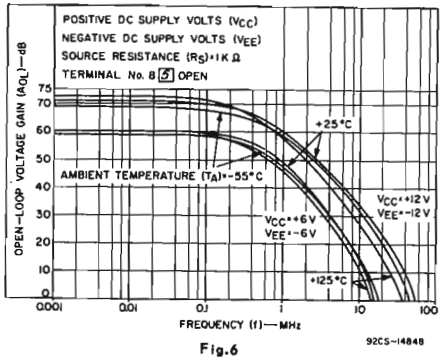


Fig.6

OPEN-LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3029 AND CA3030

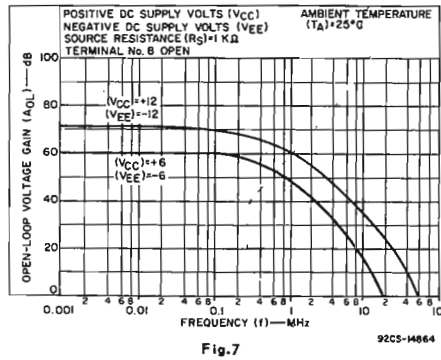
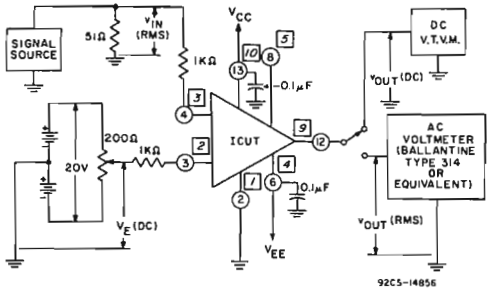


Fig.7

OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE, AND OPEN-LOOP BANDWIDTH AT -3 dB POINT TEST CIRCUIT



Procedure:

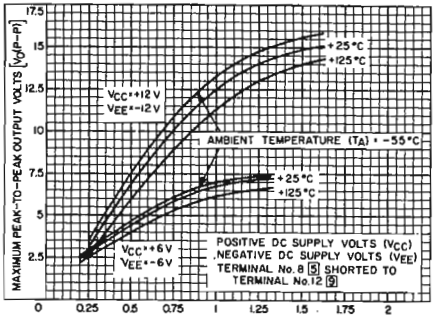
1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz.

$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

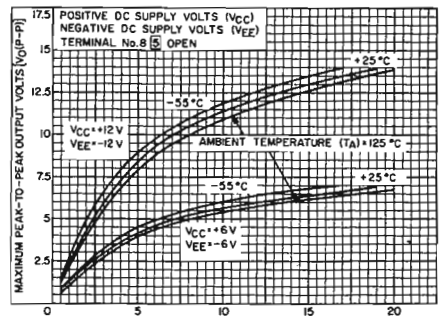
3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz.
4. Measure Open-Loop Bandwidth at -3 dB Point.
   Reference Level = A_{OL} at 1 kHz.

Fig.8

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3008, CA3010, CA3015, CA3016, CA3037, CA3038



(a)



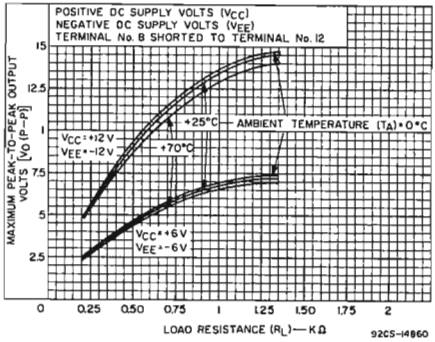
(b)

Fig.9

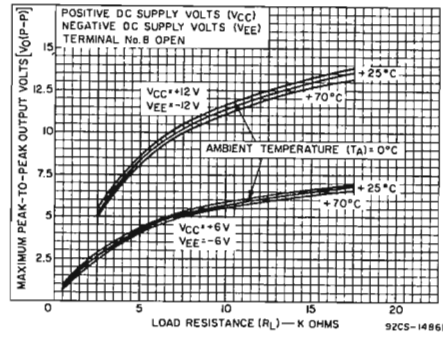
TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3029 AND CA3030



(a)



(b)

Fig.10

COMMON-MODE REJECTION RATIO AND COMMON-MODE INPUT-VOLTAGE-RANGE TEST CIRCUIT

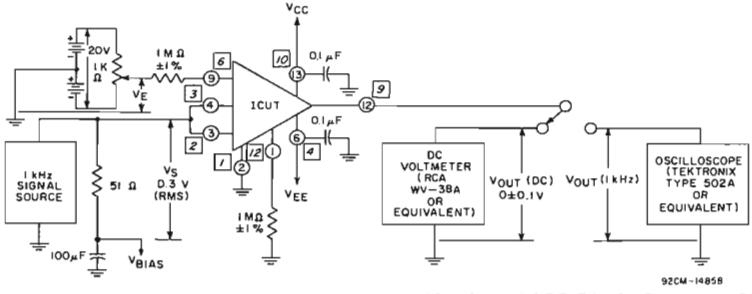


Fig.11

Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for $V_{OUT(DC)}$ = 0 ± 0.1 V.
2. Apply 1-kHz sinusoidal input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB}.$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

COMMON-MODE REJECTION RATIO vs. FREQUENCY

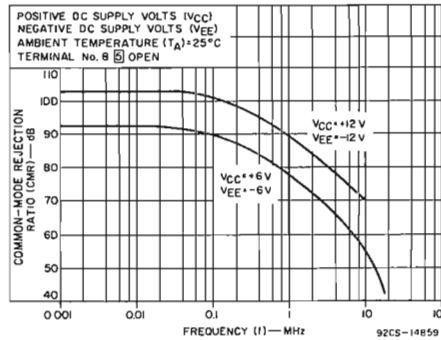


Fig.12

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

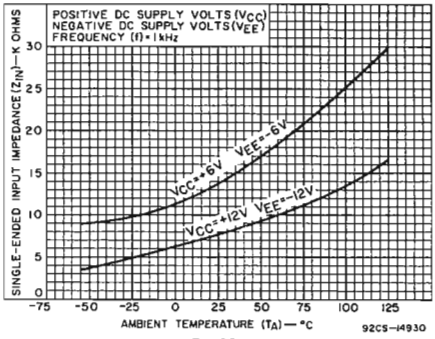


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

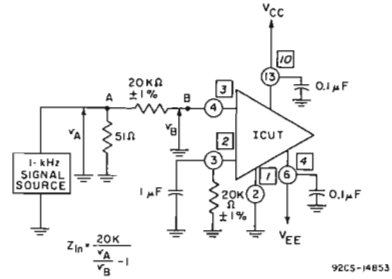


Fig.14

OUTPUT IMPEDANCE TEST CIRCUIT

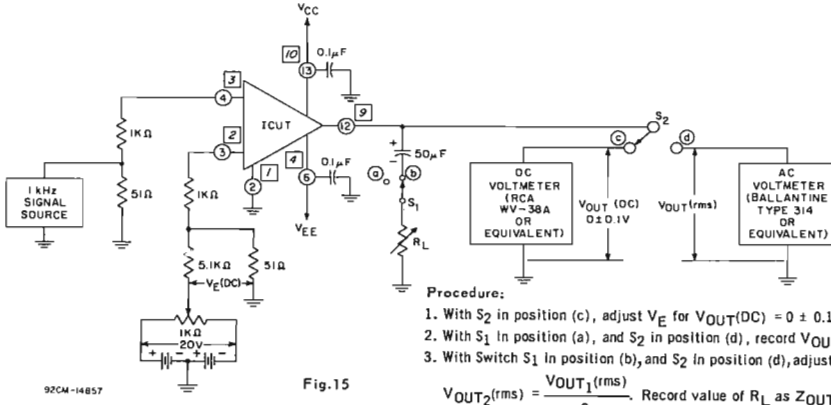
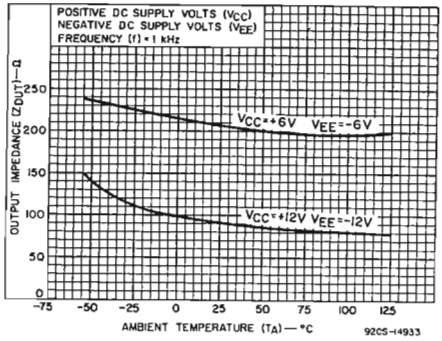


Fig.15

Procedure:

1. With S_2 in position (c), adjust V_E for V_{OUT}(DC) = 0 ± 0.1 volt.
2. With S_1 in position (a), and S_2 in position (d), record V_{OUT_1}(rms).
3. With Switch S_1 in position (b), and S_2 in position (d), adjust R_L until $V_{OUT_2}(\text{rms}) = \frac{V_{OUT_1}(\text{rms})}{2}$. Record value of R_L as Z_{OUT}.



OUTPUT IMPEDANCE vs. TEMPERATURE

Fig.16

RCA
Solid State
Division

Linear Integrated Circuits

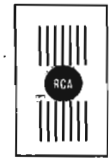
CA3008A CA3015A CA3030A
CA3010A CA3016A CA3037A
CA3029A CA3038A

Operational Amplifiers

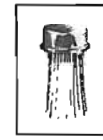
Monolithic Silicon

6-VOLT TYPES	12-VOLT TYPES	PACKAGE
CA3008A	CA3016A	14-Lead Flat Pack
CA3010A	CA3015A	12-Lead TO-5 Style
CA3029A	CA3030A	14-Lead Plastic Dual In-Line (TO-116)
CA3037A	CA3038A	14-Lead Ceramic Dual In-Line (TO-116)

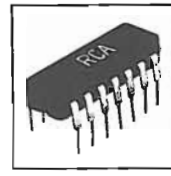
- These new types have all the desirable features and characteristics of their prototypes plus lower noise figures and improved input characteristics for offset voltage, offset current, bias current, and impedance.
- All types are electrically identical within their voltage groups
- Designed for use in Telemetry, Data-Processing, Instrumentation, and Communication Equipment
- Built-in temperature stability from -55°C to +125°C for Flatpack, TO-5 style, and ceramic dual in-line packages; 0°C to +70°C for plastic dual in-line package
- Companion Application Notes ICAN-5290, "Integrated Circuit Operational Amplifiers"; ICAN-5213, "Application of the RCA-CA3015, CA3016 Integrated Circuit Operational Amplifiers"; and ICAN-5015, "Application of the RCA-CA3008, CA3010 Integrated Circuit Operational Amplifiers" cover Bode characteristics, phase compensation, frequency shaping, and amplifier design.



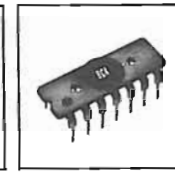
CA3008A, CA3016A



CA3010A, CA3015A



CA3029A, CA3030A



CA3037A, CA3038A

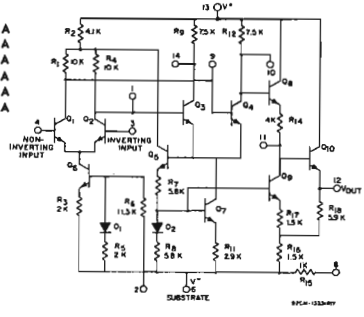
HIGHLIGHTS

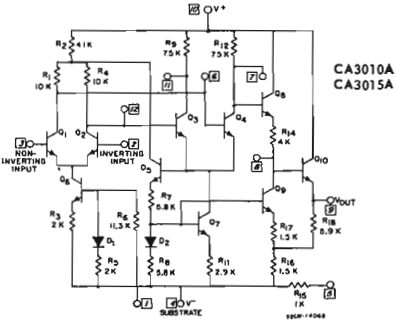
	6V Types	12V Types	
• Open-Loop Voltage Gain	60	70	dB typ.
• Common-Mode Rejection Ratio	94	103	dB typ.
• Input Impedance	20	10	k typ.
• Input Offset Voltage	0.9	1	mV typ.
• Input Offset Current	0.3	0.5	A typ.
• Input Bias Current	2.5	4.7	A typ.
• Static Power Drain at ±12V	-	175	mW typ.
at ±6V	30	30	mW typ.
at ±3V	7	7	mW typ.

APPLICATIONS

- Narrow-Band and Band-pass Amplifier
- Operational Functions
- Feedback Amplifier
- DC and Video Amplifier
- Multivibrator
- Oscillator
- Comparator
- Servo Driver
- Scaling Adder
- Balanced Modulator-Driver

CA3008A
CA3016A
CA3029A
CA3030A
CA3037A
CA3038A





CA3010A
CA3015A

Fig.1

SCHEMATIC DIAGRAMS

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010A	CA3008A, CA3029A, CA3037A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010A	CA3008A, CA3029A, CA3037A	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
-	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 (CA3008A, CA3029A, CA3037A) 4 & 9 (CA3010A)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.4, CA3010A (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015A	CA3016A, CA3030A, CA3038A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015A	CA3016A, CA3030A, CA3038A	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 (CA3016A, CA3030A, CA3038A) 4 & 9 (CA3015A)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.4, CA3015A (Substrate) DO NOT GROUND				

	CA3008A, CA3016A, CA3037A, CA3038A	CA3010A, CA3015A, CA3029A, CA3030A
OPERATING TEMPERATURE RANGE	-55°C to +125°C	-40°C to +85°C
STORAGE TEMPERATURE RANGE	-65°C to +200°C	-65°C to +150°C

	CA3016A, CA3030A, CA3038A	CA3015A, CA3008A, CA3029A	CA3010A, CA3037A
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V	
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW	

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 (CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A), Terminal No.5 (CA3010A, CA3015A) Not Connected Unless Otherwise Specified	Test Circuit Fig.	CA3008A CA3010A CA3029A CA3037A Min.	Typ.	Max.	CA3016A CA3015A CA3030A CA3038A Min.	Typ.	Max.	Units	Typical Characteristic Curves Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	0.9 -	2 -	- -	- 1	- 2	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.3 -	1.5 -	- -	- 0.5	- 1.6	μA	2
Input Bias Current	I_{IB}	= +6V = -6V = +12V = -12V	5	- -	2.5 -	4 -	- -	- 4.7	- 6	μA	3
Input Offset Voltage Sensitivity: Positive	$-V_{IO}/-V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$-V_{IO}/-V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_D	= +6 V = -6 V = +12V = -12V	4	- -	40 -	- -	- -	- 175	- -	mW	none
		5 shorted to 9 V_{CC} = +6V, V_{EE} = -6V 8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		- -	102 -	- -	- -	- 500	- -		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Slew Rate	SR	V_{CC} = +6V V_{EE} = -6V R_S = 1 kΩ = +12V = -12V	none	- -	3 -	- -	- -	- 7	- -	V/μs	none
Common-Mode Rejection Ratio	CMR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	15 -	20 -	- -	- 7.5	- 10	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	160 -	- -	- -	- 85	- -	Ω	16
Common-Mode Input-Voltage Range	V_{ICR}	= +6V = -6V = +12V = -12V	11	+0.5 -4 -	- - -	- - -	- +0.65 -8	- - -	- - -	V	none
Noise Figure	NF	V_{CC} = +3V, V_{EE} = -3V R_S = 1 kΩ = +6V = -6V = +9V = -9V = +12V = -12V	18	- - - -	6.3 8.3 - -	9 12 - -	- - - -	6.3 8.3 10 11	9 12 14 16	dB	17

LEAD TEMPERATURE (During Soldering): ALL TYPES

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

INPUT OFFSET VOLTAGE AND CURRENT

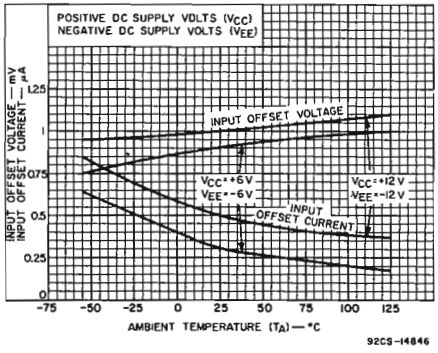


Fig.2

INPUT BIAS CURRENT

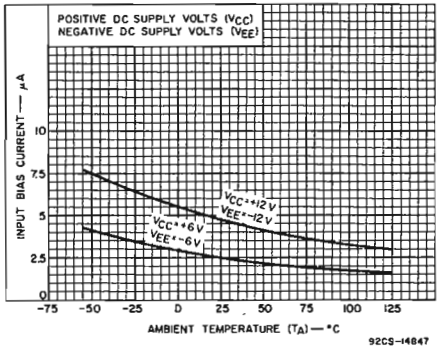


Fig.3

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

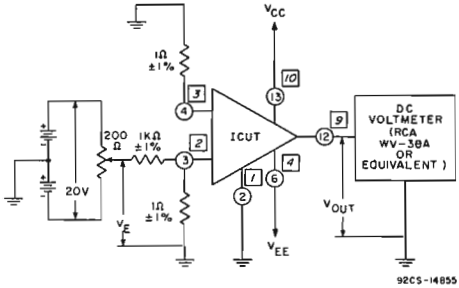


Fig.4

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

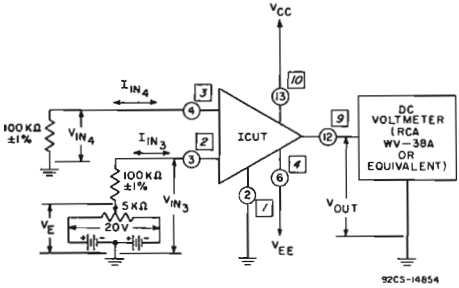


Fig.5

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the difference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal 13 or *10*

I_E = Direct Current out of Terminal 6 or *4*

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3008A, CA3010A, CA3015A, CA3016A, CA3037A, CA3038A

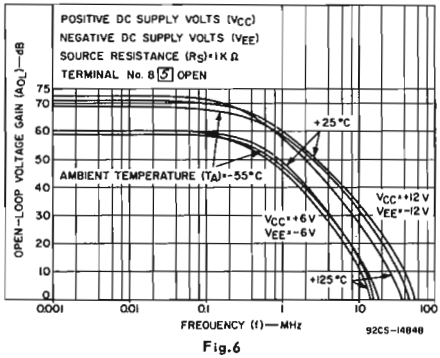


Fig.6

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3029A AND CA3030A.

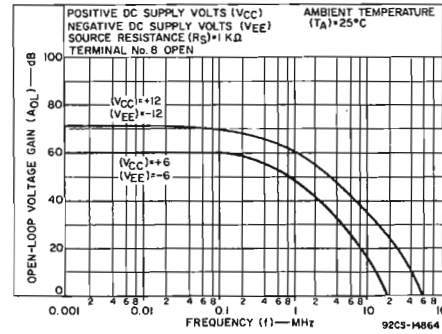
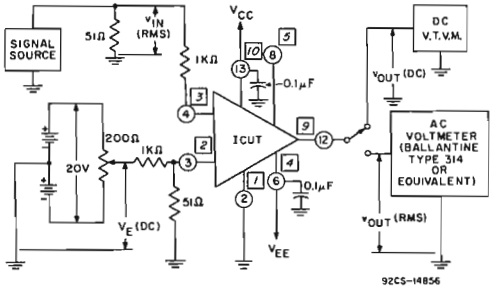


Fig.7

OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE, AND OPEN-LOOP BANDWIDTH AT -3 POINT TEST CIRCUIT



Procedure:

1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz

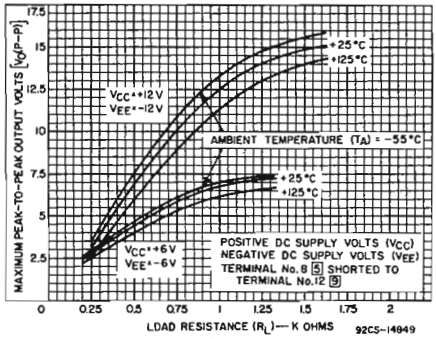
$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz
4. Measure Open-Loop Bandwidth at -3 dB Point

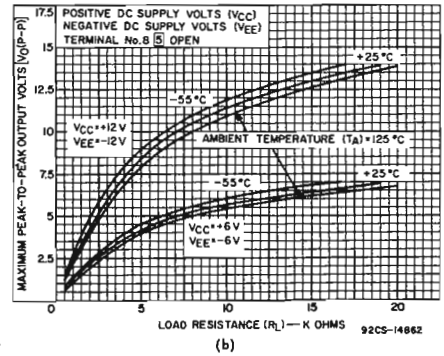
Reference Level = A_{OL} at 1 kHz

Fig.8

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3008A, CA3010A, CA3015A, CA3016A, CA3037A, CA3038A



(a)



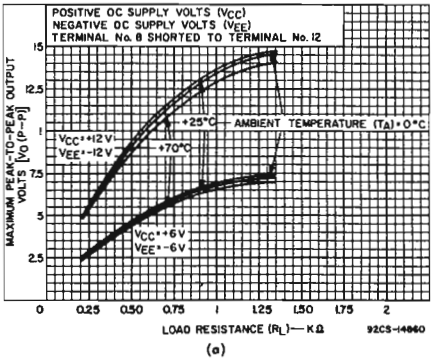
(b)

Fig.9

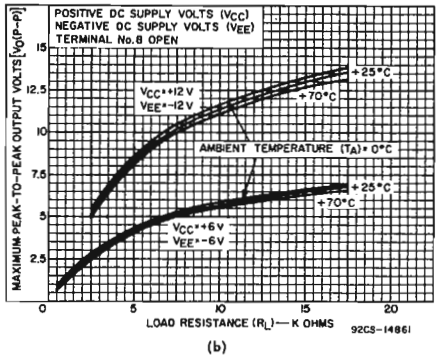
TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3029A AND CA3030A



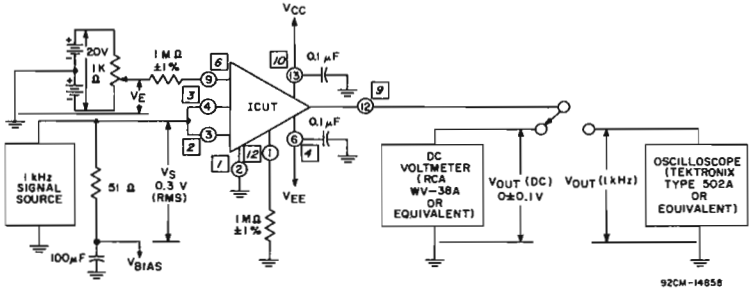
(a)



(b)

Fig.10

COMMON-MODE REJECTION RATIO AND COMMON-MODE INPUT-VOLTAGE-RANGE TEST CIRCUIT



Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for V_{OUT}(DC) = 0 ± 0.1 V.
2. Apply 1-kHz sinusoidal input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB}.$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig.11

COMMON-MODE REJECTION RATIO vs. FREQUENCY

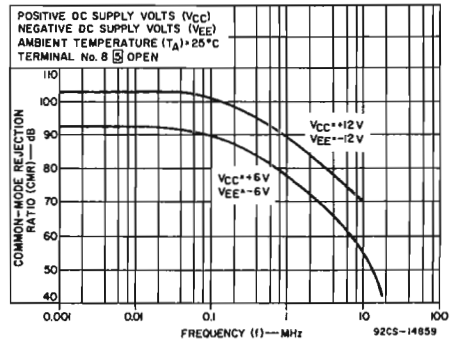


Fig.12

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

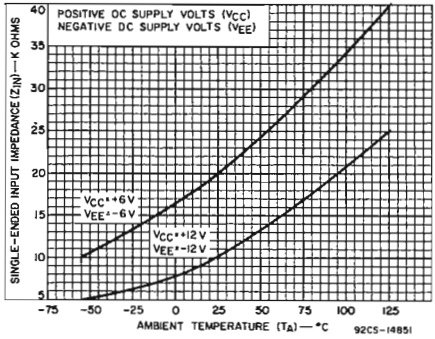


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

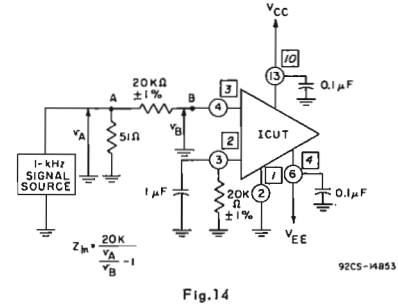


Fig.14

OUTPUT IMPEDANCE TEST CIRCUIT

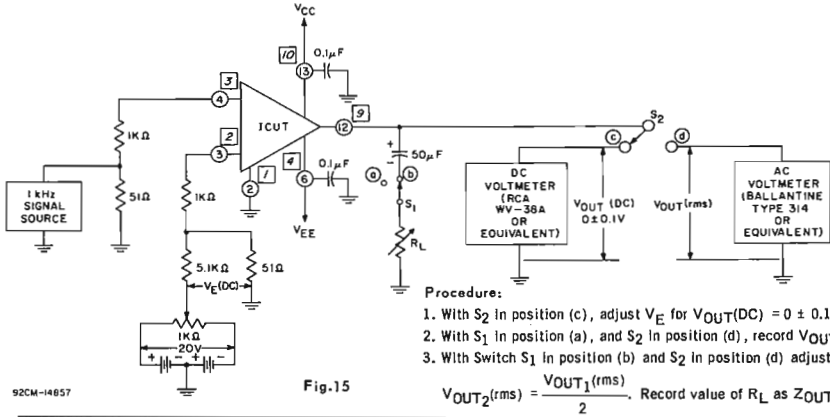
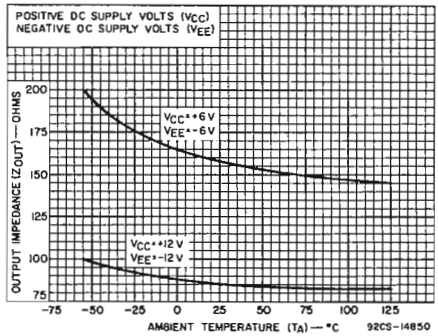


Fig.15

Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record V_{OUT_1}(rms).
3. With Switch S_1 in position (b) and S_2 in position (d) adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.



OUTPUT IMPEDANCE vs. TEMPERATURE

Fig.16

NOISE FIGURE vs. FREQUENCY

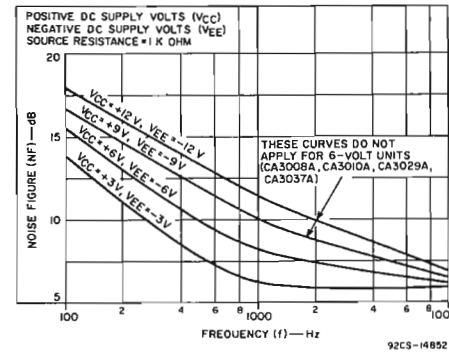


Fig.17

RCA
Solid State
Division

Linear Integrated Circuits

CA3011
CA3012

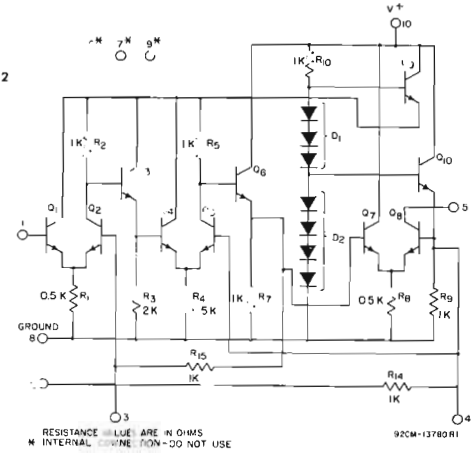
Wide-Band Amplifiers

Monolithic Silicon

FEATURES & APPLICATIONS

- exceptionally high amplifier gain: power gain at 4.5 MHz – 75 dB typ.
- excellent limiting characteristics – Input limiting voltage (knee) = 600 μV typ. at 10.7 MHz
- wide frequency capability – 100 kHz to > 20 MHz

Fig. 1 SCHEMATIC DIAGRAM FOR CA3011 AND CA3012



BLOCK DIAGRAM OF TYPICAL FM RECEIVER USING RCA-CA3011 OR CA3012 INTEGRATED CIRCUIT WIDE-BAND AMPLIFIER

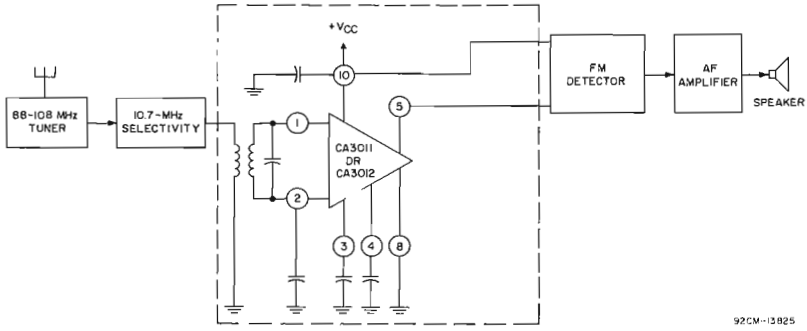


Fig. 2

ABSOLUTE-MAXIMUM VOLTAGE LIMITS AT T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 8).

NOTE: TERMINALS 6, 7, AND 9 OF RCA-CA3011 AND CA3012 ARE USED FOR INTERNAL CONNECTIONS. DO NOT APPLY VOLTAGES OR MAKE EXTERNAL CONNECTIONS TO THESE TERMINALS.

CA3011

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS						
			1	2	3	4	5	8	10
1	-3	+3	–	Same as 1	Do Not Apply External Voltage	+2.5 to +7.5	+7.5	Ground	+7.5
2	-3	+3	Same as 2	–		+2.5 to +7.5	+7.5	Ground	+7.5
3	-3	+3	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	+7.5
4	+2.5	+7.5	-3 to +3	Same as 1		–	+7.5	Ground	+7.5
5	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	–	Ground	+7.5
8	-3	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	+7.5
10	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	–
CASE	INTERNALLY CONNECTED TO TERMINAL NO.8 (GROUND TERMINAL)								

CA3012

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS						
			1	2	3	4	5	8	10
1	-3	+3	–	Same as 1	Do Not Apply External Voltage	+2.5 to +10	+10	Ground	+10
2	-3	+3	Same as 2	–		+2.5 to +10	+10	Ground	+10
3	-3	+3	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	+10
4	+2.5	+10	-3 to +3	Same as 1		–	+10	Ground	+10
5	0	+13	-3 to +3	Same as 1		+2.5 to +10	–	Ground	+10
8	-3	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	+10
10	0	+13	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	–
CASE	INTERNALLY CONNECTED TO TERMINAL NO.8 (GROUND TERMINAL)								

OPERATING-TEMPERATURE RANGE ..... -55 to +125° C
STORAGE-TEMPERATURE RANGE ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C

MAXIMUM INPUT-SIGNAL VOLTAGE:
Between Terminals 1 and 2 ..... ±3 V

MAXIMUM DEVICE DISSIPATION ..... 300 mW

RECOMMENDED MINIMUM DC SUPPLY VOLTAGE (V_{CC}) .. 5.5 V

Example of Use of LIMITS TABLE:

For RCA-3012, a maximum voltage of ±3 volts may be applied to Terminal 1 under the following conditions:

Terminal 2 is at the same dc potential as Terminal 1
Terminal 3: do not apply external voltage
Terminal 4 is at any dc potential between +2.5 and +10 volts
Terminal 5 is at a dc potential of +10 volts
Terminals 6, 7, and 9 are at 0 dc potential (NOT USED)
Terminal 8 is at dc ground potential
Terminal 10 is at a dc potential of +10 volts

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS						UNITS	TYPICAL CHARACTERISTICS CURVES
		SETUP & PROCEDURE	FREQUENCY f	DC SUPPLY VOLTAGE V_{CC}	AMBIENT TEMPERATURE T_A	RCA CA3011			RCA CA3012				
		Fig.	Mc/s	Volts	°C	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
Total Device Dissipation *	P_T	3	–	6	-55	–	80	–	66	80	135	mW	4
					+25	60	90	133	66	90	121	mW	
					+125	–	70	–	65	70	121	mW	
			–	7.5	-55	–	130	–	97	130	190	mW	4
					+25	95	120	187	97	120	167	mW	
					+125	–	100	–	95	100	167	mW	
			–	10	-55	–	–	–	150	210	275	mW	4
					+25	–	–	–	150	190	255	mW	
					+125	–	–	–	150	160	255	mW	
Voltage Gain**	A	5	1	6	-55	–	55	–	50	55	–	dB	6
					+25	60	66	–	60	66	–	dB	
					+125	–	61	–	50	61	–	dB	
		5	1	7.5	-55	–	59	–	55	59	–	dB	6
					+25	65	70	–	65	70	–	dB	
					+125	–	65	–	55	65	–	dB	
		5	1	10	-55	–	–	–	55	61	–	dB	6
					+25	–	–	–	65	71	–	dB	
					+125	–	–	–	55	66	–	dB	
		5	4.5	7.5	+25	60	67	–	60	67	–	dB	7
			10.7	7.5	+25	55	61	–	55	61	–	dB	
Input-Impedance Components: Parallel Input Resistance	R_{IN}	8	4.5	7.5	+25	–	3	–	–	3	–	kΩ	9
Parallel Input Capacitance	C_{IN}	8	4.5	7.5	+25	–	7	–	–	7	–	pF	9
Output Impedance Components: Parallel Output Resistance	R_{OUT}	10	4.5	7.5	+25	–	31.5	–	–	31.5	–	kΩ	11
Parallel Output Capacitance	C_{OUT}	10	4.5	7.5	+25	–	4.2	–	–	4.2	–	pF	11
Noise Figure	NF	12	4.5	7.5	+25	–	8.7	–	–	8.7	–	dB	13
Input Limiting Voltage (Knee)	$V_{i(lim)}$	5	4.5	7.5	+25	–	300	450	–	300	400	μV	6

* The total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

TYPICAL CHARACTERISTICS AND TEST SETUPS

DISSIPATION TEST SETUP

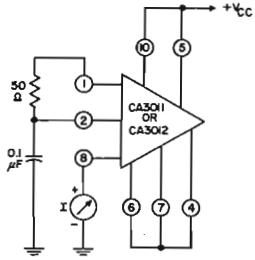


Fig.3

DISSIPATION VS TEMPERATURE

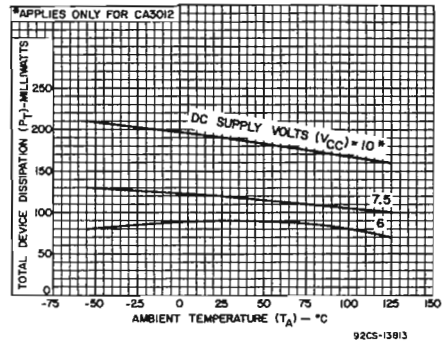


Fig.4

VOLTAGE-GAIN TEST SETUP

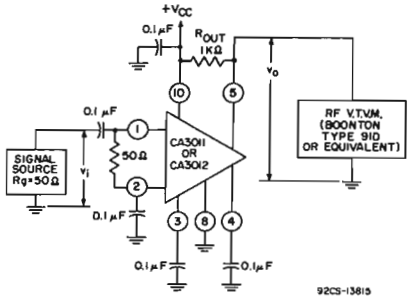


Fig.5

PROCEDURES

A - Voltage Gain:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$
4) Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

B - Input Limiting Voltage (Knee):

1) Repeat Steps A1 and A2, using v_i = 100 mV
2) Decrease v_i to the level at which v_o is 3 dB below its value for v_i = 100 mV.
3) Record v_i as Input Limiting Voltage (Knee).

VOLTAGE GAIN & INPUT LIMITING VOLTAGE VS TEMPERATURE

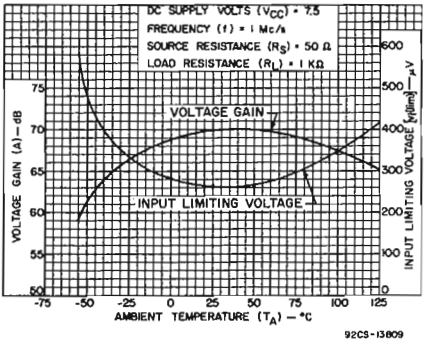


Fig.6

VOLTAGE GAIN AND INPUT LIMITING VOLTAGE VS FREQUENCY

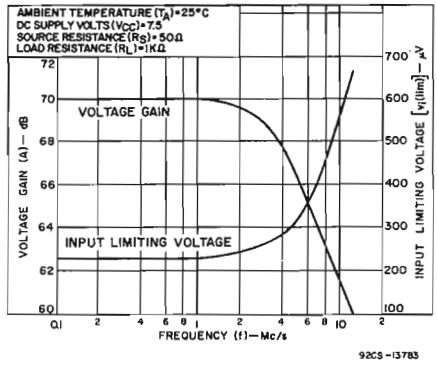


Fig.7

TYPICAL CHARACTERISTICS AND TEST SETUPS

INPUT-IMPEDANCE COMPONENTS TEST SETUP

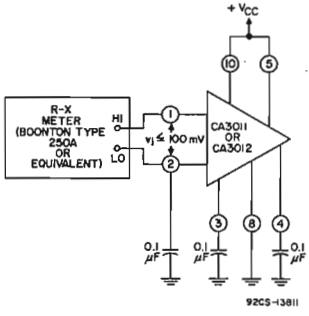


Fig.8

INPUT-IMPEDANCE COMPONENTS VS FREQUENCY

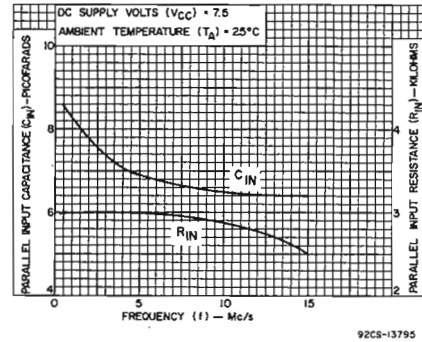


Fig.9

OUTPUT-IMPEDANCE COMPONENTS TEST SETUP

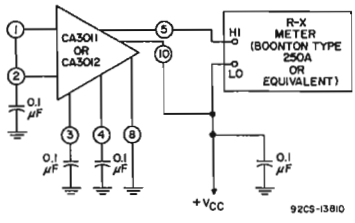


Fig.10

OUTPUT-IMPEDANCE COMPONENTS VS FREQUENCY

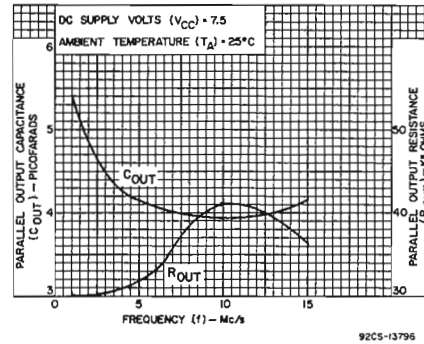
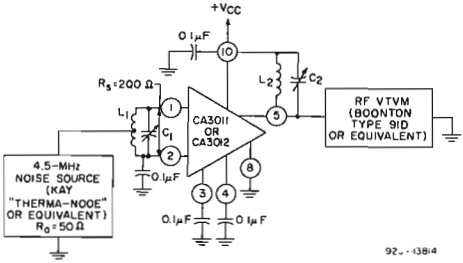


Fig.11

NOISE FIGURE TEST SETUP



L_1 = 82 μH, center-tapped

L_2 = 2.36 μH

C_1,C_2 = Arco Type 423 padder, or equivalent

Fig.12

NOISE FIGURE VS DC SUPPLY VOLTAGE

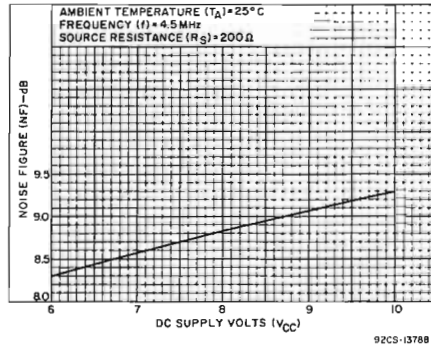


Fig.13

RCA
Solid State
Division

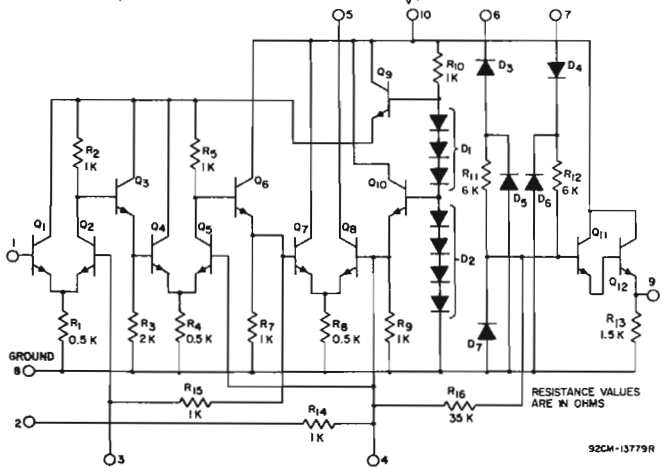
Linear Integrated Circuits

CA3013
CA3014

Wide-Band Amplifier-Discriminators

Monolithic Silicon

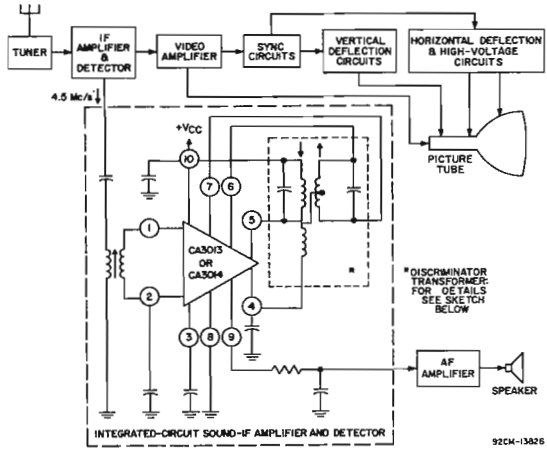
SCHEMATIC DIAGRAM FOR CA3013 AND CA3014



FEATURES & APPLICATIONS:

- exceptionally high gain:
  power gain at 4.5 MHz — 75 dB typ.
- excellent limiting characteristics — input limiting voltage (knee) = 300 μV typ. at 4.5 MHz
- excellent AM rejection: > 50 dB at 4.5 MHz
- high audio-voltage recovery — 220 mV typ. at 4.5 MHz 25 kHz deviation
- wide frequency capability — 100 kHz to > 20 MHz
- comprehensive circuit functions:
  if amplifier, AM and noise limiter, FM detector, audio preamplifier

BLOCK DIAGRAM OF TYPICAL TELEVISION RECEIVER USING RCA INTEGRATED-CIRCUIT SOUND-IF AMPLIFIER AND DETECTOR SECTION



ABSOLUTE-MAXIMUM VOLTAGE LIMITS AT T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 8).

CA3013

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS									
			1	2	3	4	5	6	7	8	9	10
1	-3	+3	-	Same as 1	Do Not Apply External Voltage	+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
2	-3	+3	Same as 2	-		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
3	-3	+3	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
4	+2.5	+7.5	-3 to +3	Same as 1		-	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
5	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	-	Same as 4	Same as 4	Ground	AF Output	+7.5
6	+2.5	+7.5	-3 to +3	Same as 1		Same as 6	+7.5	-	Same as 4	Ground	AF Output	+7.5
7	+2.5	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	-	Ground	AF Output	+7.5
8	-3	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
9	0	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	-	+7.5
10	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	-
CASE	INTERNALLY CONNECTED TO TERMINAL No.8 (GROUND TERMINAL)											

CA3014

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS									
			1	2	3	4	5	6	7	8	9	10
1	-3	+3	-	Same as 1	Do Not Apply External Voltage	+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
2	-3	+3	Same as 2	-		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
3	-3	+3	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
4	+2.5	+10	-3 to +3	Same as 1		-	+10	Same as 4	Same as 4	Ground	AF Output	+10
5	0	+13	-3 to +3	Same as 1		+2.5 to +10	-	Same as 4	Same as 4	Ground	AF Output	+10
6	+2.5	+10	-3 to +3	Same as 1		Same as 6	+10	-	Same as 4	Ground	AF Output	+10
7	+2.5	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	-	Ground	AF Output	+10
8	-3	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
9	0	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	-	+10
10	0	+13	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	-
CASE	INTERNALLY CONNECTED TO TERMINAL No.8 (GROUND TERMINAL)											

OPERATING-TEMPERATURE RANGE ..... -55 to +125°C

STORAGE-TEMPERATURE RANGE ..... -65 to +150°C

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max ..... +265°C

MAXIMUM INPUT-SIGNAL VOLTAGE:
Between Terminals 1 and 2 ..... ± 3 V

MAXIMUM DEVICE DISSIPATION ..... 300 mW

RECOMMENDED MINIMUM DC
SUPPLY VOLTAGE (V_{CC}) ..... 5.5 V

Exemple of use of LIMITS TABLE:

For RCA-CA3013, a maximum voltage of ±3 volts may be applied to Terminal 1 under the following conditions:

Terminal 2 is at the same dc potential as Terminal 1
Terminal 3: do not apply external voltage
Terminal 4 is at any dc potential between +2.5 and +7.5 volts
Terminal 5 is at a dc potential of +7.5 volts
Terminals 6 and 7 are at the same dc potential as Terminal 4
Terminal 8 is at dc ground potential
Terminal 9 is used as the af output terminal
Terminal 10 is at a dc potential of +7.5 volts

ELECTRICAL CHARACTERISTICS (See Page 8 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS				LIMITS						UNITS	TYPICAL CHARACTERISTICS CURVES
		SETUP & PROCEDURE	FREQUENCY f	DC SUPPLY VOLTAGE V_{CC}	AMBIENT TEMPERATURE T_A	RCA CA3013			RCA CA3014				
		Fig.	Mc/s	volts	°C	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
Total Device Dissipation*	P_T	3	–	6	-55	–	80	–	73	80	120	mW	4
					+25	60	90	133	73	90	110	mW	
					+125	–	70	–	60	70	110	mW	
		3	–	7.5	-55	–	130	–	106	130	170	mW	4
					+25	87	120	187	106	120	150	mW	
					+125	–	100	–	90	100	150	mW	
		3	–	10	-55	–	–	–	165	210	250	mW	4
					+25	–	–	–	165	190	230	mW	
					+125	–	–	–	150	160	230	mW	
Voltage Gain**	A	5	1	6	-55	–	55	–	50	55	–	dB	6
					+25	60	66	–	60	66	–	dB	
					+125	–	61	–	50	61	–	dB	
		5	1	7.5	-55	–	59	–	55	59	–	dB	6
					+25	65	70	–	65	70	–	dB	
					+125	–	65	–	55	65	–	dB	
		5	1	10	-55	–	–	–	55	61	–	dB	6
					+25	–	–	–	65	71	–	dB	
					+125	–	–	–	55	66	–	dB	
		5	4.5	7.5	+25	60	67	–	60	67	–	dB	7
			10.7	7.5	+25	55	60	–	55	60	–	dB	
Input-Impedance Components: Parallel Input Resistance	R_{IN}	8	4.5	7.5	+25	–	3	–	–	3	–	kΩ	9
Parallel Input Capacitance	C_{IN}	8	4.5	7.5	+25	–	7	–	–	7	–	pF	9
Output-Impedance Components: Parallel Output Resistance	R_{OUT}	10	4.5	7.5	+25	–	31.5	–	–	31.5	–	kΩ	11
Parallel Output Capacitance	C_{OUT}	10	4.5	7.5	+25	–	4.2	–	–	4.2	–	pF	11
Noise Figure	NF	12	4.5	7.5	+25	–	8.7	–	–	8.7	–	dB	13
Input Limiting Voltage (Knee)	v_i(lim)	14	4.5	7.5	+25	–	300	450	–	300	400	μV	15
Recovered AF Voltage	v_o(af)	14	4.5	6	+25	–	155	–	–	155	–	mV	15
				7.5	+25	128	188	–	135	188	–	mV	
				10	+25	–	–	–	–	220	–	mV	
Amplitude-Modulation Rejection	AMR	16	4.5	7.5	+25	–	50	–	–	50	–	dB	–
Discriminator Output Resistance	R_O(disc)	–	4.5	7.5	+25	–	60	–	–	60	–	Ω	–
Total Harmonic Distortion	THD	14	4.5	7.5	+25	–	1.8	–	–	1.8	–	%	17

* Total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

TYPICAL CHARACTERISTICS AND TEST SETUPS

DISSIPATION TEST SETUP

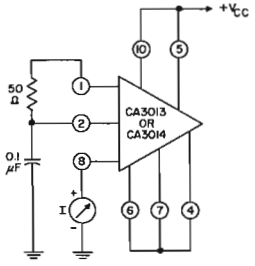


Fig.3

DISSIPATION vs. TEMPERATURE

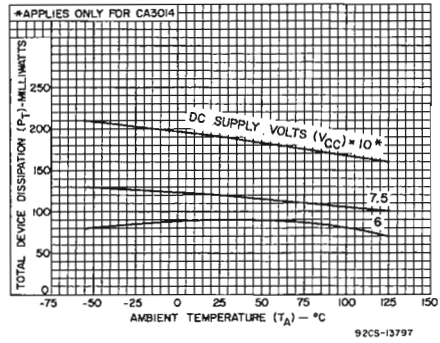
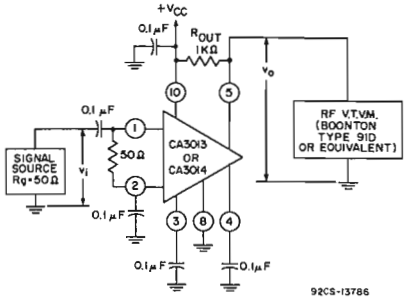


Fig.4

VOLTAGE-GAIN TEST SETUP



PROCEDURE:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$.
4) Repeat Steps 1, 2, and 3 for each frequency and/or temperature desired.

Fig.5

1-Mc/s VOLTAGE GAIN vs. TEMPERATURE

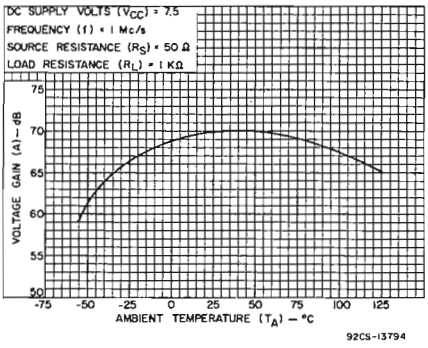


Fig.6

VOLTAGE GAIN vs. FREQUENCY

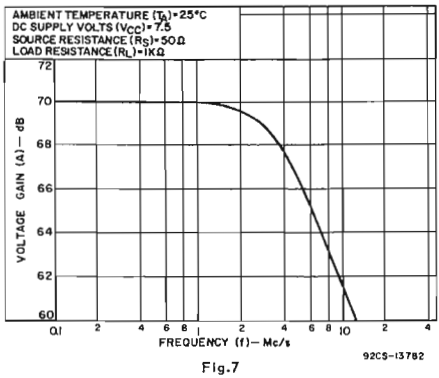


Fig.7

TYPICAL CHARACTERISTICS AND TEST SETUPS

INPUT-IMPEDANCE COMPONENTS TEST SETUP

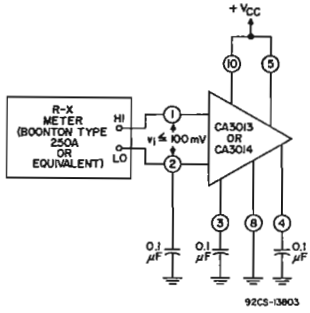


Fig.8

INPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

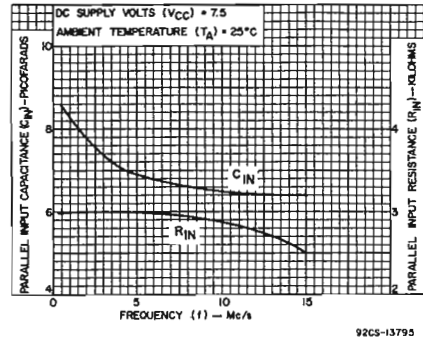


Fig.9

OUTPUT-IMPEDANCE COMPONENTS TEST SETUP

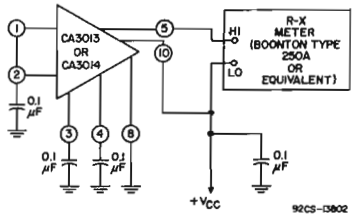


Fig.10

OUTPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

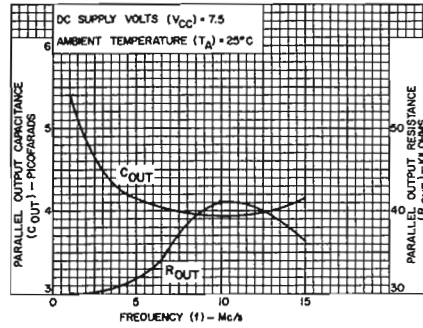
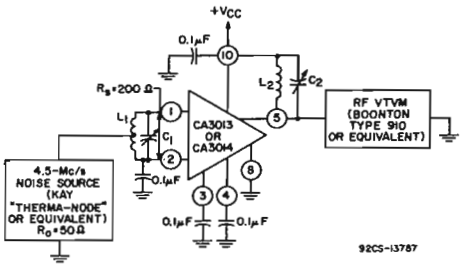


Fig.11

NOISE FIGURE TEST SETUP



L_1 = 82 μH, center-tapped

L_2 = 2.36 μH

C_1, C_2 = Arco Type 423 padder, or equivalent

Fig.12

NOISE FIGURE vs. DC SUPPLY VOLTAGE

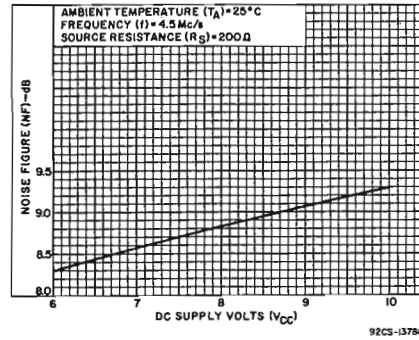
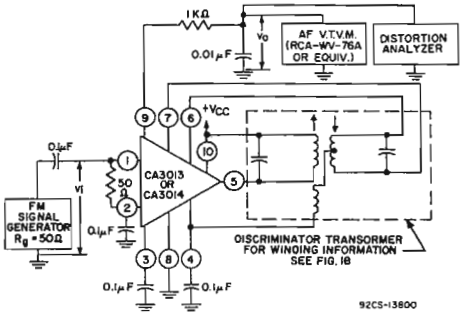


Fig.13

TYPICAL CHARACTERISTICS AND TEST SETUPS

INPUT LIMITING VOLTAGE, RECOVERED AF VOLTAGE, AND TOTAL HARMONIC DISTORTION TEST SETUP



PROCEDURE:

A - Recovered-AF Voltage Output:

1) Set input frequency = 4.5 Mc/s, v_i = 100 mV rms, modulating frequency = 1 kc/s, frequency deviation = ±25 kc/s.

2) Record v_o as Recovered-AF Voltage Output.

B - Input Limiting Voltage (Knee):

1) Repeat Steps A1 and A2, using v_i = 100 mV rms.

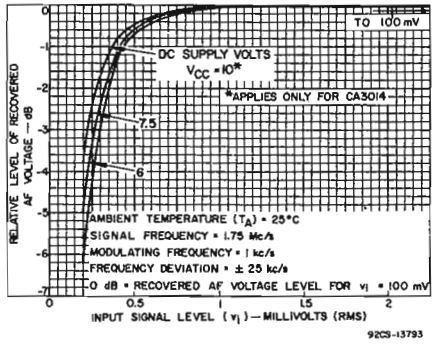
2) Decrease v_i to the level at which v_o is 3 dB below its value for v_i = 100 mV.

3) Record v_i as Input Limiting Voltage (Knee).

Fig. 14

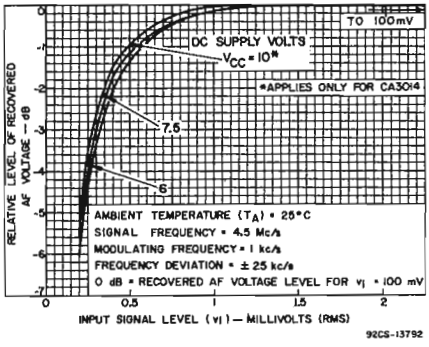
INPUT LIMITING VOLTAGE (KNEE) AND RECOVERED AF VOLTAGE

at 1.75 Mc/s



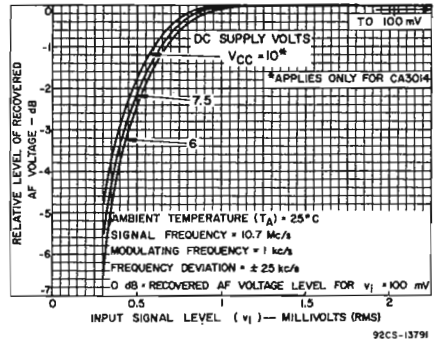
(a)

at 4.5 Mc/s



(b)

at 10.7 Mc/s

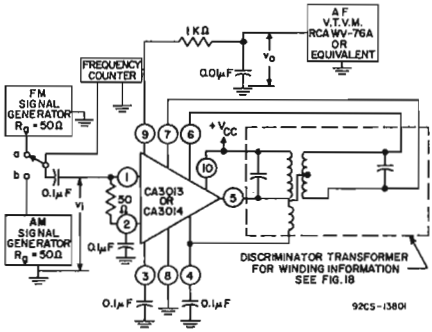


(c)

Fig. 15

TYPICAL CHARACTERISTICS AND TEST SETUPS

AM-REJECTION TEST SETUP



PROCEDURE:

1) With Switch S in position "a", set input frequency = 4.5 Mc/s, v_i = 10 mV rms, modulating frequency = 1 kc/s, frequency deviation = ±25 kc/s.
2) Record v_o.
3) Place Switch S in position "b", and set input frequency = 4.5 Mc/s, v_i = 10 mV rms, modulating frequency = 1 kc/s, % modulation = 50.
4) Measure v_o, and record value in dB below value in Step 2 as AM Rejection.

Fig. 16

TOTAL HARMONIC DISTORTION vs. DC SUPPLY VOLTAGE

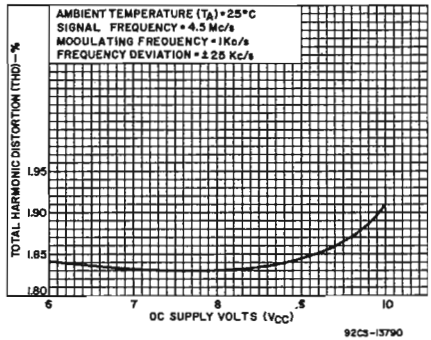
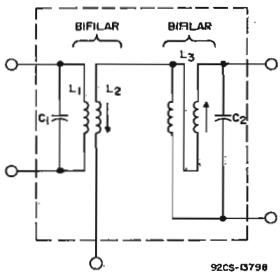


Fig. 17

DISCRIMINATOR TRANSFORMER SCHEMATIC



(a)

CONSTRUCTION DETAILS OF DISCRIMINATOR TRANSFORMERS SHOWN IN FIGS. 2, 14 AND 16

Coil-Form Outside Diameter = 7/32 inch

Slugs: Radio Industries, Inc. Type "E" Material, or equivalent

Wire Type: "GRIPEZE"*, or equivalent

Operating Frequency Mc/s	Wire Size (AWG #)	Turns L_1▲	Turns L_2▲	Turns L_3	C_1 pF	C_2 pF
1.75	40	44	20	44 total (22 bifilar wound)	820	820
4.5	36	18	7	22 total (11 bifilar wound)	560	330
10.7	36	18	18	18 total (9 bifilar wound)	100	100

* Registered Trade Mark, Phelps-Dodge Copper Products.

▲ wound bifilar.

NOTE: The mutual coupling between L_1 and L_3 is adjusted for the desired degree of linearity.

(b)

Fig. 18

RCA Solid State Division

Linear Integrated Circuits

CA3018
CA3018A

General-Purpose Transistor Arrays

Monolithic Silicon

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

APPLICATIONS

- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated-Circuit Transistor Array" for suggested Applications.

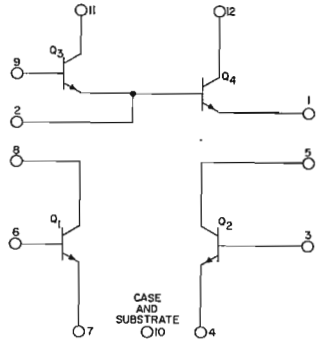


Fig. 1 - Schematic Diagram for CA3018 and CA3018A

TWO ISOLATED TRANSISTORS AND A DARLINGTON-CONNECTED TRANSISTOR PAIR

For Low-Power Applications at Frequencies from DC Through the VHF Range

12-Lead TO-5 Style

FEATURES

- Matched monolithic general purpose transistors
- H_{FE} matched ± 10%
- V_{BE} matched ± 2 mV CA3018A (± 5mV CA3018)
- Operation from DC to 120 MHz
- Wide operating current range
- CA3018A performance characteristics controlled from 10 μA to 10mA
- Low noise figure - - 3.2 dB typical at 1KHz
- Full military temperature range capability (-55 to + 125°C)

Maximum Ratings, Absolute-Maximum Values, at TA=25°C

	CA3018	CA3018A	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	450	450	mW
Derate at 5 mW/°C for $T_A > 85°C$			
Temperature Range:			
Operating	-55 to + 125	-55 to + 125	°C
Storage.	-65 to + 150	-65 to + 150	°C
LEAD TEMPERATURE (During Soldering)			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)			
from case for 10 seconds max.	+265		°C

The following ratings apply for each transistor in the device:

	CA3018	CA3018A	
Collector-to-Emitter Voltage, V_{CEO} ·	15	15	V
Collector-to-Base Voltage, V_{CBO} · ·	20	30	V
Collector-to-Substrate Voltage, V_{CIO}*	20	40	V
Emitter-to-Base Voltage, V_{EBO} · · ·	5	5	V
Collector Current, I_C	50	50	mA

*The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. *The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

Characteristics apply for each transistor in the CA3018 and CA3018A as specified.

ELECTRICAL CHARACTERISTICS at T_A = 25°C	SYMBOLS	SPECIAL TEST CONDITIONS	CA3018 LIMITS			CA3018A LIMITS			Units	CHARACTERISTICS CURVES
			Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS										
Collector-Cutoff Current	I_{CBO}	V_{CB}=10V, I_E=0	–	0.002	100	–	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE}=10V, I_B=0	–	See Curve	5	–	See Curve	0.5	μA	3
Collector-Cutoff Current Darlington Pair	I_{CEOD}	V_{CE}=10V, I_B=0	–	–	–	–	–	5	μA	–
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	15	24	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0	20	60	–	30	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0	5	7	–	5	7	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C=10μA, I_{CI}=0	20	60	–	40	60	–	V	–
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B=1mA, I_C=10mA	–	0.23	–	–	0.23	0.5	V	–
Static Forward Current Transfer Ratio	h_{FE}	V_{CE}=3V, I_C=10mA I_C=1mA I_C=10μA	– 30 –	100 100 54	– 200 –	50 60 30	100 100 54	– 200 –	– – –	4
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		V_{CE}=3V, I_{C1}=I_{C2}=1mA	0.9	0.97	–	0.9	0.97	–	–	4
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	V_{CE}=3V I_C=1mA I_C=100μA	1500 –	5400 –	– –	2000 1000	5400 2800	– –	–	5
Base-to-Emitter Voltage	V_{BE}	V_{CE}=3V I_E=1mA I_E=10mA	– –	0.715 0.800	– –	0.600 –	0.715 0.800	0.800 0.900	V	6
Input Offset Voltage	$\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE}=3V, I_E=1mA	–	0.48	5	–	0.48	2	mV	6,8
Temperature Coefficient: Base-to-Emitter Voltage Q_1,Q_2	$\lvert \frac{\Delta V_{BE}}{\Delta T} \rvert$	V_{CE}=3V, I_E=1mA	–	-1.9	–	–	-1.9	–	$mV/^oC$	7
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} (V_{9-1})	V_{CE}=3V I_E=10mA I_E=1mA	– –	1.46 1.32	– –	– 1.10	1.46 1.32	1.60 1.50	V	9
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$\lvert \frac{\Delta V_{BED}}{\Delta T} \rvert$	V_{CE}=3V, I_E=1mA	–	4.4	–	–	4.4	–	$mV/^oC$	10
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\lvert \frac{\Delta V_{BE_1} - V_{BE_2}}{\Delta T} \rvert$	V_{CC}=+6V, V_{EE}=-6V, I_{C1}=I_{C2}=1mA	–	10	–	–	10	–	$\mu V/^oC$	–

ELECTRICAL CHARACTERISTICS, (CONT'D)

DYNAMIC CHARACTERISTICS			CA3018			CA3018A				
Low Frequency Noise Figure	NF	f=1 KHz, V_{CE}=3V, I_C=100μA Source resistance=1 KΩ	–	3.25	–	–	3.25	–	dB	11(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward Current-Transfer Ratio	h_{fe}	f=1kHz, V_{CE}=3V, I_C=1mA	–	110	–	–	110	–	–	12
Short-Circuit Input Impedance	h_{ie}		–	3.5	–	–	3.5	–	KΩ	12
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	μmho	12
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	1.8×10^{-4}	–	–	1.8×10^{-4}	–	–	12
Admittance Characteristics:										
Forward Transfer Admittance	Y_{fe}	f=1MHz, V_{CE}=3V, I_C=1mA	–	31-j1.5	–	–	31-j1.5	–	mmho	13
Input Admittance	Y_{ie}		–	0.3+j0.04	–	–	0.3+j0.04	–	mmho	14
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho	15
Reverse Transfer Admittance	Y_{re}		See Curve			See Curve			mmho	16
Gain-Bandwidth Product	f_T	V_{CE}=3V, I_C=3mA	300	500	–	300	500	–	MHz	17
Emitter-to-Base Capacitance	C_{EB}	V_{EB}=3V, I_E=0	–	0.6	–	–	0.6	–	pF	–
Collector-to-Base Capacitance	C_{CB}	V_{CB}=3V, I_C=0	–	0.58	–	–	0.58	–	pF	–
Collector-to-Substrate Capacitance	C_{CI}	V_{CI}=3V, I_C=0	–	2.8	–	–	2.8	–	pF	–

STATIC CHARACTERISTICS

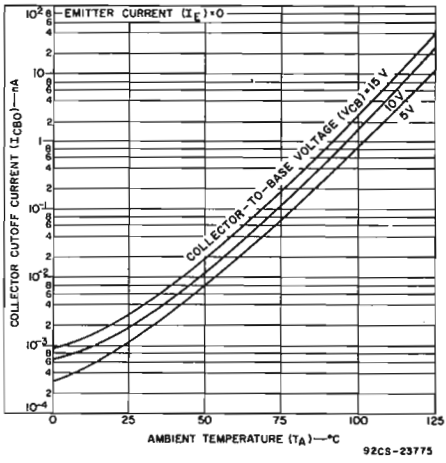


Fig.2 - Typical Collector-To-Base Cutoff Current vs Ambient Temperature for Each Transistor.

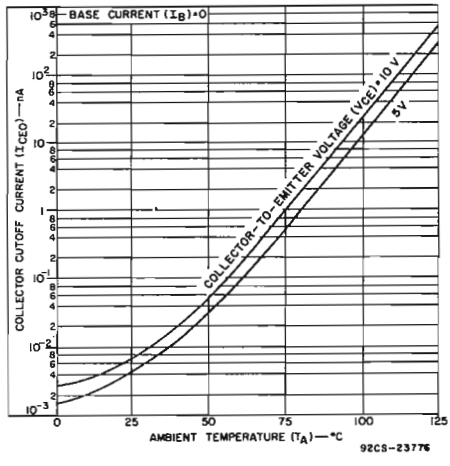


Fig.3 - Typical Collector-To-Emmiter Cutoff Current vs Ambient Temperature for Each Transistor.

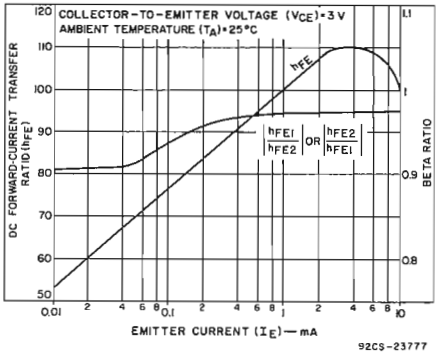


Fig.4 - Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q, and Q_2 vs Emitter Current.

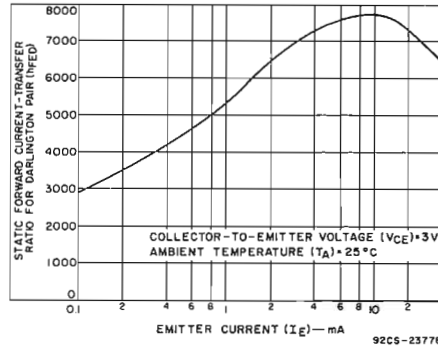


Fig.5 - Typical Static Forword Current - Transfer Ratio for Darlington-connected Transisters Q_3 and Q_4 vs Emitter Current.

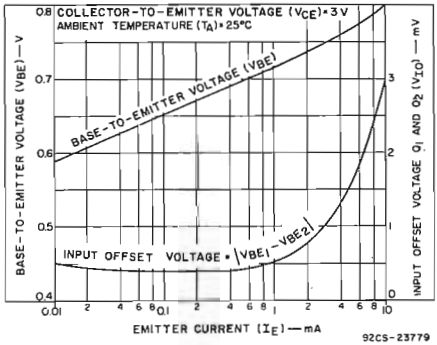


Fig.6 - Typical Static Base-to-Emitter Voltage Characteristic and Input Offset Voltage for Q_1 and Q_2 vs Emitter Current.

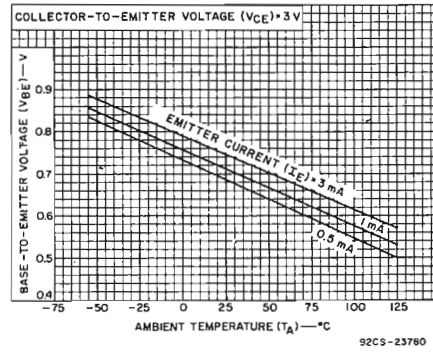


Fig.7 - Typical Base-To-Emitter Valtage Characteristic for Each Transistar vs Ambient Temperature

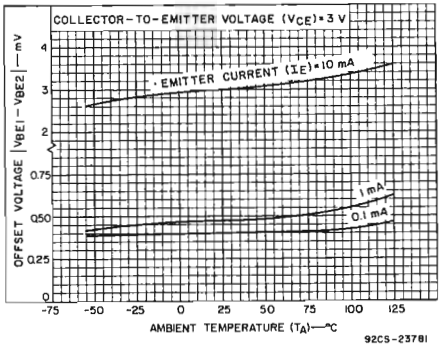


Fig.8 - Typical Offset Voltage Characteristic vs Ambient Temperature

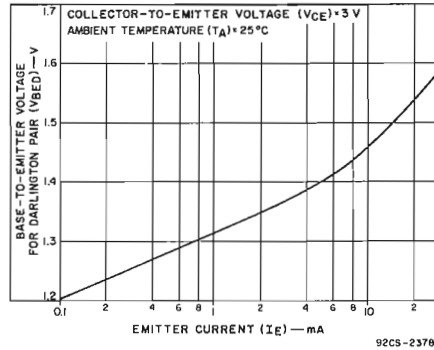


Fig.9 - Typical Static Input Valtage Characteristic for Darlington Pair (Q_3 and Q_4) vs Emitter Current

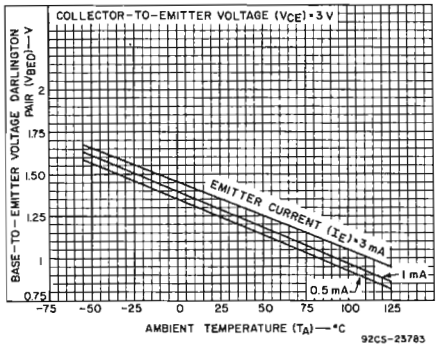


Fig.10 - Typical Static Input Voltage Characteristic for Darlington Poir (Q_3 and Q_4) vs Ambient Temperature.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

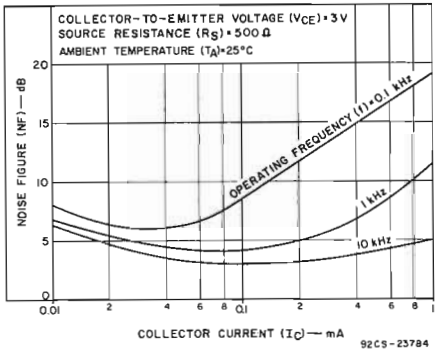


Fig.11(a) - Noise Figure vs Collector Current, R_S = 500 Ω.

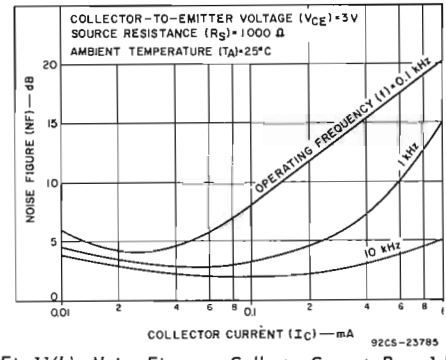


Fig.11(b) - Noise Figure vs Collector Current, R_S = 1 KΩ.

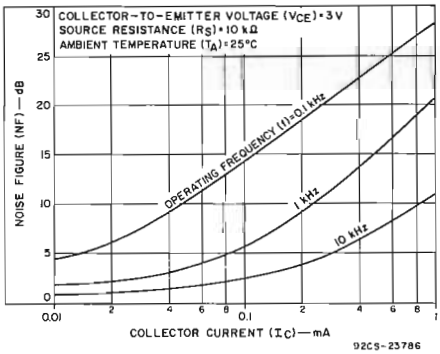


Fig.11(c) - Noise Figure vs Collector Current, R_S = 10 KΩ.

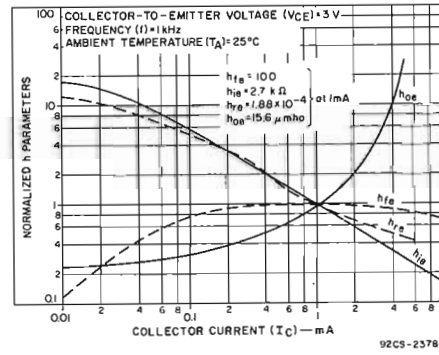


Fig.12 - Forward Current-Transfer Ratio (h_{fe}), Short-Circuit Input Impedance (h_{ie}), Open-Circuit Output Impedance (h_{oe}), and Open-Circuit Reverse Voltage-Transfer Ratio (h_{re}) vs Collector Current

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

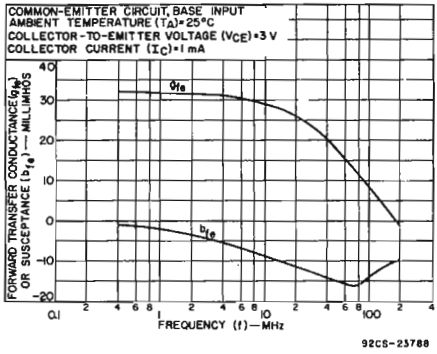


Fig.13 - Forward Transfer Admittance (Y_{fe})

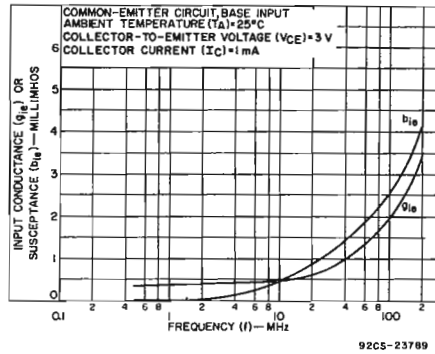


Fig.14 - Input Admittance (Y_{ie})

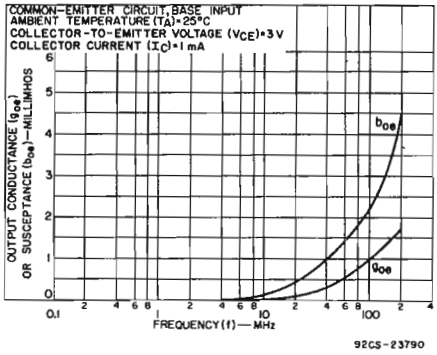


Fig.15 - Output Admittance (Y_{oe})

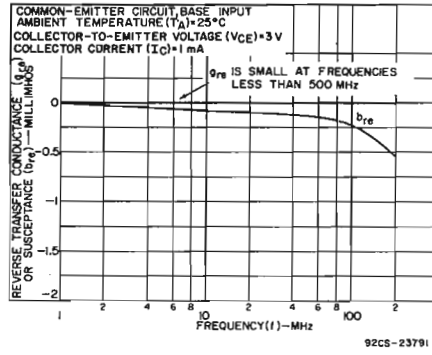


Fig.16 - Reverse Transfer Admittance (Y_{re})

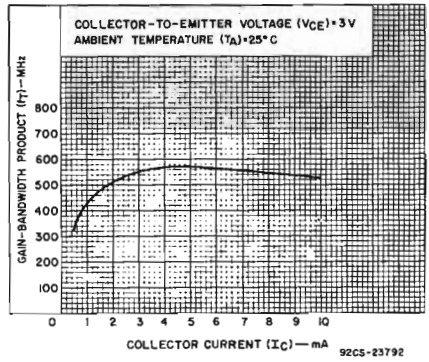


Fig.17 - Typical Gain-Bandwidth Product (f_T) vs Collector Current

RCA
Solid State
Division

Linear Integrated Circuits

CA3019

DIODE ARRAY

Monolithic Silicon

The CA3019 consists of one Diode "Quad" and two Isolated Diodes on a Common Substrate.

10-Pin TO-5

- Designed for use in Telemetry, Data-Processing, Instrumentation, and Communication Equipment
- Built-in Temperature Stability for Operation from -55°C to +125°C
- 10-Terminal TO-5 Package
- Hermetically Sealed
- Companion Application Note, ICAN-5299 "Application of the RCA CA3019 Integrated-Circuit Diode Array"

HIGHLIGHTS

- Excellent Diode Match
- Low Leakage Current
- Low Pedestal Voltage when Gating

APPLICATIONS

- Modulator
- Mixer
- Balanced Modulator
- Analog Switch
- Diode Gate for Chopper-Modulator Applications

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:
Any one diode unit . . . . . 20 max. mW
Total for device . . . . . 120 max. mW

TEMPERATURE RANGE:
Storage . . . . . -65 to +150 °C
Operating . . . . . -55 to +125 °C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

VOLTAGE: See Table

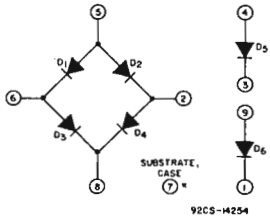


Fig.1 - Schematic Diagram for CA3019.

Absolute-Maximum Voltage Limits at $T_A = 25^{\circ}C$

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3	+12	7	-6
2	-3	+12	7	-6
3	-3	+12	7	-6
4	-3	+12	7	-6
5	-3	+12	7	-6
6	-3	+12	7	-6
7	-18	0	1, 2, 3, 6, 8	0
8	-3	+12	7	-6
9	-3	+12	7	-6
10	NO CONNECTION			
CASE	INTERNALLY CONNECTED TO TERMINAL 7 **DO NOT GROUND**			

ELECTRICAL CHARACTERISTICS, at an Ambient Temperature, T_A, of 25°C
CHARACTERISTICS APPLY FOR EACH DIODE UNIT, UNLESS OTHERWISE SPECIFIED.

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS	SPECIAL TEST CONDITIONS	LIMITS TYPE CA3019				TYPICAL CHARACTERISTICS CURVES
		Fig.		Min.	Typ.	Max.	Units	Fig.
DC Forward Voltage Drop	V_F	-	DC Forward Current (I_F) = 1 mA	-	0.73	0.78	V	2
DC Reverse Breakdown Voltage	$V_{(BR)R}$	-	DC Reverse Current (I_R) = -10 μA	4	6	-	V	-
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	-	DC Reverse Current (I_R) = -10 μA	25	80	-	V	-
DC Reverse (Leakage) Current	I_R	-	DC Reverse Voltage (V_R) = -4 V	-	0.0055	10	μA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	-	DC Reverse Voltage (V_R) = -4 V	-	0.010	10	μA	-
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F1} - V_{F2} \rvert$	-	DC Forward Current (I_F) = 1 mA	-	1	5	mV	-
Single Diode Capacitance	C_D	-	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) = -2 V	-	1.8	-	pF	4
Diode Quad-to-Substrate Capacitance	C_{DQ-I}		Frequency (f) = 1 MHz DC Reverse Voltage (V_R) between Terminal 2,5,6, or 8 of Diode Quad and Terminal 7 (Substrate) = -2 V					
			Terminal 2 or 6 to Terminal 7	-	4.4	-	pF	5
			Terminal 5 or 8 to Terminal 7	-	2.7	-	pF	6
Series Gate Switching Pedestal Voltage	V_S	7		-	10	-	mV	-

TYPICAL CHARACTERISTICS

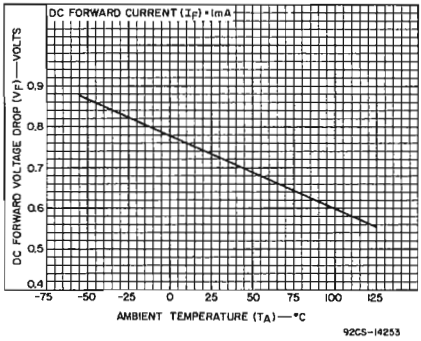


Fig.2 - DC Forward Voltage Drop (any Diode) vs Temperature for CA3019.

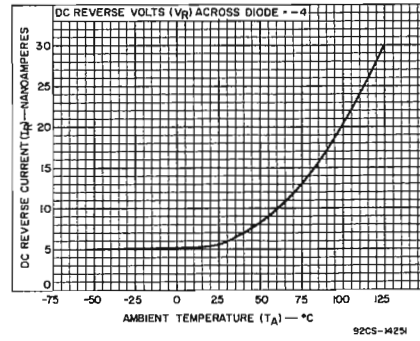


Fig.3 - Reverse (Leakage) Current (any Diode) vs Temperature for CA3019.

TYPICAL CHARACTERISTICS

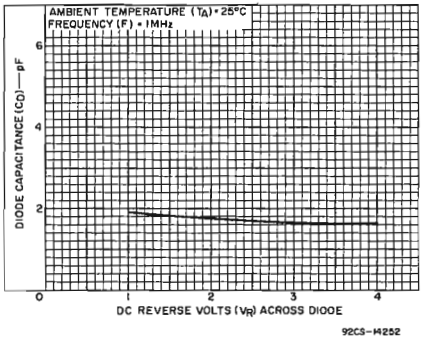


Fig.4 - Diode Capacitance (any Diode) vs Reverse Voltage for CA3019.

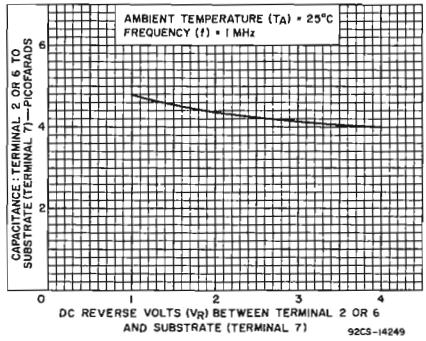


Fig.5 - Diode Quad-to-Substrate Capacitance vs Reverse Voltage for CA3019.

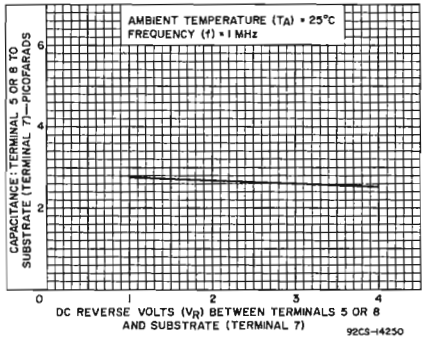


Fig.6 - Diode Quad-to-Substrate Capacitance vs Reverse Voltage for CA3019.

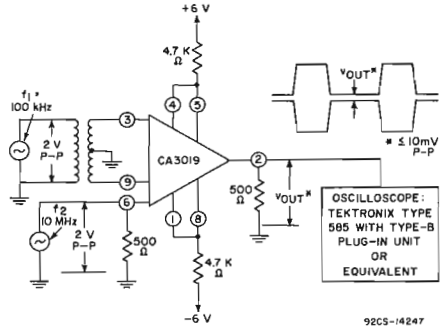


Fig.7 - Series Gate Switching Test Setup for CA3019.

RCA
Solid State
Division

Linear Integrated Circuits

CA3020
CA3020A

Multipurpose Wide-Band Power Amplifiers

Monolithic Silicon

The RCA-CA3020 and CA3020A are Integrated-Circuit, Multistage, Multipurpose, Wide-Band Power Amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable direct-coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The CA3020 and CA3020A are particularly suited for service as Class B power amplifiers. The CA3020A can provide a maximum power output of 1 watt from a 12-volt DC supply with a typical power gain of 75 dB. The CA3020 provides 0.5 watt power output from a 9-volt supply with the same power gain.

These types are supplied in hermetically sealed, TO-5 style 12-lead packages.

SCHEMATIC DIAGRAM FOR CA3020 AND CA3020A

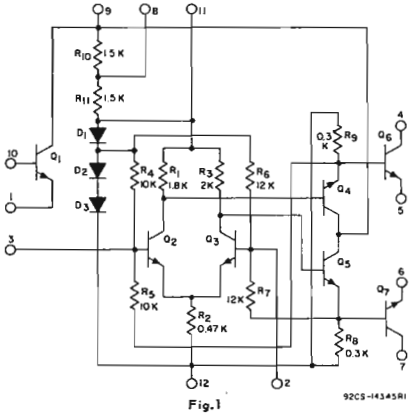


Fig.1

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ± 30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

MULTIPURPOSE WIDE-BAND POWER AMPLIFIERS

For Military, Industrial, and Commercial Equipment at Frequencies up to 8 MHz

12-Lead TO-5

FEATURES

- High power output - class B amplifier —
  CA3020 .... 0.5 watt typ. at V_{CC} = +9V
  CA3020A ... 1.0 watt typ. at V_{CC} = +12V
- Wide frequency range —
  Up to 8 MHZ with resistive loads
- High power gain ..... 75db typ.
- Single power supply for class B operation with transformer —
  CA3020 ..... 3 to 9V
  CA3020A ..... 3 to 12V
- Built-in temperature-tracking voltage regulator provides stable operation over -55°C to +125°C temperature range

APPLICATIONS

- AF power amplifiers for portable and fixed sound and communications systems
- Servo-control amplifiers
- Wide-band linear mixers
- Video power amplifiers
- Transmission-line driver amplifiers (balanced and unbalanced)
- Fan-in and fan-out amplifiers for computer logic circuits
- Lamp-control amplifiers
- Motor-control amplifiers
- Power multivibrator
- Power switches
- Companion Application Note, ICAN 5766 "Application of CA3020 and CA3020A Integrated Circuit Multipurpose Wide-Band Power Amplifiers."

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:

WITHOUT HEAT SINK	WITH HEAT SINK
At T_A = 25°C . . . . . 1 W	At T_C = 25°C . . . . . 2 W
Above T_A = 25°C . . . . . derate linearly 6.7 mW/°C	At T_C = 25°C to T_C = 55°C . . . . . 2 W
	Above T_C = 55°C . . derate linearly 16.7 mW/°C

TEMPERATURE RANGE:

Operating . . . . . -55°C to +125°C
Storage . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 12 is 0 to +10 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		*	*	*	*	*	*	*	▲ 0 -10/-12	+3 Note 1	*	+10 0
2			*	*	*	*	*	*	*	*	*	+2 -2
3				*	*	*	*	*	*	*	*	+2 -2
4					▲ +18/+25 0	*	*	*	*	*	*	▲ +18/+25 0
5						*	*	*	*	*	*	+3 Note 2
6							▲ 0 -18/-25	*	*	*	*	+3 Note 2
7								*	*	*	*	▲ +18/+25 0
8									Note 3	*	*	Note 3 0
9										+10 0	Note 1 0	+10/+12 0
10											*	+10 0
11												*
12												REF. SUB-STRATE

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	20
2	-	-
3	-	-
4	300	-
5	-	300
6	-	300
7	300	-
8	-	-
9	20	-
10	1	-
11	20	-
12	-	-

Note 1: This voltage is established by the maximum current rating.

Note 2: The emitters of Q_6 and Q_7 may be returned to a negative voltage supply through emitter resistors. Current into terminal No.9 should not be exceeded and the total device dissipation should not be exceeded.

Note 3: Terminal No.8 may be connected to terminals Nos.9, 11, or 12.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

▲ Higher value is for CA3020A.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS CA3020			LIMITS CA3020A			UNITS
		CIRCUIT AND PROCEDURE FIG.	DC SUPPLY VOLTAGE V_{CC1}	DC SUPPLY VOLTAGE V_{CC2}	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Collector-to-Emitter Breakdown Voltage, Q_6 & Q_7 at 10 mA	$V_{(BR)CER}$	2a	-	-	18	-	-	25	-	-	V
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1 mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V
Idle Currents, Q_6 & Q_7	I_4 IDLE I_7 IDLE	8	9.0	2.0	-	5.5	-	-	5.5	-	mA
Peak Output Currents, Q_6 & Q_7	I_4PK I_7PK	8	9.0	2.0	140	-	-	180	-	-	mA
Cutoff Currents, Q_6 & Q_7	I_4 CUTOFF I_7 CUTOFF	8	9.0	2.0	-	-	1.0	-	-	1.0	mA
Differetial Amplifier Current Drain	I_{CC1}	8	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA
Total Current Drain	I_{CC1} + I_{CC2}	8	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA
Differential Amplifier Input Terminal Voltages	V_2 V_3	8	9.0	2.0	-	1.11	-	-	1.11	-	V
Regulator Terminal Voltage	V_{11}	8	9.0	2.0	-	2.35	-	-	2.35	-	V
Q, Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	μA
Emitter-to-Base	I_{EBO}		3.0	-	-	-	0.1	-	-	0.1	
Collector-to-Base	I_{CBO}		3.0	-	-	-	0.1	-	-	0.1	
Forward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-	
Bandwidth at -3 dB Point	BW	9	6.0	6.0	-	8	-	-	8	-	MHz
Maximum Power Output	$P_{O(MAX)}$	10	6.0	6.0	200	300[a]	-	200	300[a]	-	mW
			9.0	9.0	400	550[a]	-	400	550[a]	-	
			9.0	12.0	-	-	-	800	1000[b]	-	
Sensitivity for P_{OUT} = 400 mW	e_{IN}	10	9.0	9.0	-	35[a]	55	-	-	-	mV
Sensitivity for P_{OUT} = 800 mW	e_{IN}	10	9.0	12.0	-	-	-	-	50[b]	100	mV
Input Resistance---- Terminal 3 to Ground	R_{IN3}	11	6.0	6.0	-	1000	-	-	1000	-	Ω
Junction-to-Case Thermal Resistance	θ_{J-C}	-	-	-	-	-	60	-	-	60	°C/W

a R_{CC} = 130 Ω

b R_{CC} = 200 Ω

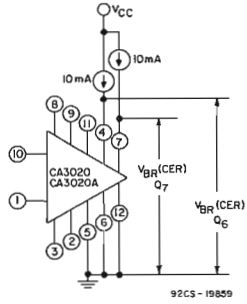


Fig.2

a. Collector-to-emitter breakdown voltage (Q_6 & Q_7) circuit

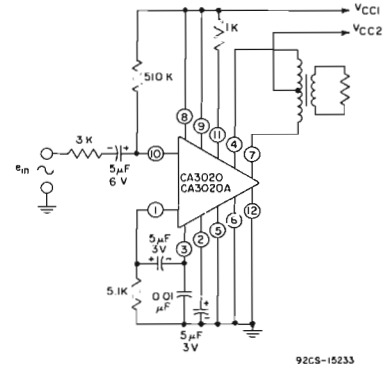


Fig.2

b. Typical audio amplifier circuit utilizing the CA3020 or CA3020A as an audio preamplifier and class B power amplifier

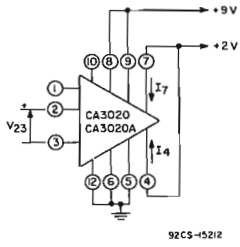
TYPICAL PERFORMANCE DATA*

An External Radiator Is Recommended for High Ambient Temperature Operation

CHARACTERISTICS	SYMBOLS	CA3020	CA3020A	UNITS
Power Supply Voltage	V_{CC_1}	9.0	9.0	V
	V_{CC_2}	9.0	12.0	
Zero Signal Current — Diff. Ampl.	I_{CC_1}	15	15	mA
Zero Signal Current — Output Ampl.	I_{CC_2}	24	24	
Maximum Signal Current — Diff. Ampl.	I_{CC_1}	16	16.6	mA
Maximum Signal Current — Output Ampl.	I_{CC_2}	125	140	
Maximum Power Output at THD = 10%	Po	550	1000	mW
Sensitivity	e_{IN}	35	45	mV
Power Gain	G_P	75	75	dB
Input Resistance	R_{IN}	55	55	kΩ
Efficiency	η	45	55	%
Signal-to-Noise Ratio	S/N	70	66	dB
THD at 150 mW level		3.1	3.3	%
Test Signal Frequency from 600Ω Generator		1000	1000	Hz
Equivalent Collector-to-Collector Load Resistance	R_{CC}	130	200	Ω

* Refer to Figs.8 through 12 for Measurement and Symbol Information.

TYPICAL TRANSFER CHARACTERISTICS



a. Test Setup

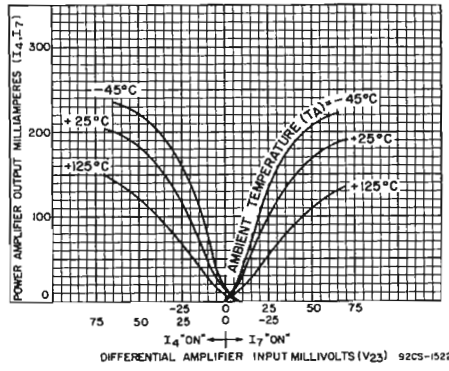
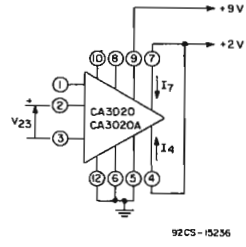


Fig.3 b. Characteristics with R_{10} shorted out



a. Test Setup

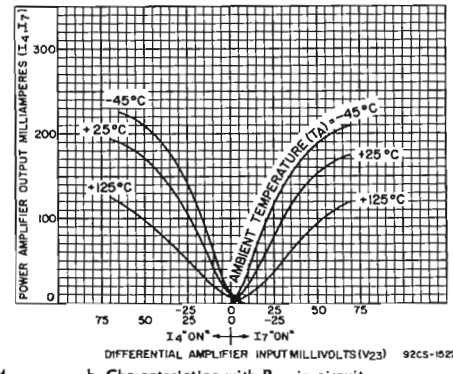
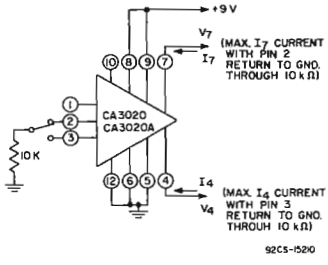


Fig.4 b. Characteristics with R_{10} in circuit

"MINIMUM DRIVE" TYPICAL CURRENT-VOLTAGE SATURATION CURVE



a. Test Setup

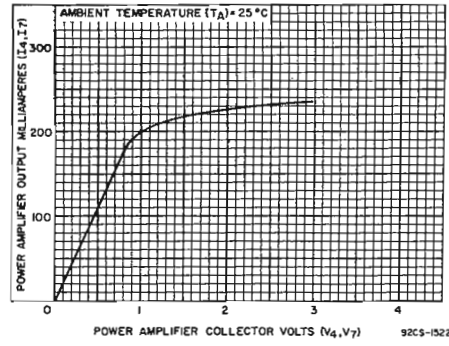
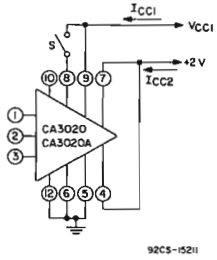
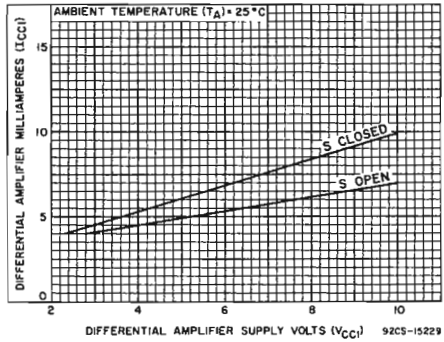


Fig.5 b. Characteristic

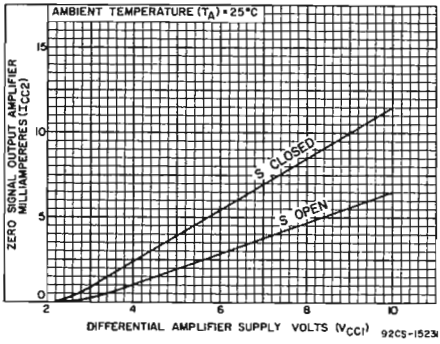
ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE



a. Test Setup



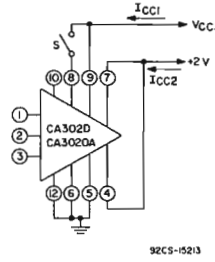
b. Differential Amplifier Characteristics



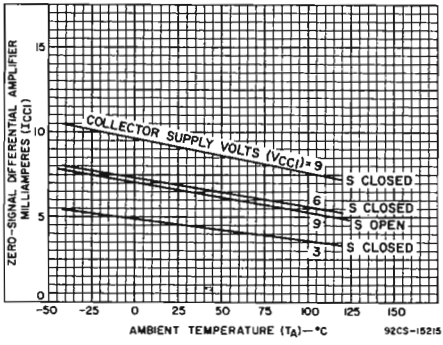
c. Output Amplifier Characteristics

Fig.6

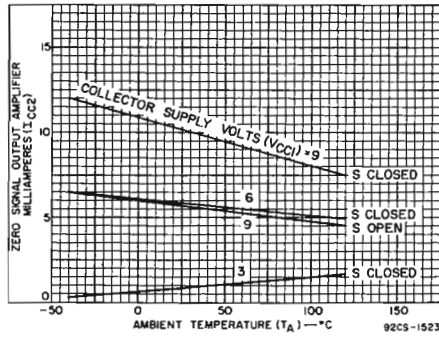
ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE



a. Test Setup



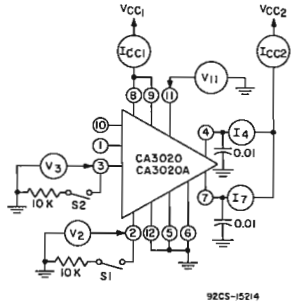
b. Differential Amplifier Characteristics



c. Output Amplifier Characteristics

Fig.7

STATIC CURRENT AND VOLTAGE TEST CIRCUIT



CURRENTS OR VOLTAGES	S1	S2
$I_{4\text{-IDLE}}$	open	open
$I_{7\text{-IDLE}}$	open	open
$I_{4\text{-PEAK}}$	open	close
$I_{7\text{-PEAK}}$	close	open
$I_{4\text{-CUTOFF}}$	close	open
$I_{7\text{-CUTOFF}}$	open	close

CURRENTS OR VOLTAGES	S1	S2
I_{CC1}	open	open
I_{CC2}	open	open
V_2	open	open
V_3	open	open
V_{11}	open	open

Fig.8

MEASUREMENT OF BANDWIDTH AT -3 dB POINTS

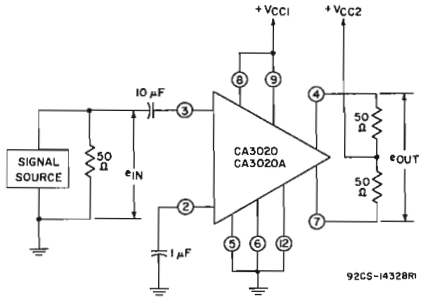


Fig.9

PROCEDURES:

1. Apply desired value of V_{CC_1} and V_{CC_2}
2. Apply 1 kHz input signal and adjust for e_{IN} = 5 mV (rms)
3. Record the resulting value of e_{OUT} in dB (reference value)
4. Vary input-signal frequency, keeping e_{IN} constant at 5 mV, and record frequencies above and below 1 kHz at which e_{OUT} decreases 3 dB below reference value.
5. Record bandwidth ss frequency range between -3 dB points.

MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN

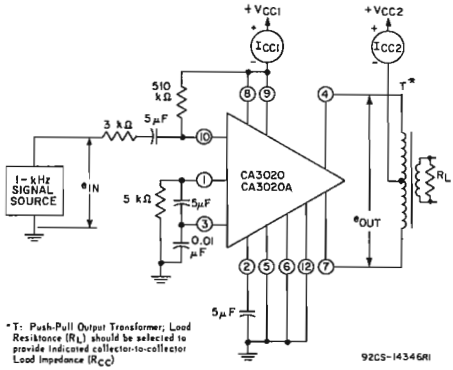


Fig.10

PROCEDURES:

Zero-Signal DC Current Drain

1. Apply desired Value of V_{CC_1} and V_{CC_2} and reduce e_{IN} to 0V
2. Record resulting values of I_{CC_1} and I_{CC_2} in mA as Zero-Signal DC Current Drain.

Maximum-Signal DC Current Drain, Maximum Power Output, Circuit Efficiency, Sensitivity, and Transducer Power Gain

1. Apply desired value of V_{CC_1} and V_{CC_2} and adjust e_{IN} to the value at which the Total Harmonic Distortion in the output of the amplifier = 10%
2. Record resulting value of I_{CC_1} and I_{CC_2} in mA as Maximum-Signal DC Current Drain
3. Determine resulting amplifier power output in watts and record as Maximum Power Output (P_{OUT})
4. Calculate Circuit Efficiency (η) in % as follows:

$$\eta = 100\,\frac{P_{OUT}}{V_{CC_1} I_{CC_1} + V_{CC_2} I_{CC_2}}$$

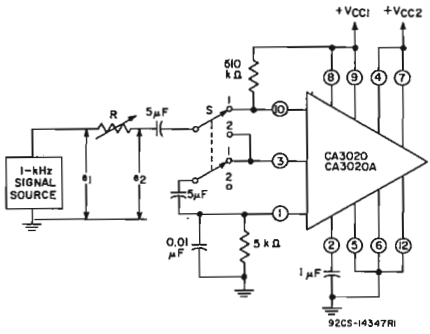
where P_{OUT} is in watts, V_{CC_1} and V_{CC_2} are in volts, and I_{CC_1} and I_{CC_2} are in amperes.

5. Record velue of e_{IN} in mV^2 (rms) required in Step 1 as Sensitivity (e_{IN})
6. Calculate Transducer Power Gain (G_p) in dB as follows:

$$G_p = 10 \log_{10} \frac{P_{OUT}}{P_{IN}}$$

where P_{IN} (in mW) = $\dfrac{e_{IN}^2}{3000 + R_{IN(10)}}$

MEASUREMENT OF INPUT RESISTANCE



PROCEDURES:

Input Resistance Terminal 10 to Ground ($R_{IN_{10}}$)

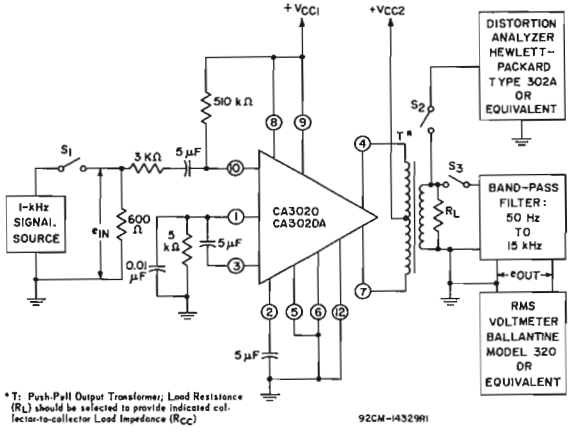
1. Apply desired value of V_{CC_1} and V_{CC_2} and set S in Position 1
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as $R_{IN_{10}}$

Input Resistance Terminal 3 to Ground (R_{IN_3})

1. Apply desired value of V_{CC_1} and V_{CC_2} set S in Position 2
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as R_{IN_3}

Fig.11

MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION



PROCEDURES:

Signal-to-Noise Ratio

1. Close S_1 and S_3; open S_2
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for an amplifier output of 150mW and record resulting value of E_{OUT} in dB as e_{OUT_1} (reference value)
4. Open S_1 and record resulting value of e_{OUT} in dB as e_{OUT_2}
5. Signal-to-Noise Ratio (S/N) = $20\log_{10} \frac{e_{OUT_1}}{e_{OUT_2}}$.

Total Harmonic Distortion

1. Close S_1 and S_2; open S_3
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for desired level amplifier output power
4. Record Total Harmonic Distortion (THD) in %

Fig.12

RCA Solid State Division

Linear Integrated Circuits

CA3021
CA3022
CA3023

Low-Power Video and Wideband Amplifiers

Monolithic Silicon

RCA-CA3021, CA3022, and CA3023 are low-power integrated-circuit wideband amplifiers with a wide range of applications in industrial, military, and commercial communications equipment. Each consists of a multistage amplifier circuit and unconnected diodes on a single chip, hermetically sealed in a 12-lead TO-5 style package. The diodes may be connected to provide limiting in FM applications.

The CA3021, CA3022, and CA3023 have the same maximum ratings, and differ principally in dissipation (dc power requirements) and bandwidth capability. All three devices are designed for operation over the temperature range from -55° C to +125° C.

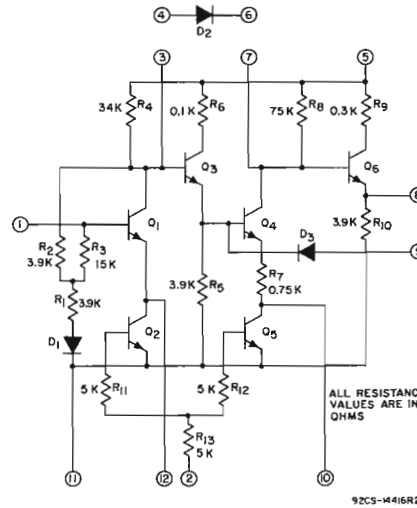
HIGHLIGHTS

- Low DC Power Drain:
  P_D { CA3021 = 4 mW typ. / CA3022 = 12.5 mW typ. / CA3023 = 35 mW typ. } at V_{CC} = 6 V
- Excellent frequency response:
  -3 dB BW { CA3021 = 2.4 MHz typ. / CA3022 = 7.5 MHz typ. / CA3023 = 16 MHz typ.
- High Voltage Gain:
  A { CA3021 = 56 dB typ. at 0.5 MHz / CA3022 = 57 dB typ. at 2.5 MHz / CA3023 = 53 dB typ. at 5 MHz
- Wide AGC Range: 33 dB typ.
- Only one power supply (4.5 to 12 V) required
- Hermetically Sealed 12-Lead TO-5-style package
- Operation from -55° C to +125° C

APPLICATIONS

- Gain-Controlled Linear Amplifiers
- AM/FM IF Amplifiers • Video Amplifiers • Limiters

SCHEMATIC DIAGRAM FOR CA3021, CA3022, AND CA3023



ABSOLUTE-MAXIMUM RATINGS:

OPERATING-TEMPERATURE RANGE	-55°C to +125°C	
STORAGE-TEMPERATURE RANGE	-65°C to +150°C	
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C	
DEVICE DISSIPATION, P_T	120 max.	mW
INPUT-SIGNAL VOLTAGE	-3, +3 max.	V
DC VOLTAGES AND CURRENTS	See Table Below	

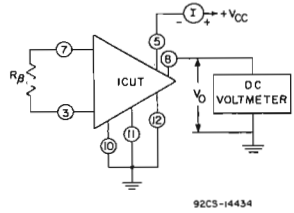
	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS	
TERMINAL	NEGATIVE	POSITIVE	TERMINAL	CONDITIONS
1	-3V	+3V	1	Connected to Voltage Source through 100Ω Resistor
			5	+12V
			10, 11, 12	Ground
2	-3V	+12V	5	+12V
			10, 11, 12	Ground
3	0V	+12V	5	+12V
			10, 11, 12	Ground
4	-12V	+12V	6, 11	Ground
	10 max. mA			
5	0V	+18V	10, 11, 12	Ground
6	-12V	+12V	5, 11	Ground
	10 max. mA			

	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS	
TERMINAL	NEGATIVE	POSITIVE	TERMINAL	CONDITIONS
7	0V	+12V	5	+12V
			10, 11, 12	Ground
8	20 max. mA		5	+12V
			10, 11, 12	Ground
9	-0.5V	+3V	5	+12V
			10, 11, 12	Ground
10	0V	+4V	2,5	+12V
			11	Ground
11	-6V	+12V	2	Ground
			5	+12V
12	0V	+4V	2,5	+12V
			11	Ground

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, V_{CC} = +6V, unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS									UNITS	TYPICAL CHARACTERISTIC CURVE
		TEST SETUP AND PROCEDURE	FEEDBACK RESISTANCE (R_β) BETWEEN TERMINALS 3 AND 7	FREQUENCY f	CA3021 (TA5219)			CA3022 (TA5236)			CA3023 (TA5218)				
		Fig.	Ω	MHz	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Fig.
Device Dissipation	P_T	2	∞	–	1	4	8	–	–	–	–	–	–	mW	3a,d
			∞	–	–	–	–	5	12.5	24	–	–	–	mW	3b,d
			○	–	–	–	–	–	–	–	24	35	48	mW	3c,d
Quiescent Output Voltage	V_O	2	39k	–	–	2.2	–	–	–	–	–	–	–	V	–
			10k	–	–	–	–	–	1.9	–	–	–	–	V	
			4.7k	–	–	–	–	–	–	–	–	1.3	–	V	
AGC Source Current	I_{AGC}	4	V_{AGC} = +6V		–	0.8	–	–	0.8	–	–	0.8	–	mA	–
Voltage Gain	A	5	560k	0.5	50	56	–	–	–	–	–	–	–	dB	6a
			39k	0.8	40	46	–	–	–	–	–	–	–	dB	6a,d
			39k	2.5	–	–	–	50	57	–	–	–	–	dB	6b
			10k	3	–	–	–	40	44	–	–	–	–	dB	6b,d
			18k	5	–	–	–	–	–	–	50	53	–	dB	6c
			4.7k	10	–	–	–	–	–	–	40	44	–	dB	6c,d
Bandwidth at -3 dB Point	BW	5	39k	–	0.8	2.4	–	–	–	–	–	–	–	MHz	6a
			10k	–	–	–	–	3	7.5	–	–	–	–	MHz	6b
			4.7k	–	–	–	–	–	–	–	10	16	–	MHz	6c
Input-Impedance Components: Input Resistance	R_{IN}	7	39k	1	–	4000	–	–	–	–	–	–	–	Ω	–
			10k	5	–	–	–	–	1300	–	–	–	–	Ω	
			4.7k	10	–	–	–	–	–	–	–	300	–	Ω	
Input-Impedance Components: Input Capacitance	C_{IN}	7	39k	1	–	11	–	–	–	–	–	–	–	pF	–
			10k	5	–	–	–	–	18	–	–	–	–	pF	
			4.7k	10	–	–	–	–	–	–	–	13	–	pF	
Output Resistance	R_{OUT}	8	39k	1	–	300	–	–	–	–	–	–	–	Ω	–
			10k	5	–	–	–	–	120	–	–	–	–	○	
			4.7k	10	–	–	–	–	–	–	–	100	–	○	
Noise Figure	NF	9	39k	1	–	4.2	8.5	–	–	–	–	–	–	dB	–
			10k	1	–	–	–	–	4.4	8.5	–	–	–	dB	
			4.7k	1	–	–	–	–	–	–	–	6.5	8.5	dB	
AGC Range	AGC	10	–	1	–	33	–	–	–	–	–	–	–	dB	–
			–	5	–	–	–	–	33	–	–	–	–	dB	
			–	10	–	–	–	–	–	–	–	33	–	dB	
Maximum Output Voltage (RMS Value)	V_{out}	5	39k	1	–	0.6	–	–	–	–	–	–	–	$V_{(rms)}$	–
			10k	5	–	–	–	–	0.7	–	–	–	–	$V_{(rms)}$	
			4.7k	10	–	–	–	–	–	–	–	0.5	–	$V_{(rms)}$	

TEST SETUP FOR MEASUREMENT OF DEVICE DISSIPATION AND QUIESCENT OUTPUT VOLTAGE



$P_T = V_{CC}\ (I)$

Fig.2

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3022

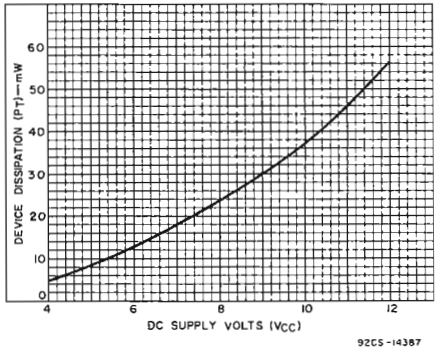


Fig.3(b)

DEVICE DISSIPATION VS TEMPERATURE FOR CA3021, CA3022, AND CA3023

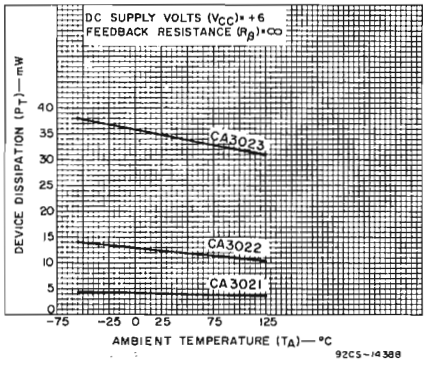


Fig.3(d)

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3021

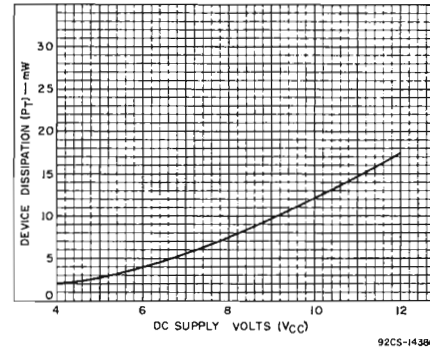


Fig.3(a)

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3023

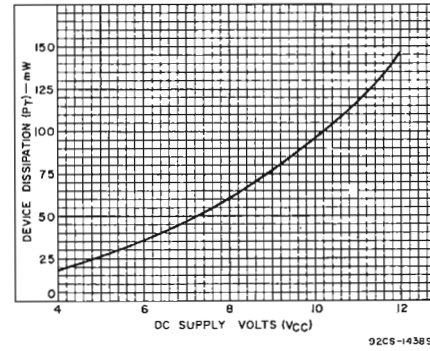
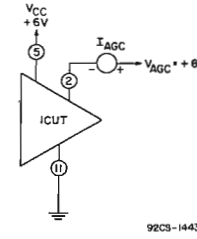


Fig.3(c)

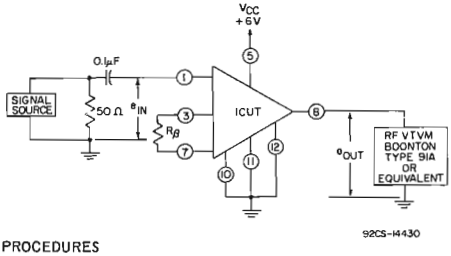
TEST SETUP FOR MEASUREMENT OF AGC SOURCE CURRENT



I_{AGC} IS THE CURRENT FLOWING INTO TERMINAL 2.

Fig.4

TEST SETUP FOR MEASUREMENTS OF VOLTAGE-GAIN, -3dB BANDWIDTH, AND MAXIMUM OUTPUT VOLTAGE



PROCEDURES

Voltage Gain:

(a) Set e_{in} = 0.5 mVat frequency specified, read e_{out} Voltage Gain

(A) = 20 $\text{Log}_{10} \frac{e_{out}}{e_{in}}$

Bandwidth:

(a) Set e_{out} to a convenient reference voltage at f = 100 kHz and record corresponding value of e_{in}.

(b) Increase the frequency, keeping e_{in} constant until e_{out} drops 3-dB. Record Bandwidth.

Fig. 5

VOLTAGE GAIN VS FREQUENCY FOR CA3021

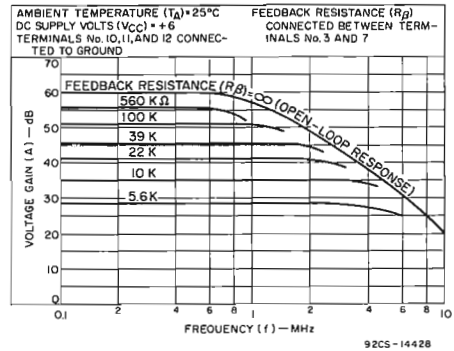


Fig.6(a)

VOLTAGE GAIN VS FREQUENCY FOR CA3022

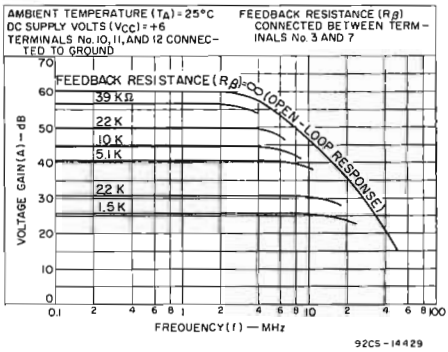


Fig.6(b)

VOLTAGE GAIN VS FREQUENCY FOR CA3023

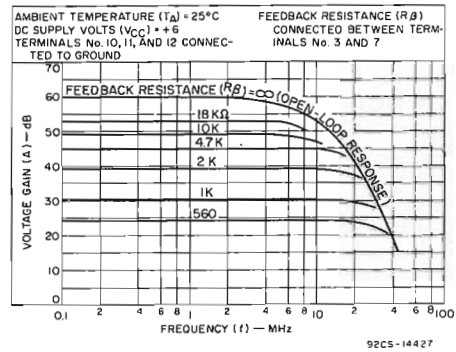


Fig.6(c)

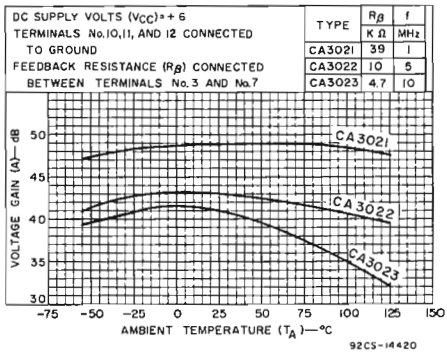
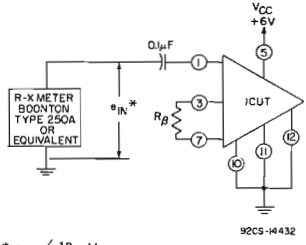


Fig.6(d)

VOLTAGE GAIN VS TEMPERATURE FOR CA3021, CA3022, AND CA3023

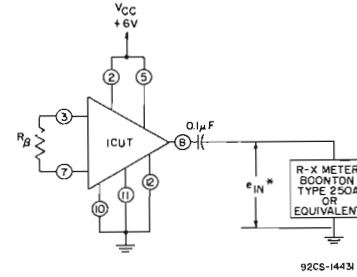
TEST SETUP FOR MEASUREMENT OF INPUT-IMPEDANCE COMPONENTS



* $e_{in} \leq 10$ mV

Fig.7

TEST SETUP FOR MEASUREMENT OF OUTPUT RESISTANCE

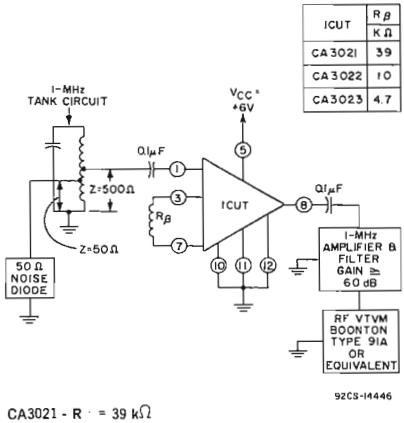


* $e_{in} \leq 10$ mV

Fig.8

TEST SETUP FOR MEASUREMENT OF NOISE FIGURE

ICUT	Rβ KΩ
CA3021	39
CA3022	10
CA3023	4.7

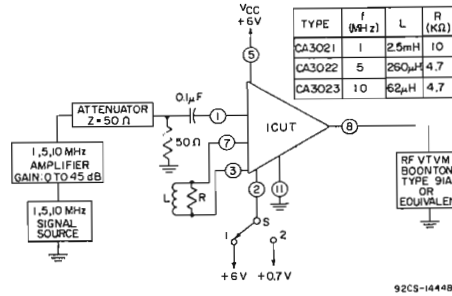


CA3021 - Rβ = 39 kΩ
CA3022 - Rβ = 10 kΩ
CA3023 - Rβ = 4.7 kΩ

Fig.9

TEST SETUP FOR MEASUREMENT OF AGC RANGE

TYPE	f (MHz)	L	R (KΩ)
CA3021	1	2.5mH	10
CA3022	5	260μH	4.7
CA3023	10	62μH	4.7



$$\text{AGC RANGE} = 20 \log_{10} \frac{\text{A WITH S IN POSITION 1}}{\text{A WITH S IN POSITION 2}}$$

(A = VOLTAGE GAIN)

	f MHz
CA3021	1
CA3022	5
CA3023	10

Fig. 10

RCA
Solid State
Division

Linear Integrated Circuits

CA3026
CA3054

Transistor Array

Monolithic Silicon

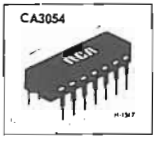
The CA3026 and CA3054 each consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300 MHz. These features make the CA3026 and CA3054 useful from dc to 120 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3026 and CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

DUAL INDEPENDENT DIFFERENTIAL AMPLIFIERS

For Low-Power Applications at Frequencies from DC to 120 MHz

12-Lead TO-5



14-Lead
Dual-In-Line
Plastic Package

APPLICATIONS

- Dual sense amplifiers
- Dual Schmitt triggers
- Multifunction combinations -- RF/Mixer/Oscillator; Converter/IF
- IF amplifiers (differential and/or cascade)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascade limiters
- Synchronous detectors
- Pairs of balanced mixers
- Synthesizer mixers
- Balanced (push-pull) cascade amplifiers

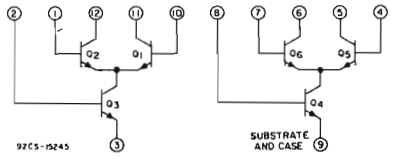


Fig.1a - Schematic Diagram for CA3026.

FEATURES

- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Maximum input offset voltage -- ±5 mV
- Full military temperature range capability -- -55°C to +125°C
- Limited temperature range -- 0°C to 85°C for CA3054

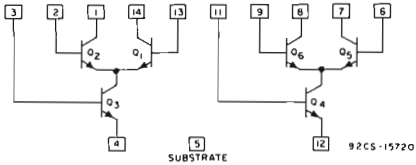


Fig.1b - Schematic Diagram for CA3054.

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT $T_A = 25^oC$

	CA3026	CA3054	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55^oC$	Derate at 5	6.67	$mW/^oC$
Temperature Range:			
Operating	-55 to + 125		^oC
Storage	-65 to + 150		^oC
Lead Temperature (During Soldering):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265		^oC

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 and CA3054 is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.*

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1† and horizontal terminal 3† is +15 to -5 volts.

† For CA3026; corresponding terminals for CA3054 are vertical terminal 2 and horizontal terminal 4.

CA3054 TERMINAL No. →		13	14	1	2	3	4	6	7	8	9	11	12	5
↓	CA3026 TERMINAL No. →	10	11	12	1	2	3	4	5	6	7	8	Note 1 9	Note 1 9
13	10		0 -20	*	+5 -5	*	+15 -5	*	*	*	*	*	*	*
14	11			*	*	*	+20 0	*	*	*	*	*	*	+20 0
1	12				+20 0	*	+20 0	*	*	*	*	*	*	+20 0
2	1					*	+15 -5	*	*	*	*	*	*	*
3	2						+1 -5	*	*	*	*	*	*	*
4	3							*	*	*	*	*	*	*
6	4								0 -20	*	+5 -5	*	+15 -5	*
7	5									*	*	*	*	+20 0
8	6										+20 0	*	*	+20 0
9	7											*	+15 -5	*
11	8												+1 -5	*
12	9													*
5	9													Ref Sub-strate

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Note 1: In the CA3026 terminal No.9 is connected to the emitter of Q_4, the reference substrate, and the case; therefore, the case should not be grounded. Two terminal 9 columns (CA3026) appear in the voltage rating chart because it is a composite chart for both the CA3026 and the CA3054. Wherever an asterisk is shown in one column 9 and a rating is shown in the other column 9, the asterisk should be ignored.

Maximum Current Ratings

CA3054 TERMINAL No.●	CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
13	10	5	0.1
14	11	50	0.1
1	12	50	0.1
2	1	5	0.1
3	2	5	0.1
4	3	0.1	-50
6	4	5	0.1
7	5	50	0.1
8	6	50	0.1
9	7	5	0.1
11	8	5	0.1
12	9	0.1	50

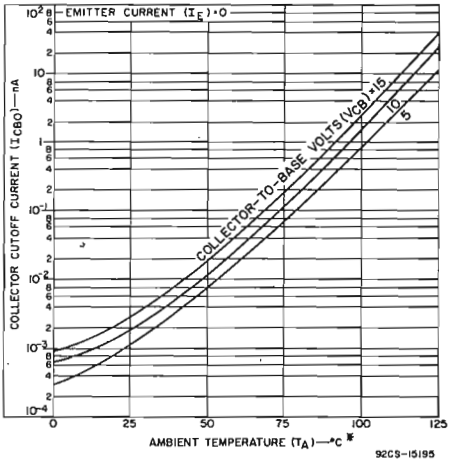
● Terminal No.10 of CA3054 is not used

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIRCUIT FIG.	CA3026 CA3054 LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC CHARACTERISTICS								
For Each Differential Amplifier								
Input Offset Voltage	V_{IO}	V_{CB} = 3 V; $I_{E(Q3)} \simeq I_{E(Q4)}$ = 2 mA	-	-	0.45	5	mV	6
Input Offset Current	I_{IO}		-	-	0.3	2	μA	7
Input Bias Current	I_I		-	-	10	24	μA	3
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$		-	-	0.98 to 1.02	-	-	3
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		-	-	1.1	-	μV/°C	5
For Each Transistor								
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CB} = 3 V; I_C = 50 μA	-	-	0.630	0.700	V	6
		1 mA	-	-	0.715	0.800		
		3 mA	-	-	0.750	0.850		
		10 mA	-	-	0.800	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3 V, I_C = 1 mA	-	-	-1.9	-	μV/°C	4
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	-	0.002	100	nA	2
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	-	15	24	-	V	-
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	-	20	60	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	-	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	-	5	7	-	V	-
DYNAMIC CHARACTERISTICS								
Common-Mode Rejection Ratio For Each Amplifier	CMR	V_{CC} = 12 V; V_{EE} = -6 V; V_x = -3.3 V; f = 1 kHz	8a	-	100	-	dB	8b
AGC Range, One Stage	AGC		9a	-	75	-	dB	9b
Voltage Gain, Single Stage Double-Ended Output	A		9a	-	32	-	dB	9b
AGC Range, Two Stage	AGC		10a	-	105	-	dB	10b
Voltage Gain, Two Stage Double-Ended Output	A		10a	-	60	-	dB	10b
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor)								
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	-	110	-	-	11
Short-Circuit Input Impedance	h_{ie}		-	-	3.5	-	kΩ	11
Open-Circuit Output Impedance	h_{oe}		-	-	15.6	-	μmho	11
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	-	1.8×10^{-4}	-	-	11

DYNAMIC CHARACTERISTICS CONT'D.									
1/f Noise Figure (For Single Transistor)	NF	f = 1 kHz, V_{CE} = 3 V	-	-	3.25	-	dB	-
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 3 V, I_C = 3 mA	-	-	550	-	MHz	12
Admittance Characteristics; Differential Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Each Collector $I_C \approx$ 1.25 mA f = 1 MHz	-	-	-20+j0	-	mmho	13a
Input Admittance	y_{11}		-	-	0.22+j0.1	-	mmho	13b
Output Admittance	y_{22}		-	-	0.01+j0	-	mmho	13c
Reverse Transfer Admittance	y_{12}		-	-	-0.003 +j0	-	mmho	13d
Admittance Characteristics; Cascode Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Total Stage $I_C \approx$ 2.5 mA f = 1 MHz	-	-	68-j0	-	mmho	14a
Input Admittance	y_{11}		-	-	0.55+j0	-	mmho	14b
Output Admittance	y_{22}		-	-	0+j0.02	-	mmho	14c
Reverse Transfer Admittance	y_{12}		-	-	0.004-j0.005	-	μmho	14d
Noise Figure	NF	f = 100 MHz	-	-	8	-	dB	-

TYPICAL STATIC CHARACTERISTICS



* For CA3054: use data from 0°C to 85°C only

Fig.2 - Collector-to-base cutoff current vs ambient temperature for each transistor.

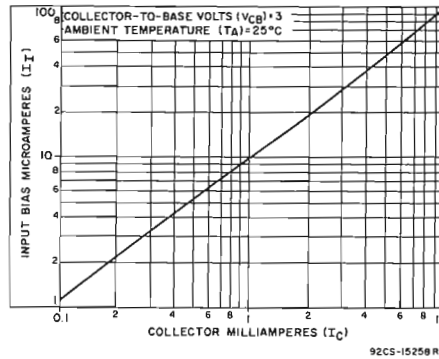


Fig.3 - Input bias current characteristic vs collector current for each transistor.

TYPICAL STATIC CHARACTERISTICS

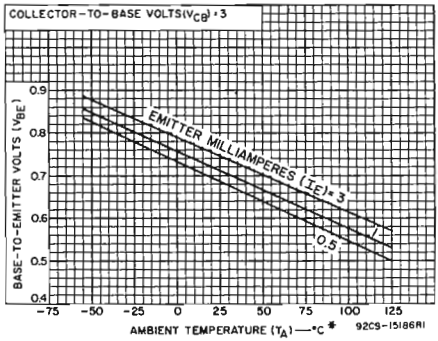


Fig.4 - Base-to-emitter voltage characteristic for each transistor vs ambient temperature.

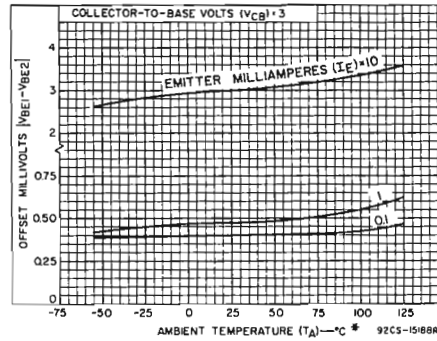


Fig.5 - Offset voltage characteristic vs ambient temperature for differential pairs.

* For CA3054: use data from 0°C to 85°C only

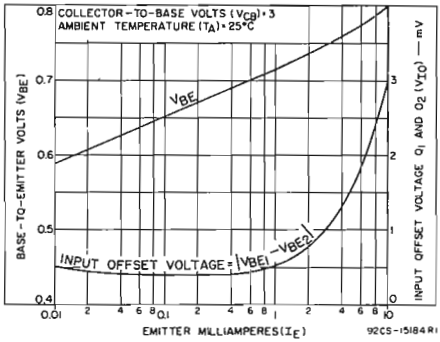


Fig.6 - Static base-to-emitter voltage characteristic and input offset voltage for differential pairs vs emitter current.

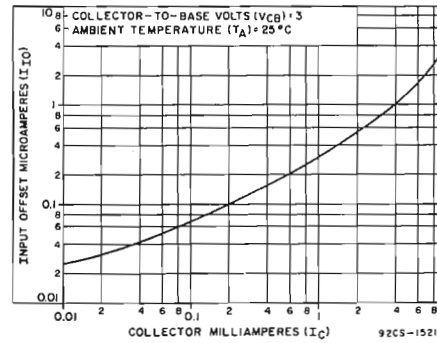
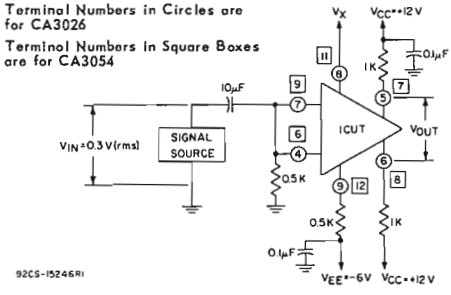


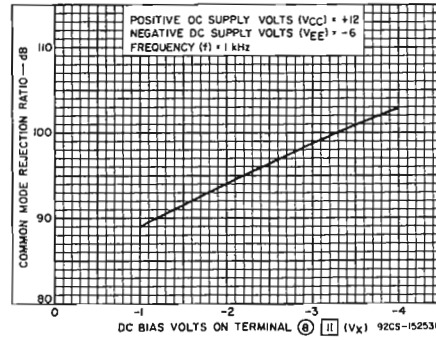
Fig.7 - Input offset current for matched differential pairs vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS

COMMON MODE REJECTION RATIO



(a) Test setup

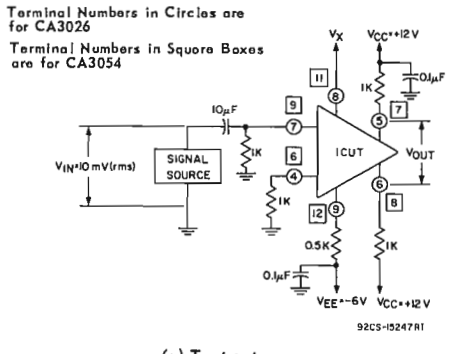


(b) Characteristic

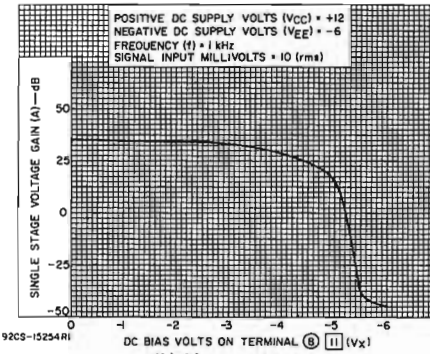
Fig.8

TYPICAL DYNAMIC CHARACTERISTICS (cont'd)

SINGLE-STAGE VOLTAGE GAIN



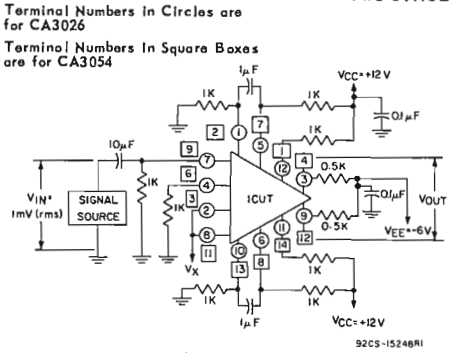
(a) Test setup



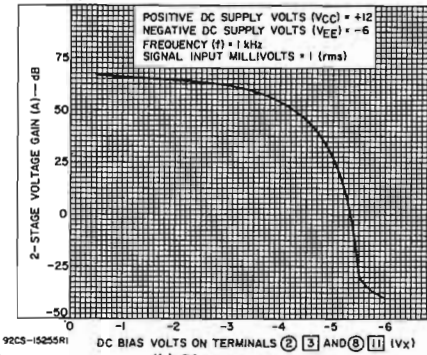
(b) Characteristic

Fig.9

TWO-STAGE VOLTAGE GAIN



(a) Test setup



(b) Characteristic

Fig.10

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

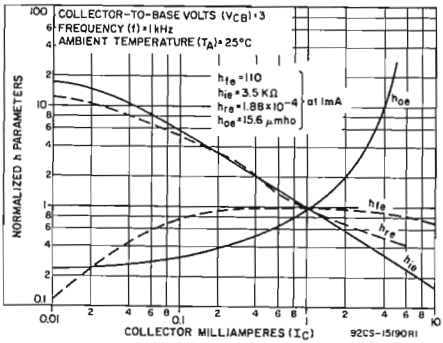


Fig.11 - Forward current-transfer ratio (h_{fe}), short-circuit input impedance (h_{ie}), open-circuit output impedance (h_{oe}), and open-circuit reverse voltage-transfer ratio (h_{re}) vs collector current for each transistor.

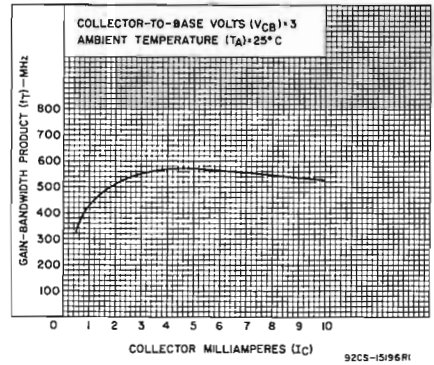


Fig.12 - Gain-bandwidth product (f_T) vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER

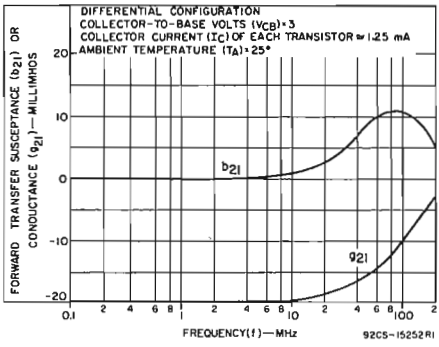


Fig.13(a) - Forward transfer admittance (Y_{21}) vs frequency.

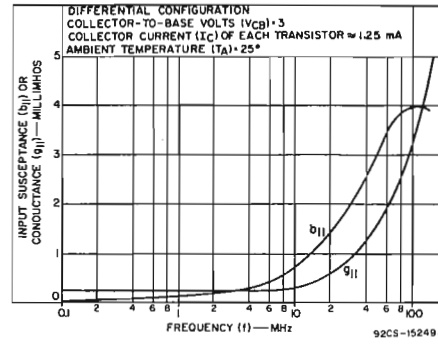


Fig.13(b) - Input admittance (Y_{11}).

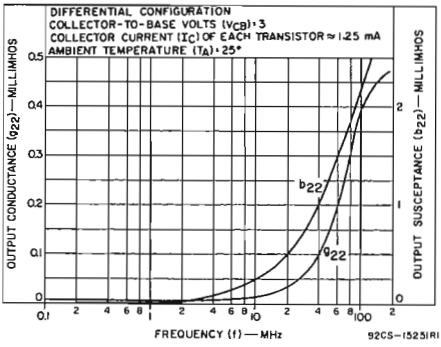


Fig.13(c) - Output admittance (Y_{22}) vs frequency.

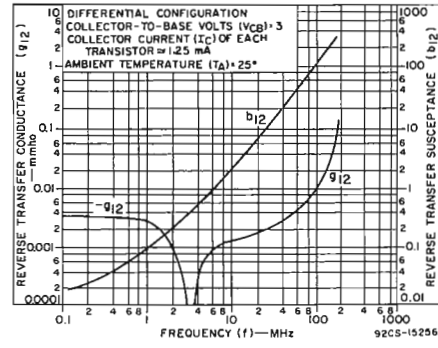


Fig.13(d) - Reverse transfer admittance (Y_{12}) vs frequency.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER

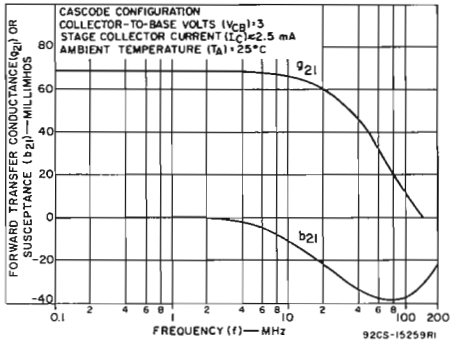


Fig.14(a) - Forward transfer admittance (Y_{21}) vs frequency.

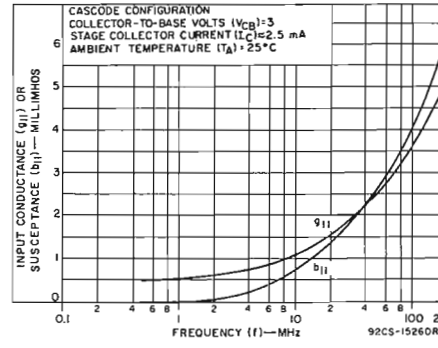


Fig.14(b) - Input admittance (Y_{11}) vs frequency.

TYPICAL CHARACTERISTICS FOR EACH CASCODE AMPLIFIER (cont'd)

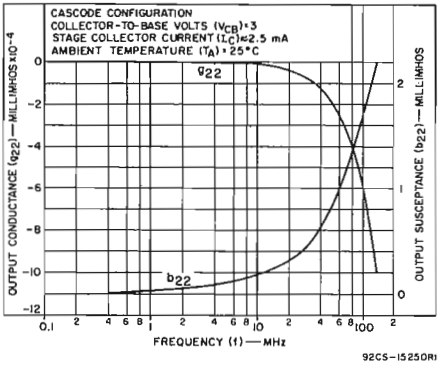


Fig.14(c) - Output admittance (Y_{22}) vs frequency.

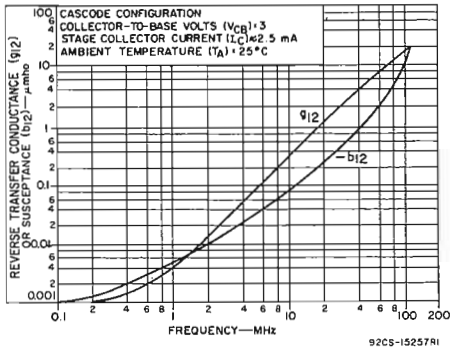


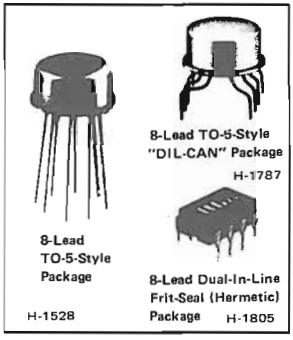
Fig.14(d) - Reverse transfer admittance (Y_{12}) vs frequency.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA3028A, CA3028AF, CA3028AS
CA3028B, CA3028BF, CA3028BS
CA3053, CA3053F, CA3053S



DIFFERENTIAL/CASCODE AMPLIFIERS

For Communications and Industrial Equipment at Frequencies from DC to 120 MHz

FEATURES

- Controlled for Input Offset Voltage, Input Offset Current, and Input Bias Current (CA3028B)
- Balanced Differential Amplifier Configuration with Controlled Constant-Current Source to Provide Unexcelled Versatility
- Single- and Dual-Ended Operation
- Operation from DC to 120 MHz
- Balanced-AGC Capability
- Wide Operating-Current Range

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from dc to 120 MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical dc and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

The CA3028A, CA3028B, and CA3053 are supplied in a hermetic 8-lead TO-5-style package. The "F" versions are supplied in a frit-seal package and the "S" versions in formed-lead (DIL-CAN) packages.

APPLICATIONS

- RF and IF Amplifiers (Differential or Cascode)
- DC, Audio, and Sense Amplifiers
- Converter in the Commercial FM Band
- Oscillator • Mixer • Limiter
- Companion Application Note, ICAN 5337 "Applicotion of the RCA CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations.

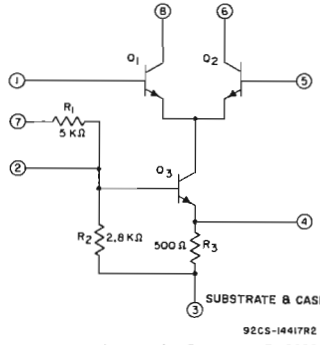


Fig. 1 - Schematic diagram for CA3028A, CA3028B and CA3053.

ABSOLUTE MAXIMUM RATINGS AT $T_A = 25^oC$

DISSIPATION:

At T_A up to 55°C
(CA3028AF, CA3028BF, CA3053F) ..... 750 mW

At $T_A > 55^oC$
(CA3028AF, CA3028BF, CA3053F) ..... Derate linearly 6.67 mW/°C

At T_A up to 85°C
(CA3028A, CA3028B, CA3053) ..... 450 mW

At $T_A > 85^oC$
(CA3028A, CA3028B, CA3053) Derate linearly 5 mW/°C

AMBIENT-TEMPERATURE RANGE:

Operating ..... −55°C to +125°C

Storage ..... −65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15▲	0 to -15▲	0 to -15▲	+5 to -5	*	*	+20⊕ to 0
2			+5 to -11	+5 to -1	+15♦ to 0	*	+15♦ to 0	*
3‡				+10 to 0	+15♦ to 0	+30● to 0	+15♦ to 0	+30● to 0
4					+15♦ to 0	*	*	*
5						+20⊕ to 0	*	*
6							*	*
7								*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

▲ Limit is -12V for CA3053

⊕ Limit is +15V for CA3053

♦ Limit is +12V for CA3053

● Limit is +24V for CA3028A and +18V for CA3053

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS $+V_{CC}$	SPECIAL TEST CONDITIONS $-V_{EE}$	LIMITS TYPE CA3028A Min.	LIMITS TYPE CA3028A Typ.	LIMITS TYPE CA3028A Max.	LIMITS TYPE CA3028B Min.	LIMITS TYPE CA3028B Typ.	LIMITS TYPE CA3028B Max.	LIMITS TYPE CA3053 Min.	LIMITS TYPE CA3053 Typ.	LIMITS TYPE CA3053 Max.	UNITS	TYPICAL CHARACTERISTICS CURVES Fig.
STATIC CHARACTERISTICS															
Input Offset Voltage	V_{IO}	2	6V 12V	6V 12V	- -	- -	- -	- -	0.98 0.89	5 5	- -	- -	- -	mV	4
Input Offset Current	I_{IO}	3a	6V 12V	6V 12V	- -	- -	- -	- -	0.56 1.06	5 6	- -	- -	- -	μA	4
Input Bias Current	I_I	3a	6V 12V	6V 12V	- -	16.6 36	70 106	- -	16.6 36	40 80	- -	- -	- -	μA	5a
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	29 36	85 125		5b
Quiescent Operating Current	I_6 or I_8	3a	6V 12V	6V 12V	0.8 2	1.25 3.3	2 5	1 2.5	1.25 3.3	1.5 4	- -	- -	- -	mA	6a 7
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	1.2 2.0	2.2 3.3	3.5 5.0		6b
AGC Bias Current (Into Constant-Current Source Terminal No.7)	I_7	8a	12V 12V	V_{AGC} =+9 V_{AGC} = +12	- -	1.28 1.65	- -	- -	1.28 1.65	- -	- -	- -	- -	mA	8b
		-	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	1.15 1.55	- -		-
Input Current (Terminal No.7)	I_7	-	6V 12V	6V 12V	0.5 1	0.85 1.65	1 2.1	0.5 1	0.85 1.65	1 2.1	- -	- -	- -	mA	-
Device Dissipation	P_T	3a	6V 12V	6V 12V	24 120	36 175	54 260	24 120	36 175	42 220	- -	- -	- -	mW	9
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	50 100	80 150		-

ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A Min.	Typ.	Max.	LIMITS TYPE CA3028B Min.	Typ.	Max.	UNITS	TYPICAL CHARAC-TERISTICS CURVE Fig.
DYNAMIC CHARACTERISTICS												
Power Gain	G_P	10a	f = 100 MHz	Cascode	16	20	-	16	20	-	dB	10b
		11a,d	V_{CC} = +9V	Diff.-Ampl.	14	17	-	14	17	-		11b,e
		10a	f = 10.7 MHz	Cascode	35	39	-	35	39	-	dB	10b
		11a	V_{CC} = +9V	Diff.-Ampl.	28	32	-	28	32	-		11b
Noise Figure	NF	10a	f = 100 MHz	Cascode	-	7.2	9	-	7.2	9	dB	10c
		11a,d	V_{CC} +9V	Diff.-Ampl.	-	6.7	9	-	6.7	9		11c,e
Input Admittance	Y_{11}	-	f = 10.7 MHz, V_{CC} = +9V	Cascode				-	0.6 + j 1.6	-	mmho	12
		-		Diff.-Ampl.				-	0.5 + j 0.5	-		13
Reverse Transfer Admittance	Y_{12}	-		Cascode				-	0.0003 - j0	-	mmho	14
		-		Diff.-Ampl.				-	0.01 - j0.0002	-		15
Forward Transfer Admittance	Y_{21}	-		Cascode				-	99 - j18	-	mmho	16
		-		Diff.-Ampl.				-	37 + j0.5	-		17
Output Admittance	Y_{22}	-		Cascode				-	0. + j0.08	-	mmho	18
		-		Diff.-Ampl.				-	0.04 + j0.23	-		19
Power Output (Untuned)	P_o	20a	f = 10.7 MHz	Diff.-Ampl. 50Ω Input-Output	-	5.7	-	-	5.7	-	mW	20b
AGC Range (Max. Power Gain to Full Cutoff)	AGC	21a	V_{CC} = +9V	Diff.-Ampl.	-	62	-	-	62	-	dB	21b
Voltage Gain, at f = 10.7 MHz	A	22a	f = 10.7 MHz, V_{CC} = +9V, R_L = 1 kΩ	Cascode	-	40	-	-	40	-	dB	22b
		22c		Diff.-Ampl.	-	30	-	-	30	-		22d
Voltage Gain, Differential at f = 1 kHz	A	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	35	38	42	dB	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	40	42.5	45		
Max. Peak-to-Peak Output Voltage at f = 1 kHz	V_o(P-P)	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	7	11.5	-	V_{P-P}	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	15	23	-		
Bandwidth at -3 dB point	BW	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	-	7.3	-	MHz	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	-	8	-		
Common-Mode Input-Voltage Range	V_{CMR}	24	V_{CC} = +6V, V_{EE} = -6V		-	-	-	-2.5	(-3.2 - 4.5)	4	V	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	-5	(-7 - 9)	7		
Common-Mode Rejection Ratio	CMR	24	V_{CC} = +6V, V_{EE} = -6V		-	-	-	60	110	-	dB	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	60	90	-		
Input Impedance at f = 1 kHz	Z_{IN}		V_{CC} = +6V, V_{EE} = -6V		-	-	-	-	5.5	-	kΩ	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	3	-		
Peak-to-Peak Output Current	I_{P-P}		V_{CC} = +9V	f = 10.7 MHz, e_{in} = 400 mV Diff.-Ampl.	2	4	7	2.5	4	6	mA	-
			V_{CC} = +12V		3.5	6	10 -	4.5	6	8		

ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3053 Min.	Typ.	Max.	UNITS	TYPICAL CHARAC-TERISTICS CURVE Fig.
DYNAMIC CHARACTERISTICS										
Power Gain		G_P	10a	f = 10.7 MHz	Cascode	35	39	-	dB	
			11a	V_{CC} = +9V	Diff.-Ampl.	28	32			
Input Admittance		Y_{11}	-	f = 10.7 MHz V_{CC} = +9V	Cascode	-	0.6 + j 1.6	-	mmho	12
			-		Diff.-Ampl.	-	0.5 + j 0.5	-		13
Reverse Transfer Admittance		Y_{12}	-		Cascode	-	0.0003 - j0	-	mmho	14
			-		Diff.-Ampl.	-	0.01 - j0.0002	-		15
Forward Transfer Admittance		Y_{21}	-		Cascode	-	99 - j18	-	mmho	16
			-		Diff.-Ampl.	-	-37 + j0.5	-		17
Output Admittance		Y_{22}	-		Cascode	-	0. + j0.08	-	mmho	18
			-		Diff.-Ampl.	-	0.04 + j0.23	-		19
Voltage Gain	at f = 10.7 MHz	A	22a	f = 10.7 MHz V_{CC} = +0V R_L = 1 kΩ	Cascode	-	40	-	dB	22b
			22c		Diff.-Ampl.	-	30	-		22d
Peak-to-Peak Output Current		P-P		V_{CC} = +9V	f = 10.7 MHz	2	4	7	mA	
				V_{CC} = +12V	e_{in} = 400 mV Diff.-Ampl.	3.5	6	10		

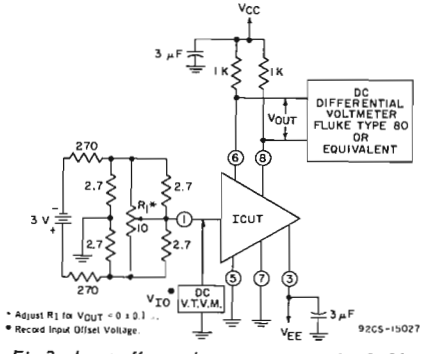


Fig.2 - Input offset voltage test circuit for CA3028B.

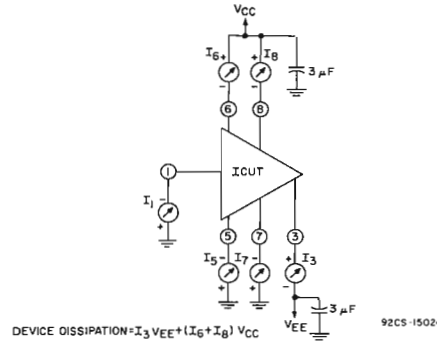


Fig.3a - Input offset current, input bias current, device dissipation, and quiescent operating current test circuit for CA3028A and CA3028B.

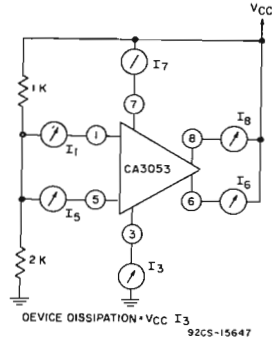


Fig.3b - Input bias current, device dissipation, and quiescent operating current test circuit for CA3053.

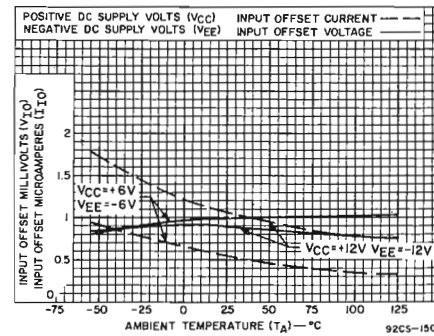


Fig.4 - Input offset voltage and input offset current for CA3028B.

TYPICAL CHARACTERISTICS

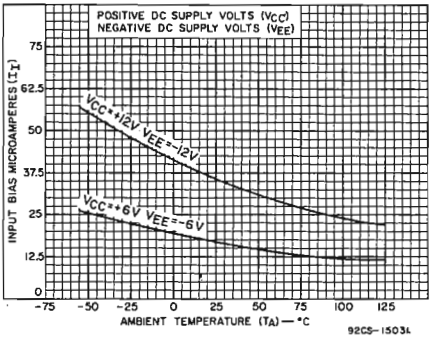


Fig.5a - Input bias current vs. ambient temperature for CA3028A and CA3028B.

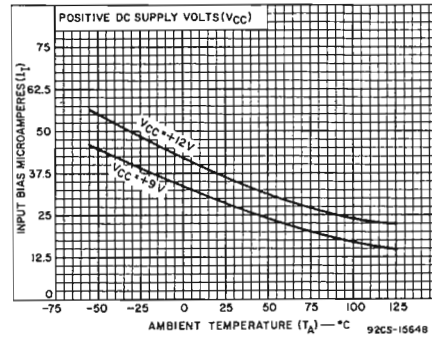


Fig.5b - Input bias current vs. ambient temperature for CA3053.

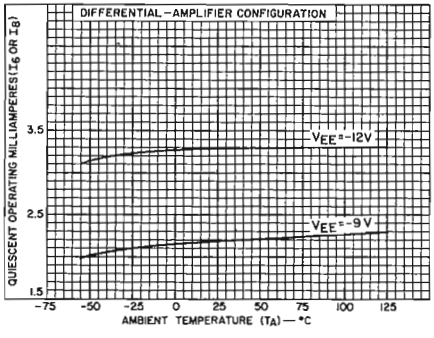


Fig.6a - Quiescent operating current vs. ambient temperature for CA3028A and CA3028B.

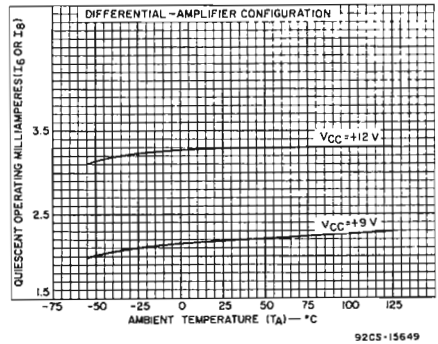


Fig.6b - Quiescent operating current vs. ambient temperature for CA3053.

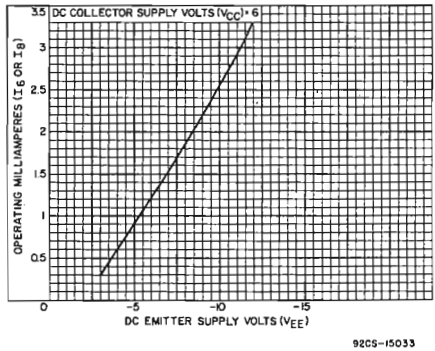


Fig.7 - Operating current vs. V_{EE} voltage for CA3028A and CA3028B.

TYPICAL CHARACTERISTICS AND TEST CIRCUITS

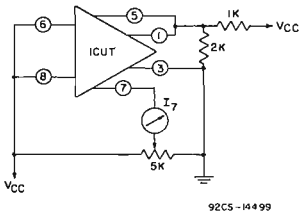


Fig.8a - AGC bias current test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

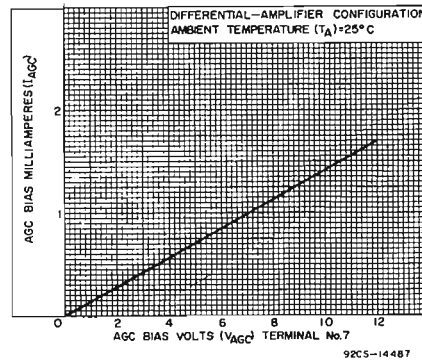


Fig.8b - AGC bias current vs. bias volts (terminal No.7) for CA3028A and CA3028B.

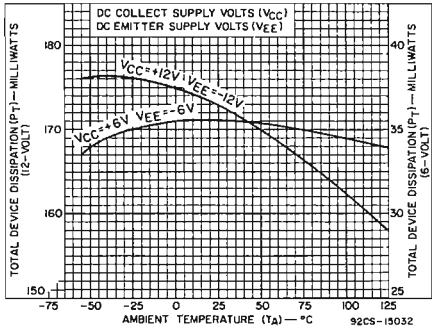
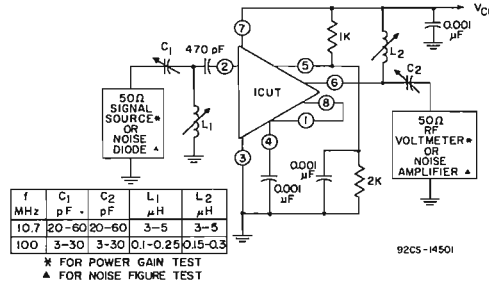


Fig.9 - Device dissipation vs. temperature for CA3028A and CA3028B.



f MHz	C1 pF	C2 pF	L1 µH	L2 µH
10.7	20-60	20-60	3-5	3-5
100	3-30	3-30	0.1-0.25	0.15-0.3

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.10a - Power gain and noise figure test circuit (cascode configuration) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Gain Test Only.

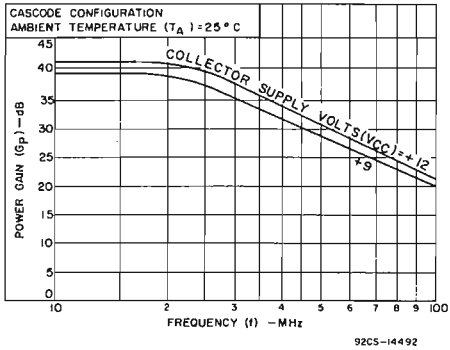


Fig.10b - Power gain vs. frequency (cascode configuration) for CA3028A and CA3028B.

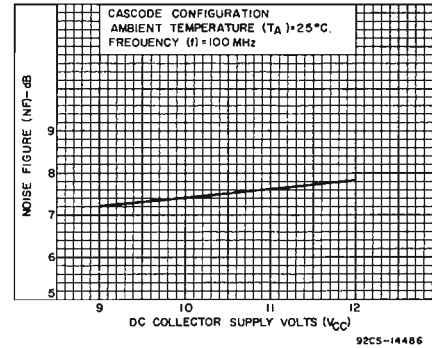
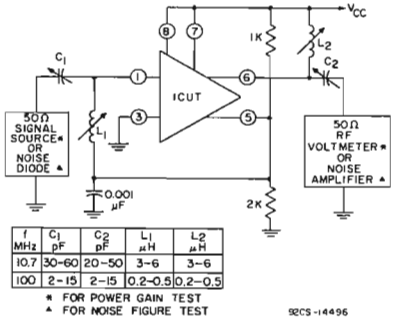


Fig.10c - 100 MHz noise figure vs. collector supply volts (cascode configuration) for CA3028A and CA3028B.

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS



f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.11a - Power gain and noise figure test circuit (differential-amplifier configuration and terminal No.7 connected to V_{CC}) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Goin Test Only.

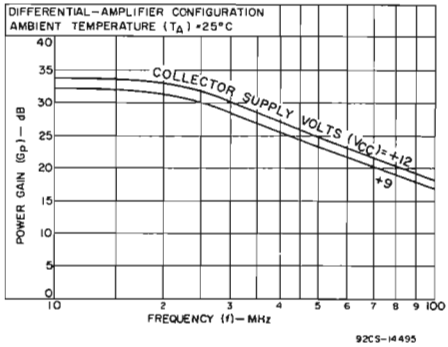


Fig.11b - Power gain vs. frequency (differential-amplifier configuration) for CA3028A and CA3028B.

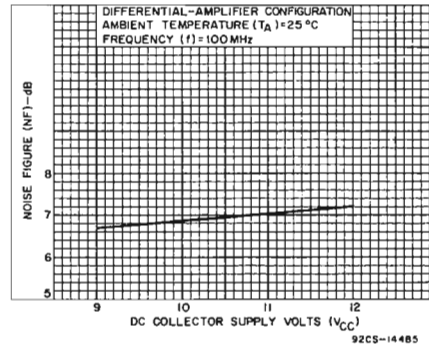
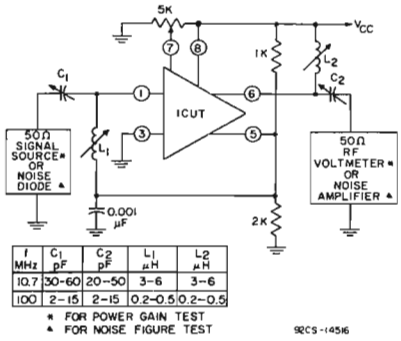


Fig.11c - 100 MHz noise figure vs. collector supply voltage (differential-amplifier configuration) for CA3028A and CA3028B.



f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.11d - Power gain and noise figure test circuit (differential-amplifier configuration for CA3028A and CA3028B.

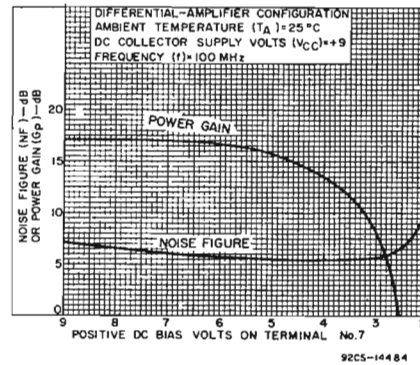


Fig.11e - 100 MHz noise figure and power gain vs. base-to-emitter bias (terminal No.7) for CA3028A and CA3028B.

TYPICAL ADMITTANCE PARAMETERS

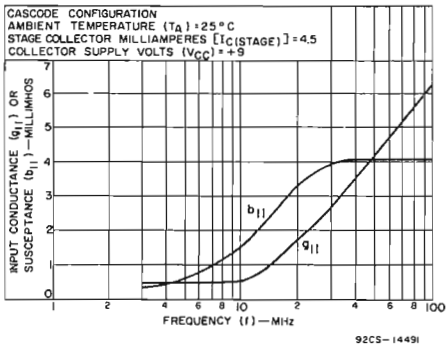


Fig.12 - Input admittance (Y_{11}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

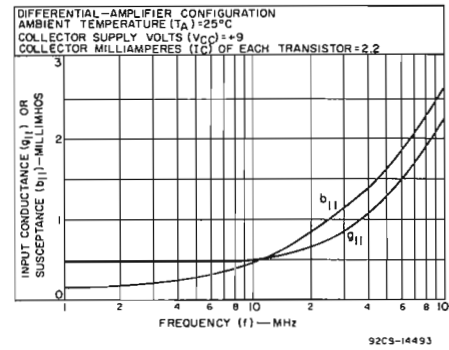


Fig.13 - Input admittance (Y_{11}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

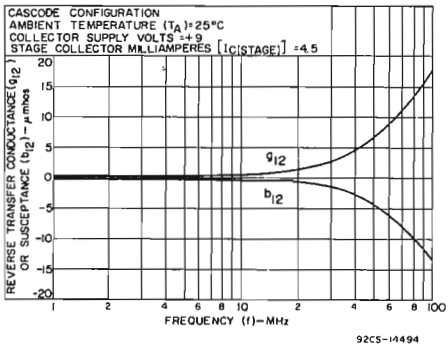


Fig.14 - Reverse transadmittance (Y_{12}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

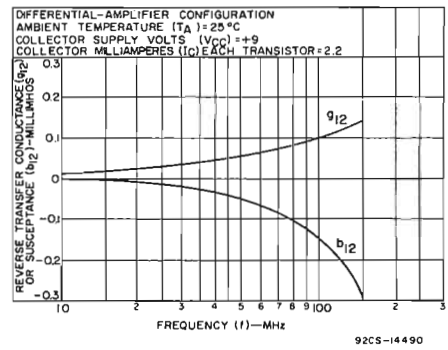


Fig.15 - Reverse transadmittance (Y_{12}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

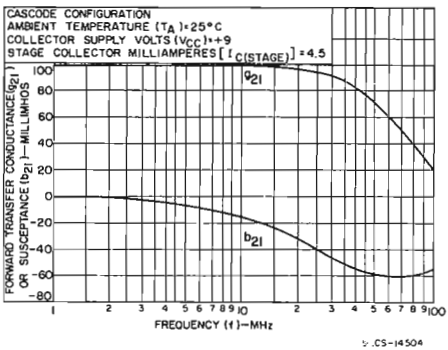


Fig.16 - Forward transadmittance (Y_{21}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

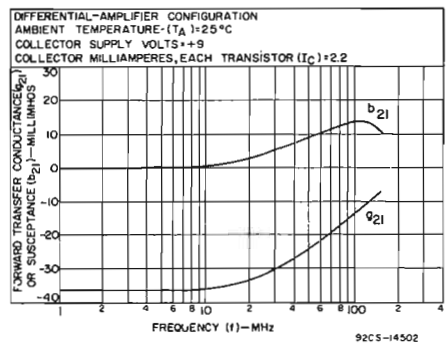


Fig.17 - Forword transadmittance (Y_{21}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TYPICAL ADMITTANCE PARAMETERS

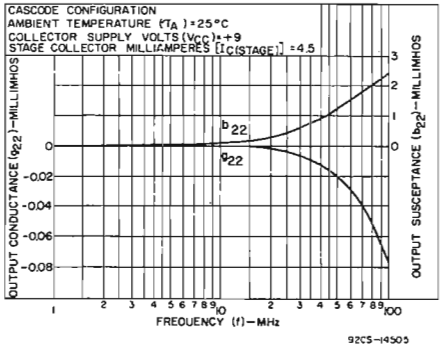


Fig.18 - Output admittance (Y_{22}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

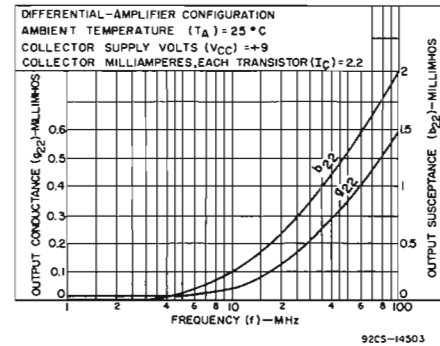


Fig.19 - Output admittance (Y_{22}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TYPICAL TEST CIRCUITS AND CHARACTERISTICS

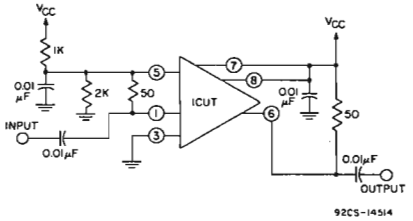


Fig.20a - Output power test circuit for CA3028A and CA3028B.

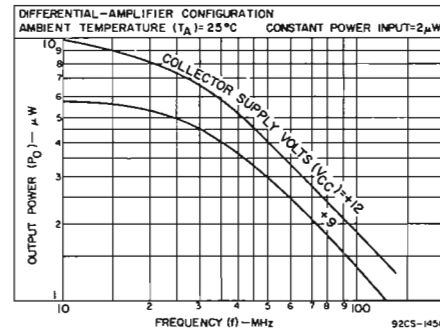
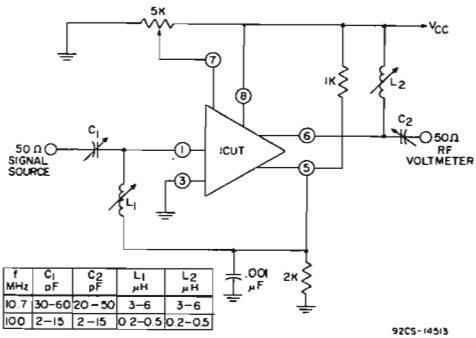


Fig.20b - Output power vs. frequency — 50Ω input and 50Ω output (differential-amplifier configuration) for CA3028A and CA3028B.



f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

Fig.21a - AGC range test circuit (differential amplifier) for CA3028A and CA3028B.

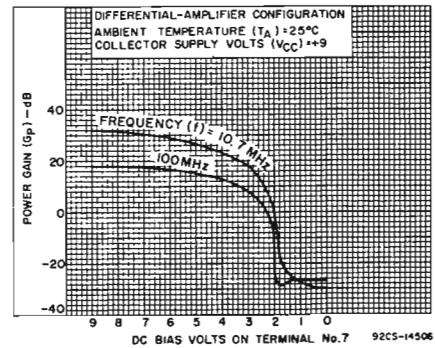


Fig.21b - AGC characteristics for CA3028A and CA3028B.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS

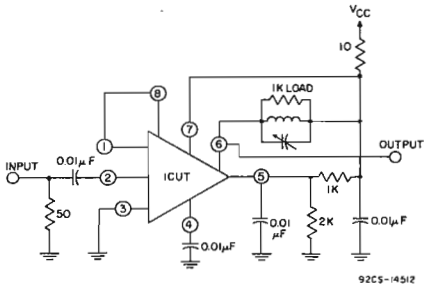


Fig.22a - Transfer characteristic (voltage gain) test circuit (10.7 MHz) cascode configuration for CA3028A, CA3028B and CA3053.

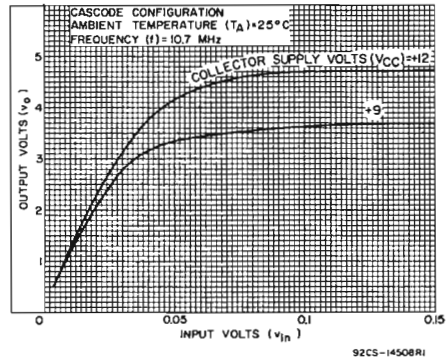


Fig.22b - Transfer characteristics (cascode configuration) for CA3028A, CA3028B and CA3053.

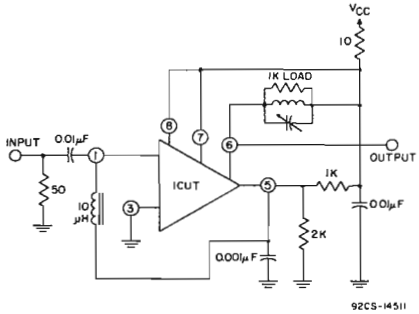


Fig.22c - Transfer characteristic (voltage gain) test circuit (10.7 MHz) differential-amplifier configuration for CA3028A, CA3028B and CA3053.

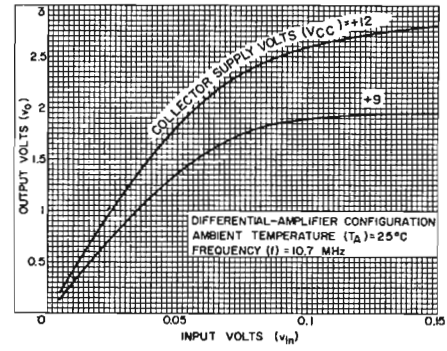
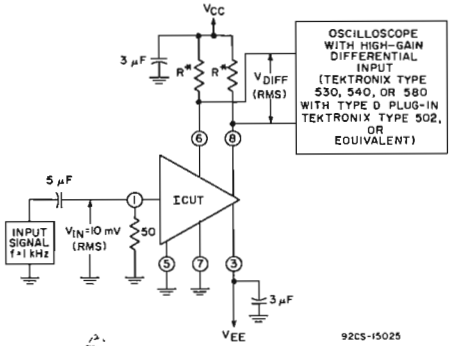
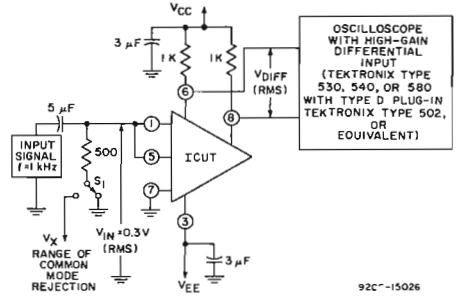


Fig.22d - Transfer characteristics (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.



* For R = 1.6 kΩ – (V_{CC} = 12V, V_{EE} = -12V)
For R = 2 kΩ – (V_{CC} = 6V, V_{EE} = -6V)

Fig.23 - Differential voltage gain, maximum peak-to-peak output voltage, and bandwidth test circuit for CA3028B.



For CMR test: S_1 to ground
For input common-mode voltage range test: S_1 to V_X

Common mode rejection ratio = $20 \log_{10} \frac{(A^*)\,(2)\,(0.3)}{V_{DIFF}\,(RMS)}$

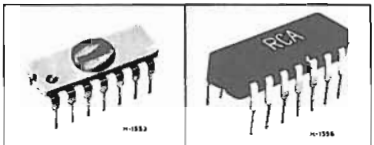
* A = Single-ended voltage gain.

Fig.24 - Common-mode rejection ratio and common-mode input-voltage range test circuit for CA3028B.

RCA
Solid State
Division

Linear Integrated Circuits

CA3033 CA3033A
CA3047 CA3047A



CERAMIC PACKAGE
CA3033, C3033A

PLASTIC PACKAGE
CA3047, CA3047A

Operational Amplifiers

For High-Output-Current Applications

APPLICATIONS

- Comparator
- Integrator
- Differentiator
- Audio Amplifier
- Summing Amplifier
- Servo Driver
- DC Amplifier
- Multivibrator
- Narrow Band and Band Pass Amplifier

FEATURES

	CA3033 CA3047 $V^+ = +12$ V $V^- = -12$ V	CA3033A CA3047A $V^+ = 15$ V $V^- = -15$ V	
Output Current	36	76	mA min.
Input Offset Current	35	25	nA max.
Open Loop Differential Gain	84	87	dB min.
Output Voltage Swing.	18	23	V_{p-p} min.
Input Bias Current	350	180	nA max.
Power Output	80	220	mW min.
Common Mode Rejection Ratio	84	93	dB min.

RCA-CA3033 is a high-performance integrated circuit operational amplifier featuring high input impedance, high gain, high power output, and low input-offset voltage and current. The device consists of two differential amplifiers in cascade and a single-ended class-B power output stage on a single monolithic silicon chip.

RCA-CA3033A has all the superior features and characteristics of the CA3033 but, in addition, can be operated at higher supply voltages to provide higher gain, higher common mode rejection, greater maximum output voltage swing, and more than double the power output.

RCA-CA3033 and CA3033A are hermetically sealed in 14-lead "dual-in-line" ceramic packages and are designed for operation over the full military temperature range of −55 °C to +125 °C.

The RCA-CA3047 and CA3047A are electrically identical to the CA3033 and CA3033A, respectively, but are limited in operating and storage temperature range.

The RCA-CA3047 and CA3047A are supplied in 14-lead, "dual-in-line" plastic packages and are designed to operate over the temperature range of 0 °C to +70 °C, ambient.

Companion Application Note, ICAN-5641 "Application of RCA CA3033 and CA3033A High Performance Integrated-Circuit Operational Amplifiers."

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

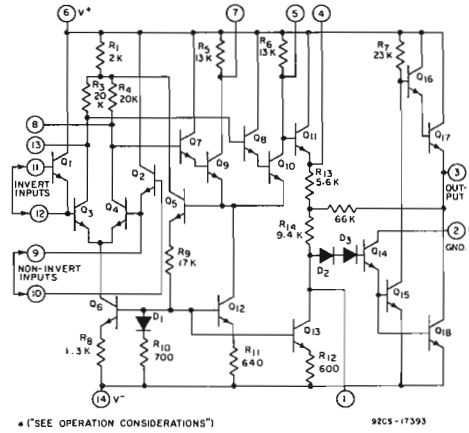


Fig. 1 - Schematic diagram of operational amplifiers, CA3033, CA3033A, CA3047, CA3047A.

ABSOLUTE-MAXIMUM RATINGS

	CA3033	CA3033A	CA3047	CA3047A
INPUT SIGNAL VOLTAGE	±10 V	−13 V, +10 V	±10 V	−13V, +10 V
DEVICE DISSIPATION:				
Up to T_C = 25 °C	1.2 W	1.2 W	750 mW	750 mW
Above T_A = 25 °C	Derate at 8 mW/°C		Derate at 6.67 mW/°C	
TEMPERATURE RANGE:				
Operating	−55 °C to +125 °C		0 °C to +70 °C	
Storage	−65 °C to +150 °C		−65 °C to +150 °C	
LEAD TEMPERATURE (During Soldering):				
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265 °C			

MAXIMUM VOLTAGE RATINGS at T_A = 25° C — CA3033, CA3047

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to the horizontal terminal 14 is 0 to +4 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1		*	*	*	*	*	*	*	*	*	*	*	*	+4 0
2			*	*	*	*	*	*	*	*	*	*	*	+26 0
3				*	*	0 −26	*	*	*	*	*	*	*	+26 0
4					+5 −1	0 −15	*	*	*	*	*	*	*	+26 0
5						0 −26	*	+20 −1 Note 1	*	*	*	*	+20 −1 Note 1	*
6							+26 0	+26 0	+26 0	+26 0	+26 0	+26 0	+26 0	+26 0
7								+20 −2 Note 1	*	*	*	*	+20 −2 Note 1	+26 0
8									+20 −1 Note 2	+20 −2 Note 3	+20 −2 Note 3	+20 −1 Note 2	*	+26 0
9										+1 −5		+5 −5	+1 −20 Note 2	+26 −5
10											+10 −10	*	+2 −20 Note 3	+26 −10
11												+1 −5	+2 −20 Note 3	+26 −10
12													+1 −20 Note 2	+26 −5
13														*
14														Sub-strate

MAXIMUM CURRENT RATINGS

CA3033 CA3047
CA3033A CA3047A

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	20	-
3	50	50
4	10	10
5	5	5
6	-	-
7	5	5
8	1	1
9	1	0.1
10	1	0.1
11	1	0.1
12	1	0.1
13	1	1
14	-	-

Notes: 1. This rating applies to the more positive terminal of terminals 8 and 13.
2. This rating applies to the more positive terminal of terminals 9 and 12.
3. This rating applies to the more positive terminal of terminals 10 and 11.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

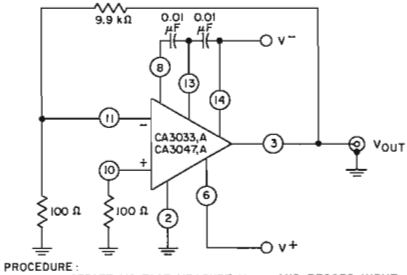
MAXIMUM VOLTAGE RATINGS at T_A = 25° C — **CA3033A, CA3047A**

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to the horizontal terminal **14** is **0** to **+4** volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1		*	*	*	*	*	*	*	*	*	*	*	*	+4 0
2			*	*	*	*	*	*	*	*	*	*	*	+38 0
3				*	*	0 −38	*	*	*	*	*	*	*	+38 0
4					+5 −1	0 −22	*	*	*	*	*	*	*	+38 0
5						0 −38	*	+30 −1 Note 1	*	*	*	*	+30 −2 Note 1	*
6							+38 0	+38 0	+38 0	+38 0	+38 0	+38 0	+38 0	+38 0
7								+30 −2 Note 1	*	*	*	*	+20 −2 Note 1	+38 0
8									+30 −1 Note 2	+30 −2 Note 3	+30 −2 Note 3	+30 −1 Note 2	*	+38 0
9										+1 −5	*	+5 −5	+1 −30 Note 2	+38 −5
10											+10 −10	*	+2 −20 Note 3	+38 −10
11												+1 −5	+2 −30 Note 3	+38 −10
12													+1 −30 Note 2	+38 −5
13														*
14														Sub- strate

MAXIMUM CURRENT RATINGS are identical for all four types (See CA3033, CA3047 chart)

Notes: See CA3033, CA3047 Rating Chart Notes.

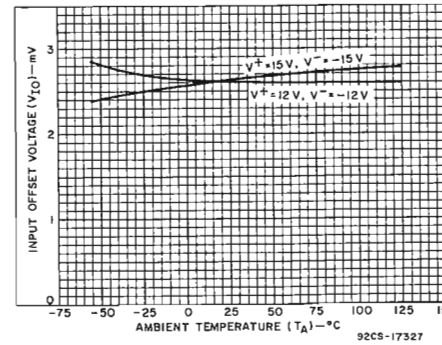


PROCEDURE:
INPUT OFFSET VOLTAGE: MEASURE V_{OUT} AND RECORD INPUT OFFSET VOLTAGE (V_{IO}) IN VOLTS AS $V_{OUT}/100$, THUS

$$V_{IO}\ (\text{IN VOLTS}) = \frac{V_{OUT}}{100}$$

92CS-17328

Fig. 2a - Input offset voltage, input offset voltage sensitivity, and device dissipation test circuit.



92CS-17327

Fig. 2b - Typical input offset voltage vs. ambient temperature.

ELECTRICAL CHARACTERISTICS
For Equipment Design

Characteristics	Symbols	Test Conditions			Typical Characteristics Curves	LIMITS						Units
						CA3033, CA3047			CA3033A, CA3047A			
		Circuit	T_A = 25° C			DC Supply Voltage V^+ = 12 V, V^- = −12 V			DC Supply Voltage V^+ = 15 V, V^- = −15 V			
		Fig.			Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	2a			2b	–	2.6	5	–	2.9	5	mV
Input Offset Current	I_{IO}	3a			3b	–	5	35	–	9	25	nA
Input Bias Current	I_I	3a			3c	–	70	350	–	100	180	nA
Input Offset Voltage Sensitivity:												
Positive	$\Delta V_{IO}/\Delta V^+$	2a			–	–	0.3	0.5	–	0.2	0.5	mV/V
Negative	$\Delta V_{IO}/\Delta V^-$	2a			–	–	0.3	0.5	–	0.2	0.5	mV/V
Device Dissipation	P_T	2a			–	60	120	180	80	170	300	mW
Open-Loop Differential Voltage Gain	A_{OL}	–	f = 1 kHz		4	84	90	–	87	93	–	dB
Common-Mode Rejection Ratio	CMRR	–			5	84	100	–	93	105	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–			–	−7.5	+5,−9	+3.5	−9.7	6,−11	4.7	V
Maximum Output-Voltage Swing	V_O(P-P)	–	f = 1 kHz	R_L = 500 Ω	–	18	22	–	–	–	–	V_{P-P}
				R_L = 300 Ω		–	–	–	23	25	–	
Input Impedance	Z_I	–			–	0.25	1.5	–	0.6	1	–	MΩ
Output Current	I_O	–		R_L = 500 Ω	6	35	44	–	–	–	–	mA-(P-P)
				R_L = 300 Ω		–	–	–	76	83	–	
Power Output THD <5%	P_o	–		R_L = 500 Ω	7	80	122	–	–	–	–	mW
				R_L = 300 Ω		–	–	–	220	255	–	

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

Input Offset Voltage Drift −55° C to 125° C	$V_{IO}/\Delta T$	2a			2b	–	6.6	–	–	6.6	–	μV/°C
Input Offset Current Drift												
−55° C to 25° C	$I_{IO}/\Delta T$	3a			3b	–	1	–	–	1	–	nA/°C
25° C to 125° C						–	0.08	–	–	0.08	–	
60-dB Amplifier Bandwidth	BW	8a	C_x, C_y = 0.001 μF		8b,c	–	230	–	–	350	–	kHz
Slew Rate	SR	9	(amplifier circuit only)		–	–	2.7	–	–	3	–	V/μs

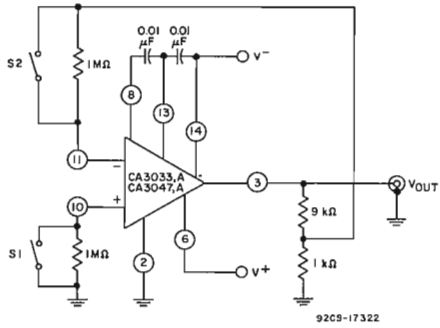


Fig. 3a - Input offset current and input bias current test circuit.

PROCEDURES:

A. Inverting Input Current

Set switch, S_1 in closed position and set switch, S_2 in open position.

Measure output voltage and convert this reading to inverting input current using the following relation:

$$I_I \text{ inverting (in } \mu A) = \frac{V_{OUT} \text{ (in volts)}}{10}$$

B. Non-inverting Input Current

Set switch, S_1 in open position and set switch, S_2 in closed position.

Measure output voltage and convert this reading to non-inverting input current using the following relation:

$$I_I \text{ non-inverting (in } \mu A) = \frac{-V_{OUT} \text{ (in volts)}}{10}$$

C. Input Offset Current

Set switches, S_1 and S_2 in open positions.

Measure output voltage and convert this reading to input offset current using the following relation:

$$I_{IO} \text{ (in } \mu A) = \frac{V_{OUT} \text{ (in volts)}}{10}$$

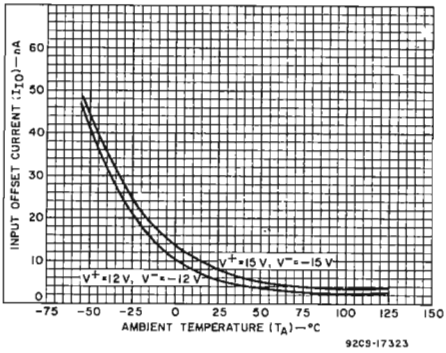


Fig. 3b - Typical input offset current vs. ambient temperature.

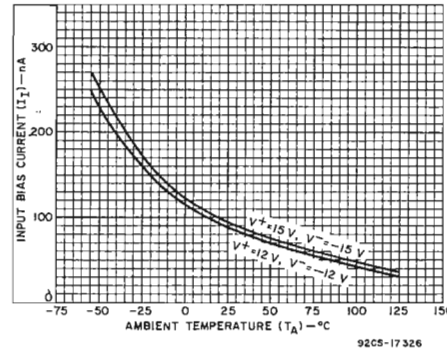


Fig. 3c - Typical input bias current vs. ambient temperature.

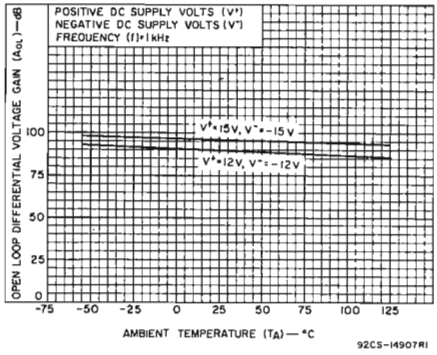


Fig. 4 - Typical open-loop differential voltage gain vs. ambient temperature.

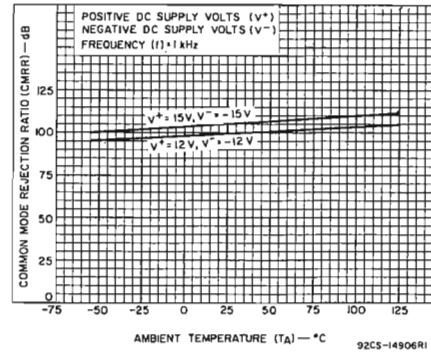


Fig. 5 - Typical common mode rejection ratio vs. ambient temperature.

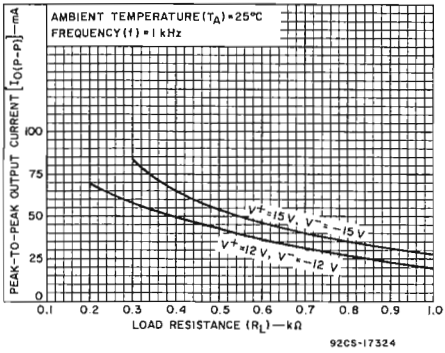


Fig. 6 - Typical peak-to-peak output current vs. load resistance.

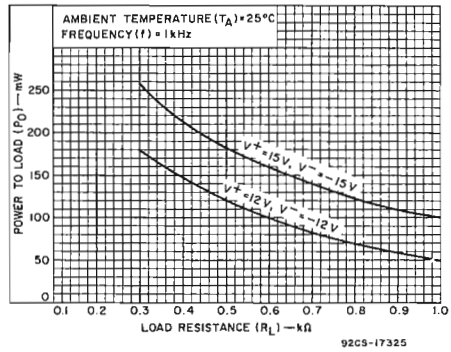


Fig. 7 - Typical power output vs. load resistance.

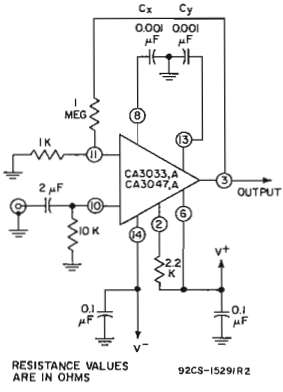


Fig. 8a - Typical 60-dB amplifier.

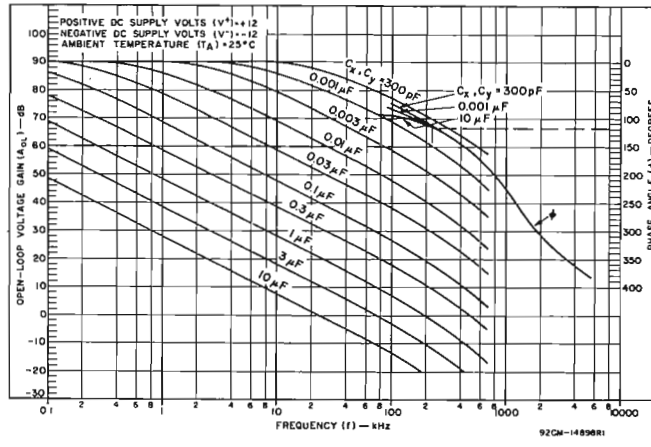


Fig. 8b - Typical phase compensation characteristics for CA3033, CA3047 (V^+ = +12 V, V^- = −12 V)

For any desired closed loop gain (in decibels), read horizontally along the gain line to the attenuation curve which provides the desired closed loop bandwidth. The required values for the compensation capacitors is shown on the curve. Move vertically from the intersection of the gain and attenuation lines until the phase angle curve (ϕ) is reached and read the phase angle between the input and output on the right-hand scale. The difference between the indicated phase angle and 180° is the typical phase margin. (A minimum phase margin of 45° is recommended to allow for component variations and differences among amplifiers.) If the phase margin is smaller than required, the desired bandwidth can be stably achieved through the use of a more complex feedback network. As the closed loop gain approaches unity, the compensating capacitors required (0.3 μF to 1.0 μF) are bulky and costly. A capacitor one-half the value shown on the chart, connected between terminals 8 and 13, and a 0.001 μF capacitor from either terminals 8 or 13 to ground or V^- is an acceptable alternative method. This arrangement provides the same gain-phase roll-off shown on the curves and permits the use of more readily available, lower-voltage disc capacitors which are smaller and cost less. For linear operation, the maximum expected difference voltage between the two collectors is less than 1 volt.

Figure 8a shows the phase compensating capacitors (C_X, C_Y) returned to ground. In some systems with large parasitic impedances in the power supply system, returning these capacitors to the negative (V^-) supply may result in more stable operation.

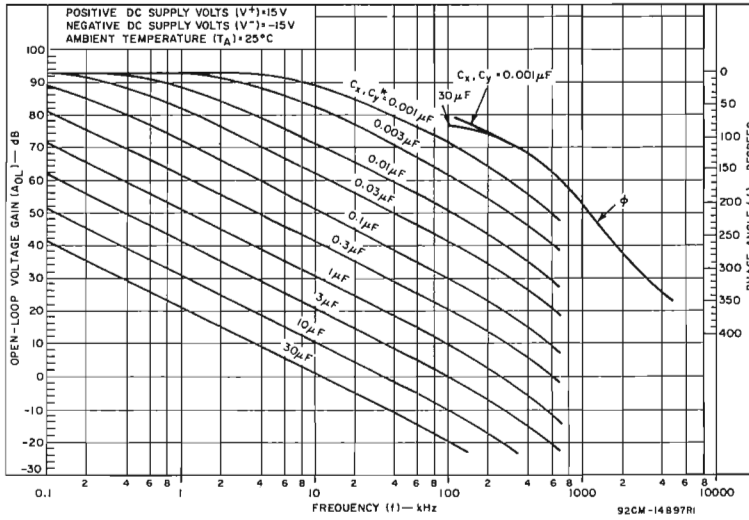


Fig. 8c - Typical phase compensation characteristics for CA3033A, CA3047A (V^+ = 15 V, V^- = −15 V).

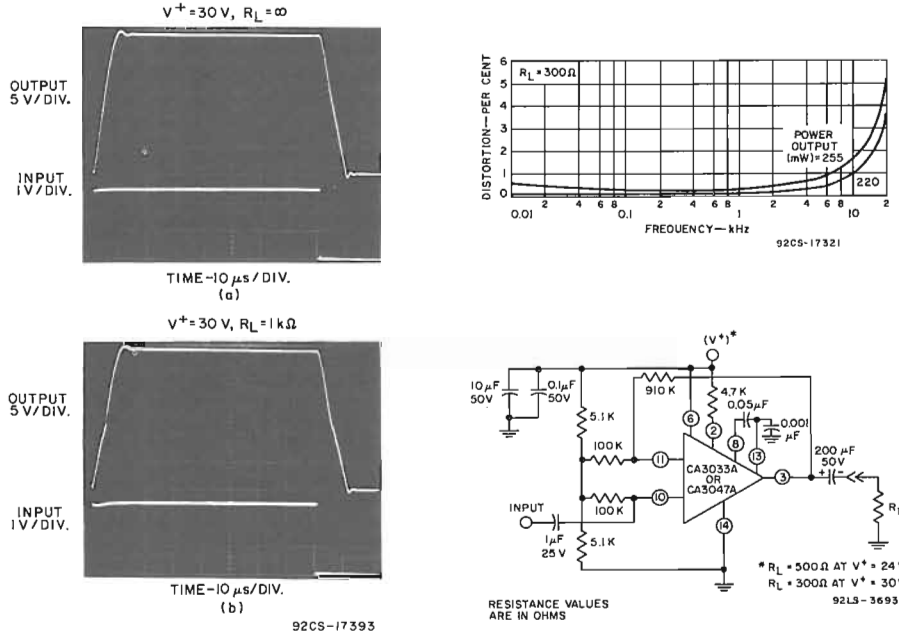


Fig. 9 - Amplifier with single voltage supply and associated pulse response waveforms and distortion curves.

OPERATING CONSIDERATIONS

The CA3033, CA3033A, CA3047, and CA3047A operational amplifiers have very high peak-pulse current capability. The open-loop output impedance is typically less than 30 ohms at 10 kHz and the peak short-circuit output current may exceed 100 milliamperes. To prevent possible damage to the chip because of excessive dissipation it is important that the output stage is not subjected to sustained high peak currents. To minimize the possibility of damage from accidental shorts, it is recommended that a 51-ohm resistor be placed in series with the output circuit.

When high peak output currents are required of the amplifier, it is desirable to provide a current-limiting resistor of about 2200 ohms in series with the collector of transistor Q_{14}. This resistor may be returned to ground, or, if its value is increased to 4700 ohms; it may be returned to the V^+ terminal.

RCA
Solid State
Division

Linear Integrated Circuits

CA3035
CA3035V1

Ultra-High-Gain
Wide-Band Amplifier Array

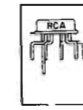
Monolithic Silicon

- Three Individual General-Purpose Amplifiers
- Ideal for service in Remote-Control Amplifiers — — e.g., TV Receivers
- Available in two electrically identical versions: CA3035 with straight leads; CA3035V1 with formed leads

CA3035

10-LEAD TO-5

CA3035V1



FORMED-LEAD 10-LEAD TO-5

HIGHLIGHTS

- Three separate amplifiers — gain and bandwidth for each amplifier can be adjusted with suitable external circuitry
- Amplifiers operable independently or in cascade
- Exceptionally high cascade voltage gain — 129 dB typ. at 40 kHz
- Low noise performance
- Wide-band response
- All amplifiers single-ended — only one power supply required
- Wide operating temperature range — -55°C to +125°C
- Built-in temperature compensation
- Hermetically sealed, all-welded 10-lead TO-5-style metal package with straight or formed leads

SCHEMATIC DIAGRAM FOR CA3035 AND CA3035V1

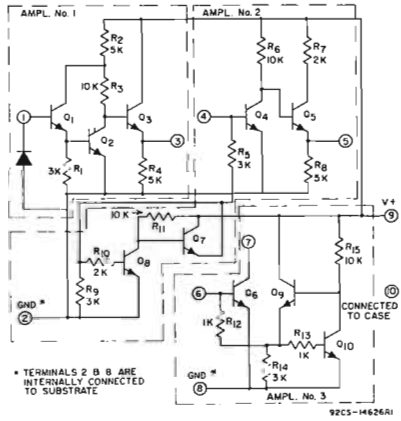


Fig. 1

TYPICAL REMOTE CONTROL SYSTEM

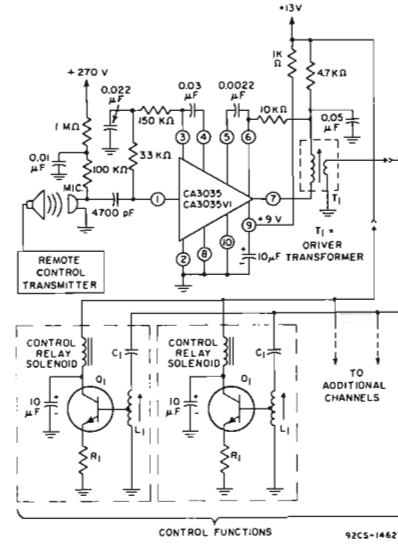


Fig. 2

ABSOLUTE-MAXIMUM RATINGS:

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Device Dissipation ..... 300 mW
Input Voltage ..... 1 V p-p
Supply Voltage ..... +15V
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUITS AND CHARAC-TERISTICS CURVES	LIMITS CA3035, CA3035V1 Min.	Typ.	Max.	UNITS
STATIC CHARACTERISTICS							
Quiescent Operating Voltage	V3 V5 V7	V_{CC} = +9V	Fig.3	– – –	2 1.9 4.9	– – –	V V V
Total Current Drain	I_d	V_{CC} = +9V, R_{L3} = 5KΩ	Fig.3	3.5	5	7.5	mA
DYNAMIC CHARACTERISTICS							
Voltage Gain: Amplifier No.1 Amplifier No.2 Amplifier No.3	 A_1 A_2 A_3	 f = 40 kHz, V_{CC} = +9V		 40 40 38	 44 46 42	 – – –	 dB dB dB
Output Voltage Swing	V_{out} V_{1out} V_{2out} V_{3out}	 R_{L1} = 10KΩ R_{L2} = 10KΩ R_{L3} = 5KΩ Sinusoidal Output, V_{CC} = +9V		 – – –	 2 2.6 8	 – – –	 Vp-p Vp-p Vp-p
Input Resistance: Amplifier No.1 Amplifier No.2 Amplifier No.3	 R_{1in} R_{2in} R_{3in}	 f = 40 kHz		 – – –	 50K 2K 670	 – – –	 Ω Ω Ω
Output Resistance	R_{1out} R_{2out} R_{3out}	f = 40 kHz		– – –	270 170 100K	– – –	Ω Ω Ω
Bandwidth at -3dB point: Amplifier No.1 Amplifier No.2 Amplifier No.3	 BW_1 BW_2 BW_3	 V_{CC} = +9V	 Fig.5 Fig.6 Fig.7	 – – –	 500 2.5 2.5	 – – –	 kHz MHz MHz
Noise Figure Amplifier No.1	 NF_1	 f = 1 kHz, R_S = 1 KΩ	 Fig.4	 –	 6	 7	 dB
Sensitivity		V_{CC} = +13V, Relay (K_1) Current = 7.5 mA	Fig.2	–	100	150	μ

STATIC CHARACTERISTICS

TEST CIRCUIT

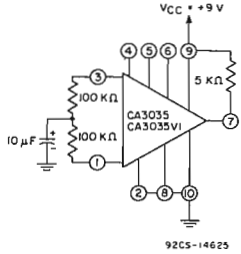
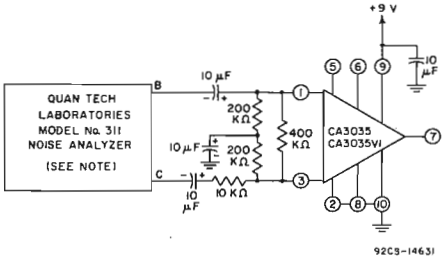


Fig.3

NOISE FIGURE TEST CIRCUIT



NOTE: SET ALL INTERNAL POWER SUPPLIES ON QUAN TECH NOISE ANALYZER TO ZERO VOLTS.

Fig.4

TYPICAL 1st-AMPLIFIER RESPONSE

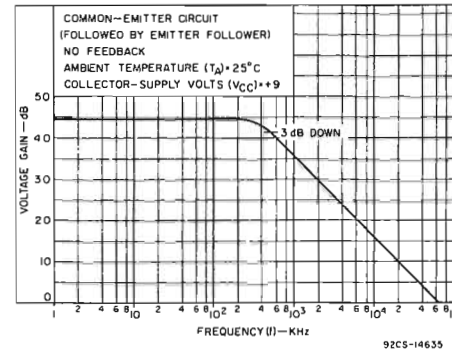


Fig.5

TYPICAL 2nd-AMPLIFIER RESPONSE

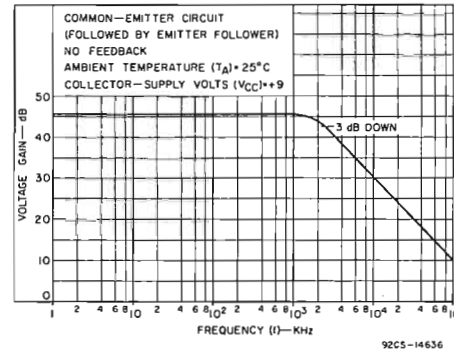


Fig.6

TYPICAL 3rd-AMPLIFIER RESPONSE

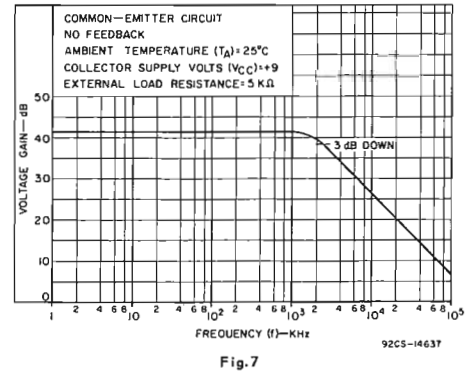


Fig.7

RCA
Solid State
Division

Linear Integrated Circuits

CA3036

DUAL DARLINGTON ARRAY

Monolithic Silicon

- Two independent low-noise wide-band amplifier channels
- Particularly useful for preamplifier and low-level amplifier applications in single-channel and stereo systems
- Wide application in low-noise industrial instrumentation amplifiers

10-Lead TO-5

HIGHLIGHTS

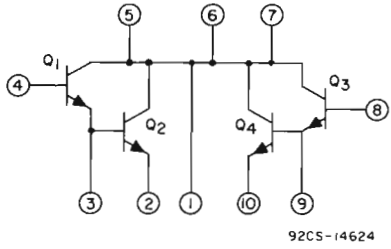
- Matched transistors with emitter-follower outputs
- Low-noise performance
- 200-MHz gain-bandwidth product
- Operation from -55°C to +125°C
- Hermetically sealed, all-welded 10-lead TO-5-style metal package

APPLICATIONS

- Stereo phonograph preamplifiers
- Low-level stereo and single channel ⑧ amplifier stages
- Low-noise, emitter-follower differential amplifiers
- Operational amplifier drivers

MAXIMUM RATINGS, Absolute-Maximum Values:

POWER DISSIPATION, P:		
Any one transistor	300 max.	mW
Total for array	600 max.	mW
TEMPERATURE RANGE:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C
The following ratings apply for each transistor in the array:		
Collector-to-Emitter Voltage, V_{CEO}	15 max.	V
Collector-to-Base Voltage, V_{CBO}	30 max.	V
Emitter-to-Base Voltage, V_{EBO}	5 max.	V
Collector Current, I_C	50 max.	mA



92CS-14624

Fig.1 — Schematic Diagram for CA3036.

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$

CHARACTERISTICS		SYMBOLS	TEST CONDITIONS	LIMITS TYPE CA3036 Min.	Typ.	Max.	UNITS
For Each Transistor (Q_1, Q_2, Q_3, Q_4)	Collector-Cutoff Current	I_{CBO}	V_{CB} = 5V, I_E = 0	–	–	0.5	μA
	Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	--	--	5	μA
	Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	20	--	V
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	30	44	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	6	--	V
For Either Input Transistor (Q_1 or Q_3)	Static Forward Current-Transfer Ratio	h_{FE}	I_{C1} or I_{C3} = 1 mA	30	82	--	--
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Emitter-to-Base Breadkown Voltage	$V_{(BR)EBO(D)}$	I_{E2} or I_{E4} = 10 μA	10	12.6	--	V
	Static Forward Current-Transfer Ratio	$h_{FE(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	1000	4540	–	–
For Each Input Transistor (Q_1 or Q_3)	Short-Circuit Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, I_{C1} or I_{C3} = 1 mA	--	82	–	--
	Short-Circuit Input Impedance	h_{ie}		--	2.6K	–	Ω
	Open-Circuit Output Admittance	h_{oe}		--	7	–	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	9.8 x 10^{-5}	–	–
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Short-Circuit Forward Current-Transfer Ratio	$h_{fe(D)}$	f = 1 kHz, $I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	–	1300	--	--
	Short-Circuit Input Impedance	$h_{ie(D)}$		--	82K	--	Ω
	Open-Circuit Output Admittance	$h_{oe(D)}$		--	108	--	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	$h_{re(D)}$		–	2.7 x 10^{-3}	--	--
	Voltage Gain	$A_{(D)}$		--	26	–	dB
	Power Gain	$G_{p(D)}$		--	47	--	dB
	Noise Voltage See Fig.3 for Test Circuit	E_N	f = 100 Hz	--	0.2	3	$\mu V(rms)/\sqrt{f(Hz)}$
			f = 1 kHz	--	0.05	0.3	
			f = 10 kHz	--	0.012	0.1	
For Either Input Transistor (Q_1 or Q_3)	Forward Transfer Admittance	y_{fe}	f = 50 MHz, I_{C1} or I_{C3} = 2 mA	--	0.68 + j 7.9	--	mmho
	Input Admittance (Output Short-Circuited)	y_{ie}		–	4.14 + j 5.95	–	mmho
	Output Admittance (Input Short-Circuited)	y_{oe}		--	1.94 + j 2.64	–	mmho
	Reverse Transfer Admittance (Input Short-Circuited)	y_{re}		--	Negligible	--	mmho
For either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Input Admittance (Output Short-Circuited)	$y_{ie(D)}$	f = 50 MHz, $I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 2 mA	--	1.71 + j 2.8	–	mmho
	Output Admittance (Input Short-Circuited)	$y_{oe(D)}$		–	3.96 + j 2.6	--	mmho
	Gain-Bandwidth Product	$f_T(D)$		150	200	--	MHz

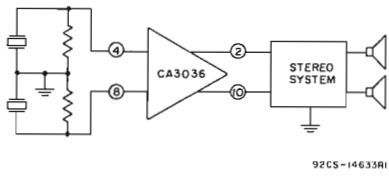


Fig.2 - Block Diagram of Stereo System using CA3036 as Phono Preamplifier.

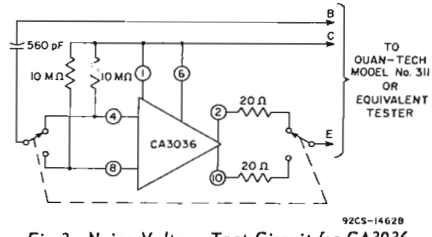


Fig.3 - Noise Voltage Test Circuit for CA3036.

RCA
Solid State
Division

Linear Integrated Circuits

CA3039

Diode Array

Six Matched Diodes on a Common Substrate
Monolithic Silicon

The RCA-CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

ULTRA-FAST LOW-CAPACITANCE MATCHED DIODES

For Applications in Communications and Switching Systems

12-Lead TO-5

APPLICATIONS

- Balanced modulators or demodulators
- Ring modulators
- High speed diode gates
- Analog switches

FEATURES

- Excellent reverse recovery time – 1 ns typ.
- Matched monolithic construction – V_F matched within 5 mV
- Low diode capacitance – C_D = 0.65 pF typical at V_R = –2 V

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

DISSIPATION:

Any one diode unit	100 mW
Total for device	600 mW
For T_A > 55°C	derate linearly 5.7 mW/°C

TEMPERATURE RANGE:

Operating	–55 to +125°C
Storage	–65 to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+ 265°C
PEAK INVERSE VOLTAGE, PIV for: D_1–D_5	5 V
D_6	0.5 V
PEAK DIODE-TO-SUBSTRATE VOLTAGE, V_{DI} for D_1–D_5 (term. 1,4,5,8 or 12 to term. 10)	+ 20, –1 V
DC FORWARD CURRENT, I_F	25 mA
PEAK RECURRENT FORWARD CURRENT, I_f	100 mA
PEAK FORWARD SURGE CURRENT, $I_{f(surge)}$	100 mA

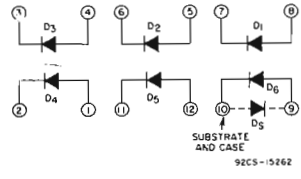


Fig. 1 - Schematic Diagram for CA3039

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES
			MIN.	TYP.	MAX.		FIG.
DC Forward Voltage Drop	V_F	I_F = 50 μA	–	0.65	0.69	V	2
		1 mA	–	0.73	0.78	V	
		3 mA	–	0.76	0.80	V	
		10 mA	–	0.81	0.90	V	
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = −10 μA	5	7	–	V	–
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = −10 μA	20	–	–	V	–
DC Reverse (Leakage) Current	I_R	V_R = −4 V	–	0.016	100	nA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = −10 V	–	0.022	100	nA	4
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	–	0.5	5	mV	2
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA	–	1	–	μV/°C	5
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	–	−1.9	–	mV/°C	6
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA	–	0.65	–	V	–
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	–	1	–	ns	–
Diode Resistance	R_D	f = 1 kHz, I_F = 1 mA	25	30	45	Ω	7
Diode Capacitance	C_D	V_R = −2 V, I_F = 0	–	0.65	–	pF	8
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF	9

TYPICAL CHARACTERISTICS

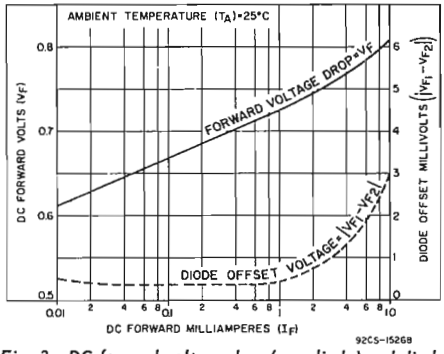


Fig. 2 - DC forward voltage drop (any diode) and diode offset voltage vs DC forward current

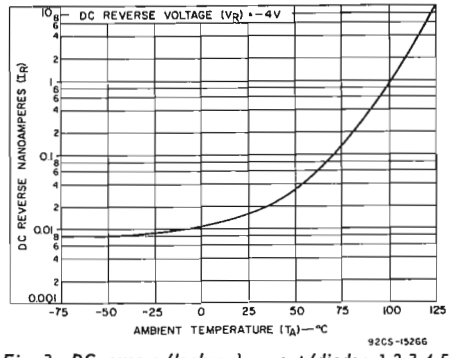


Fig. 3 - DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature

TYPICAL CHARACTERISTICS

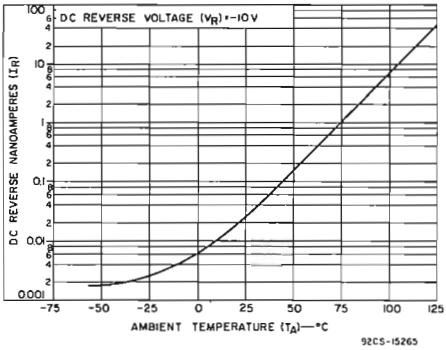


Fig. 4 - DC reverse (leakage) current between diodes (1,2,3,4,5) and substrate vs temperature

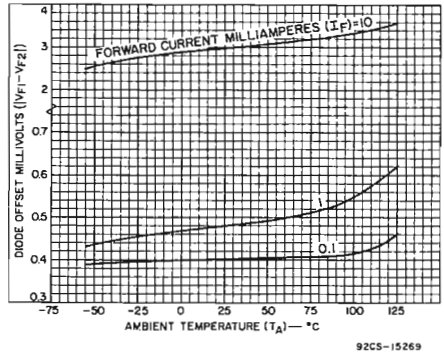


Fig. 5 - Diode offset voltage (any diode) vs temperature

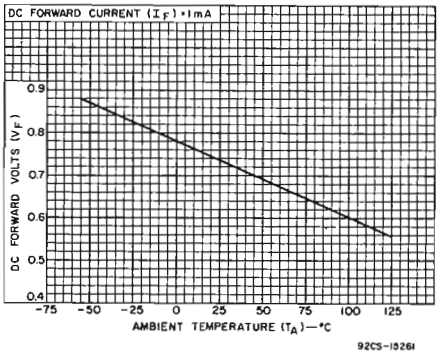


Fig. 6 - DC forward voltage drop (any diode) vs temperature

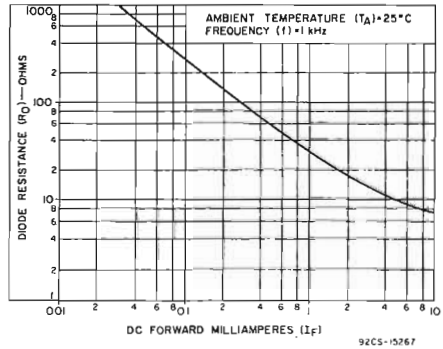


Fig. 7 - Diode resistance (any diode) vs DC forward current

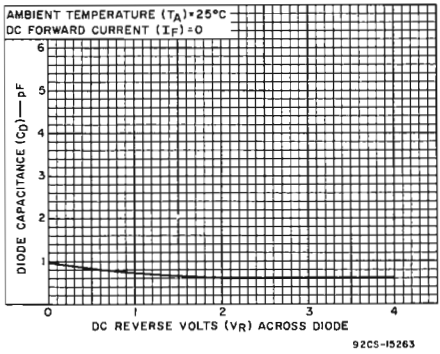


Fig. 8 - Diode capacitance (diodes 1,2,3,4,5) vs reverse voltage

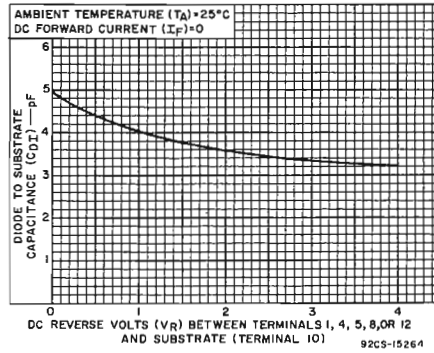


Fig. 9 - Diode-to-substrate capacitance vs reverse voltage

RCA
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CA3040

VIDEO and WIDE-BAND AMPLIFIER

For Industrial and Commercial Equipment at Frequencies up to 200 MHz

12-Lead TO-5

The RCA CA3040 is a monolithic silicon integrated circuit designed to meet the requirements of a wide variety of applications requiring high gain and wide bandwidth. The cascode-connected differential amplifier achieves a double-ended gain of 37 dB with a typical 3 dB bandwidth of 55 MHz. Emitter-Follower input and output stages provide the desirable high input impedance and low output impedance for coupling to other circuits.

The CA3040 includes two biasing options, allowing the user to optimize his design over the entire military temperature range of -55 to +125°C. **Bias Mode A** yields a substantially constant voltage at the output terminals for applications using DC coupling to succeeding stages or requiring maximum dynamic range over the temperature range. DC output voltage varies less than 0.1 volt (typically) over the entire temperature range while gain varies ±2 dB. **Bias Mode B** provides extremely stable gain over the temperature range. Gain variation is 0 dB (typically) in this Bias Mode. DC variation is ±0.8 volt.

Provisions are also made for stabilizing the operating point for either single or split power supplies.

FEATURES

- High Differential Push-Pull Voltage Gain ..... 37 dB typ.
  Single-Ended Voltage Gain..... 31 dB typ.
- Wide (3dB) Bandwidth..... 55 MHz typ.
- Balanced Input and Output
- High Input Resistance ..... 150 kΩ typ.
- Low Output Resistance..... 125 Ω typ.
- Bias Options for Temperature Compensation:
  Bias Mode A: "Constant" Voltage
  Bias Mode B: "Constant" Gain

APPLICATIONS

- Video Amplifier
- Modulator
- Mixer
- Schmitt Trigger
- IF Amplifier
- DC Amplifier
- Sense Amplifier

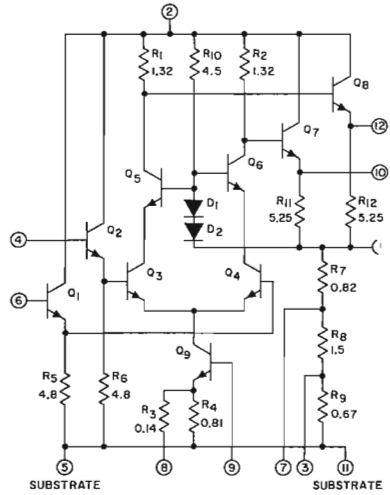


Fig.1 - Schematic Diagram for CA3040

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION * . . . . . 450 mW
Derating factor for T_A 85°C . . . . . 5 mW/°C
TEMPERATURE RANGE:
Operating . . . . . -55°C to +125°C
Storage . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

* Limitation imposed by the thermal resistance of package.

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 2 with respect to terminal 11 is 0 to +14 volts.

TERMINAL No.	1	2	3	4	5▲	6	7	8	9	10	11▲	12
1		0 -14	*	*	+14 0	*	+10 -10	*	*	*	+14 0	*
2			*	+14 0	+14 0	+14 0	*	*	*	+14 0	+14 0	+14 0
3				*	+5 -3	*	*	*	*	*	+5 -3	*
4					*	+3 -3	*	*	*	*	*	*
5▲					▲	*	+10 -3	*	+3 -7	*	0 - Note 1	*
6							*	*	*	*	*	*
7								*	*	*	+10 -3	*
8									+3 -3	*	*	*
9										*	+7 -3	*
10											*	*
11▲											▲	*
12												

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	-	-
3	5	5
4	1	0.1
5	-	-
6	1	0.1
7	5	5
8	5	5
9	1	0.1
10	-	10
11	-	-
12	-	10

▲ Reference Substrate

Note 1: External connection required for proper operation.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C Unless Otherwise Specified

Characteristics	Symbols	Test Circuits Fig.	Special Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
STATIC CHARACTERISTICS	V_{CC} = +6V, V_{EE} = −6V						
Output Voltage	V_{10} or V_{12}	2(a) 2(b)	Bias Mode Switch A or B: Closed	1.4	2.7	3.7	V
Base Bias Voltage	V_9	2(a)	Bias Mode A Switch Closed	−	-1.7	−	V
		2(b)	Bias Mode B Switch Closed	−	-1.7	−	V
Input Bias Reference Voltage	V_1	2(a) 2(b)	Bias Mode Switch A or B: Open	-1	−	+1	V
Input Bias Current	I_4, I_6	2(a) 2(b)	Bias Mode Switch A or B: Closed	−	15	45	μA
Input Unbalance Current	$\lvert I_6 - I_4 \rvert$	2(a) 2(b)	Bias Mode Switch A or B: Closed	−	−	6	μA
Power Supply Current Drain	I_2 or $I_5 + I_{11}$	2(a)	Mode A Switch open or closed	4.7	8.5	15.5	mA
	I_2 or $I_5 + I_8 + I_{11}$	2(b)	Mode B Switch open or closed				
DYNAMIC CHARACTERISTICS	V_{CC} = +12V, V_{EE} = 0, Split Voltage Supply (Optional) = +6V						
Differential Voltage Gain							
Single-Ended Input Differential Output	$A_{DIFF(DE)}$	3(a)	f = 1 MHz R_S = 50 Ω	34	37	−	dB
Single-Ended Input and Output	$A_{DIFF(SE)}$	3(a)	f = 1 MHz R_S = 50 Ω	28	31	−	dB
-3dB Bandwidth	BW	3(a)	R_S = 50 Ω	40	55	−	MHz
Differential Voltage Gain Balance	$A_{DIFF(SE)10} - A_{DIFF(SE)12}$	3(a)	f = 1 MHz	-1	0	+1	dB
Output Voltage Swing	V_8 or V_{10} RMS	3(a)	f = 1 MHz R_S = 50 Ω	−	0.5	−	V_{RMS}
Noise Figure	NF	3(a)	(Note 1) f = 30 MHz R_S = 400 Ω	−	7.5	9	dB
Parallel Input Resistance	R_I	3(a)	f = 1 MHz	−	150	−	kΩ
Parallel Input Capacitance	C_I	3(a)		−	2.2	−	pF
Output Resistance	R_O	3(a)		−	125	−	Ω
TEMPERATURE DEPENDENT CHARACTERISTICS Temperature coefficients for ambient temperature: −55°C ≤ T_A ≤ + 125°C							
Output Voltage	$\frac{\Delta V_{10} \text{ or } \Delta V_{12}}{^\circ C}$	3(a)	Bias Mode A	−	0	−	mV/°C
		3(b)	Bias Mode B	−	6.4	−	mV/°C
Power Supply Current Drain	$\Delta I_2/^\circ C$	3(a)	Bias Mode A	−	5	−	μA/°C
Differential Voltage Gain	$A_{DIFF}/^\circ C$	3(a)	Bias Mode A	−	0.0166	−	dB/°C
		3(b)	Bias Mode B	−	0	−	

Note 1: Replace 1-kΩ resistors between Term. 1 and 4 and Term. 1 and 6 with suitable chokes so that reactance at 30 MHz exceeds 5kΩ

STATIC CHARACTERISTICS TEST CIRCUITS FOR CA3040

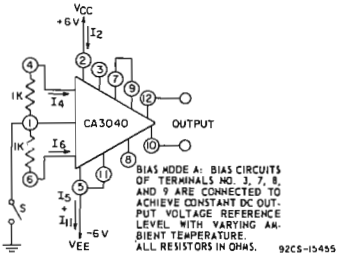


Fig.2(a) - Bias Mode A

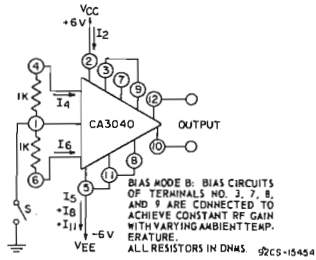
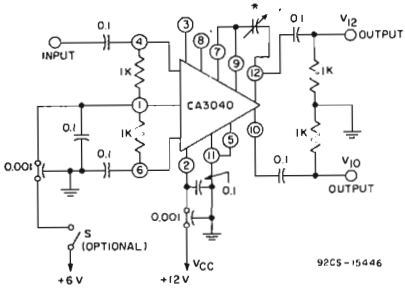


Fig.2(b) - Bias Mode B

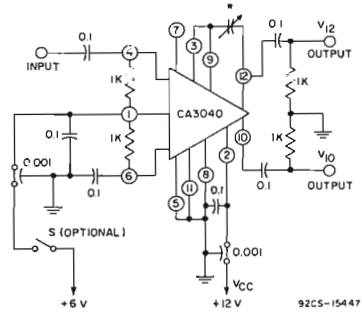
DYNAMIC CHARACTERISTICS TEST CIRCUITS FOR CA3040



* VARIABLE CAPACITANCE (0.5–1.0 μF) ADJUSTMENT FOR EQUAL 3dB BANDWIDTH AT AMPLIFIER OUTPUTS, TERMINALS 10 AND 12.

ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED)
BIAS MODE A IS AS DEFINED IN FIG. 2 (a)

Fig.3(a) - Bias Mode A



* SEE FIG 3(a)

BIAS MODE B IS AS DEFINED IN FIG 2(b)
ALL RESISTORS IN OHMS
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).

Fig.3(b) - Bias Mode B

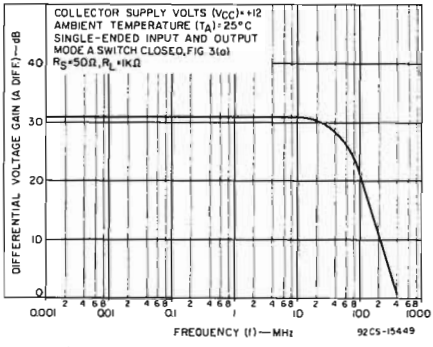


Fig.4 - Differential Voltage Gain vs Frequency

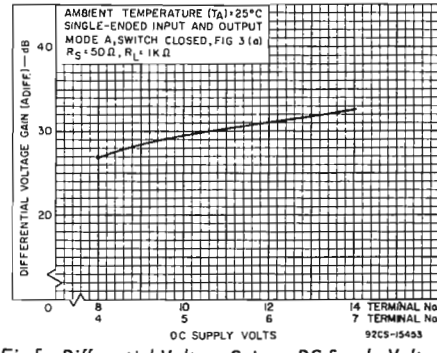


Fig.5 - Differential Voltage Gain vs DC Supply Voltages

OPERATING CONSIDERATIONS

General

The CA3040 is designed to provide flexibility in the selection of power supply configurations and to provide the circuit designer the choice between two modes of temperature-compensated performance. Mode A, which provides constant DC output voltage, is recommended for most applications. The control of the operating point provided by this mode maintains the dynamic range of the device while gain variation over most of the range is less than ±1 dB. Mode B provides constant gain for applications where this consideration is critical, but will exhibit a reduction of dynamic range at the temperature extremes.

Power Supply Considerations

Figures 2 and 3 illustrate the use of the CA3040 with balanced dual supplies and single power supplies, respectively. Both figures demonstrate that the inputs may be directly referenced to the center point of the supply (ground in Fig.2) by closing the included switch. This is the natural connection in Fig.2. This connection is optional, however, and need not be made. Use of this connection in Fig.3 implies the presence of another DC supply or a "stiff" bleeder. If such a source is present its use is suggested in order to maintain maximum common mode range. Dynamic performance and dynamic range of the output circuit are unaffected by the choice of biasing scheme used so that in most cases direct connection of Terminal No.1 to the center point of the supply is not required. Where direct connection is not used, Terminals No.4 and No.6 must be biased from Terminal No.1 for proper operation.

High-Frequency Considerations

Stable high-frequency operation requires that proper high-frequency construction techniques be followed. The photograph of Fig.6 illustrates the precautions taken in the construction of the test circuit of Fig.3.

Extreme caution is required because of the extended gain bandwidth capability of the device. Oscillations have been observed in the 400-to-800 MHz range when precautions were not taken. In addition to normal considerations of shielding, parts layout, and isolation, the following specific suggestions are made:

1. Use sockets only when necessary. Sockets, when used, must provide shielding within the pin circle. The socket shown in the chassis of Fig.6 is a Barnes MG-1201, or equivalent, modified by drilling a 1/8" hole in the center and inserting a grounded brass pin.
2. Do not bypass Terminal No.9 in normal operation. Fig.3 shows the use of neutralization between Terminal No.9 and one output to balance the amplifier at high frequencies. Experience shows that stable operation, while possible, is difficult to achieve if Terminal No.9 is bypassed to ground.
3. In DC testing, 1 kΩ, 1/4 W carbon resistors should be soldered directly to the socket Terminals No.4 and No.6 to suppress parasitic oscillations. All current carrying connections are made at the other end of the resistors. Direct sensing of Terminal No.4 or No.6 voltage should not be attempted.

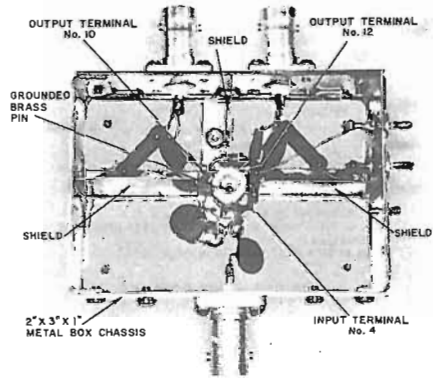


Fig.6 - Test Circuit Layout

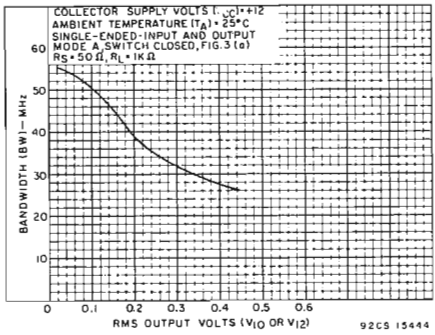


Fig.7 - 3dB Bandwidth vs Single-Ended Output Voltage

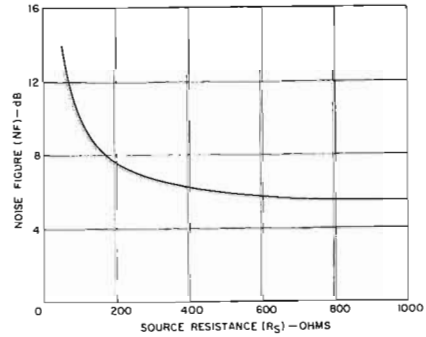


Fig.8 - Noise Figure (NF) vs Source Impedance

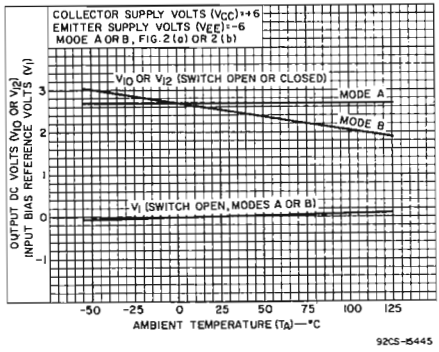


Fig.9 - Output Volts or Input Bias Reference Volts vs Ambient Temperature

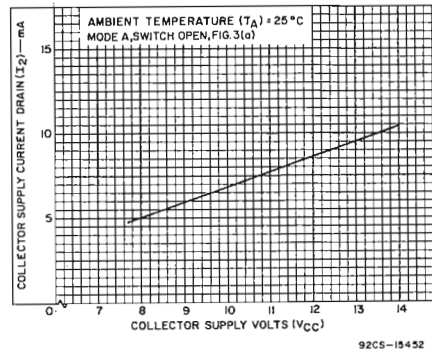


Fig.10 - Collector Supply Current Drain (I_2) vs Collector Supply Voltage (V_{CC})

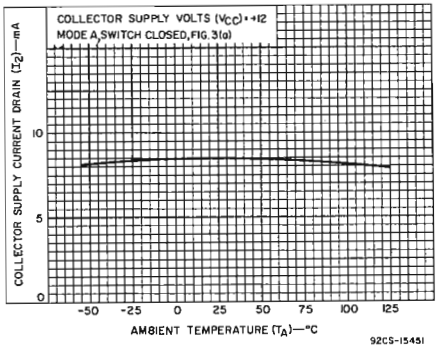


Fig.11 - Collector Supply Current Drain (I_2) vs Ambient Temperature

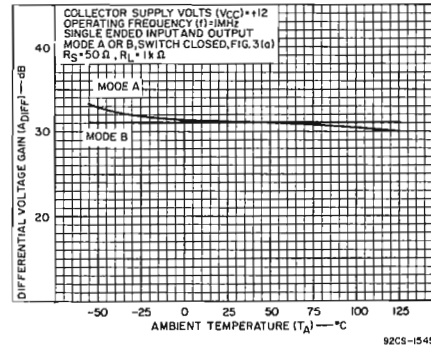


Fig.12 - Single-Ended Differential Voltage Gain vs Ambient Temperature

RCA Solid State Division

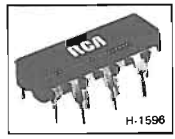
Linear Integrated Circuits

CA3041

WIDE-BAND AMPLIFIER, FM DETECTOR AF PREAMPLIFIER/DRIVER

Monolithic Silicon

For Sound Sections of TV Receivers Using Tube-Type AF Output Amplifiers



RCA Integrated Circuit Type CA3041 provides, in a single monolithic silicon chip, a major subsystem for the sound sections of TV receivers. As shown in the Schematic Diagram (Fig.1) and the TV Receiver Block Diagrams (Fig.2) the CA3041 contains a multistage wide-band if-amplifier/limiter section, an FM-detector stage, a Zener-diode-regulated power-supply section, and an af-amplifier section specifically designed to drive directly a 6AQ5 beam power tube or other audio output tube of similar characteristics.

In FM receivers, the CA3041 can be used to provide if amplification and limiting, FM detection, and af preamplification.

The CA3041 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The CA3041 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device in suitably punched printed-circuit boards. Templates showing recommended layout of printed-circuit boards for the CA3041 are provided in this bulletin (Figs. 13, 14 and 15).

FEATURES

- high-sensitivity – input limiting voltage (knee) = 150 μV typ. at 4.5 MHz
- large audio drive voltage capability
- excellent AM rejection – 58 dB typ. at 4.5 MHz
- inherent high stability – internally shielded
- internal Zener-diode-regulated voltage supply
- low harmonic radiation
- wide frequency capability – <100 kHz to > 20 MHz
- low harmonic distortion

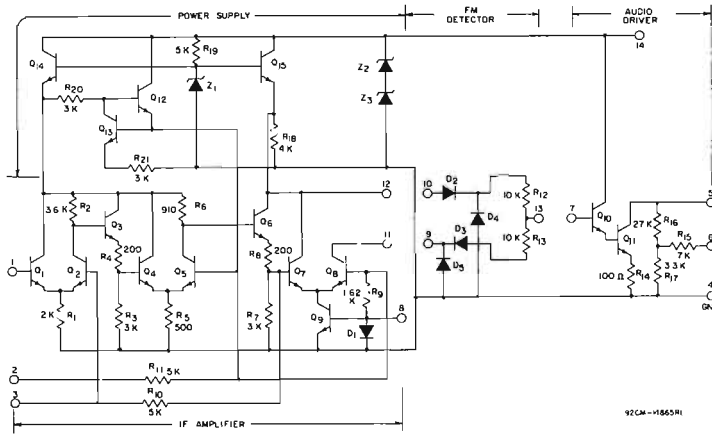


Fig.1 - Schematic diagram.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS AT T_A = 25°C

Indicated voltage or current limits for each terminal may be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 4).

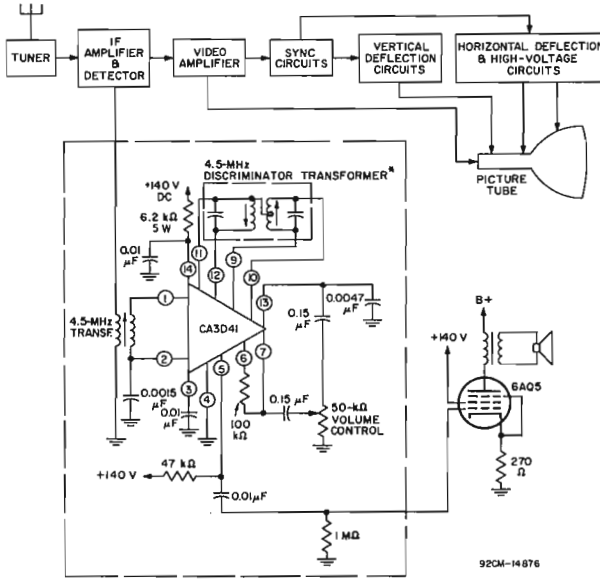
TERMINAL	VOLTAGE OR CURRENT LIMITS	VOLTAGE CONDITIONS AT OTHER TERMINALS													
		1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	-3 V to +3 V	–	AT SAME DC VOLTAGE AS TERMINAL 1	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	GROUND (VOLTAGE REFERENCE TERMINAL)	CONNECTED TO +140 V THROUGH 47 kΩ RESISTOR*	CONNECTED TO TERMINAL 7 THROUGH 100 kΩ RESISTOR*	AF-INPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 9)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 10)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 11)	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AT TERMINAL 12 (EXCEPT TERMINAL 13)	CONNECTED TO +140 V DC THROUGH 6.2-kΩ RESISTOR*
2	-3 V to +3 V	-3 to +3													
3	-3 V to +3 V	-3 to +3													
4	GROUND (VOLTAGE REFERENCE TERMINAL)	-3 to +3													
5	20 mA	-3 to +3													
6	0 V to +10 V	-3 to +3													
7	10 mA	-3 to +3													
8	10 mA	-3 to +3													
9	10 mA	-3 to +3													
10	10 mA	-3 to +3													
11	+2.5 V to +5 V	-3 to +3													
12	+2.5 V to +5 V	-3 to +3													
13	+2.5 V to +5 V	-3 to +3													
14	50 mA	-3 to +3													

* Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Device Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3041 to be exceeded may be used.

OPERATING-TEMPERATURE RANGE ..... −40° to +85°C
STORAGE-TEMPERATURE RANGE ..... −65° to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 seconds max. ..... +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE:
Between Terminals 1 and 3 ..... ±3 V
MAXIMUM DEVICE DISSIPATION:
At Ambient Temperatures up to +25°C ..... 950 mW
above +25°C ..... Derate at 10.8 mW/°C

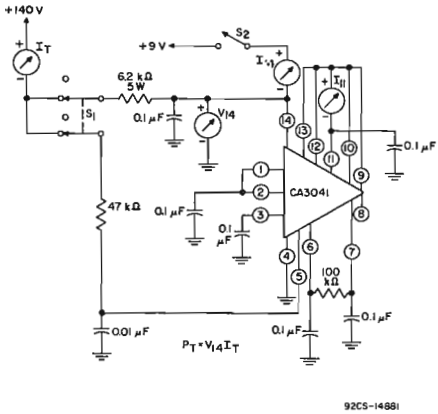
ELECTRICAL CHARACTERISTICS, *at an Ambient Temperature, T_A, of 25°C, and a DC Supply Voltage, V_{CC}, of +140 Volts applied to Terminal 14 through a resistance of 6.2 kΩ, unless otherwise indicated. Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3041 to be exceeded may be used.*

CHARACTERISTICS (See Page 7 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS: SETUP AND PROCEDURE Fig.	TEST CONDITIONS: SPECIAL CONDITIONS	LIMITS: TYPE CA3041 Min.	Typ.	Max.	Units	TYPICAL CHARACTERISTICS CURVES Fig.
Total Device Dissipation	P_T	3	T_A = 0°C	220	245	270	mW	4
			T_A = +25°C	225	250	275	mW	
			T_A = +85°C	230	255	280	mW	
Zener Regulating Voltage (DC Supply Voltage at Terminal 14)	V_{14}	–		10.5	11.2	12.3	V	–
Quiescent Operating Current (into Terminal 11)	I_{11}	3		0.25	0.63	1	mA	–
9-Volt Current Drain (Quiescent Operating Current into Terminal 14)	I_{14}	3	V_{CC} = +9 V applied directly to Terminal 14	7	11	16	mA	–
Input-Impedance Components: Parallel Input Resistance	R_i	5	f = 4.5 MHz	–	11	–	kΩ	–
Parallel Input Capacitance	C_i	5	f = 4.5 MHz	–	5	–	pF	–
Output-Impedance Components: Parallel Output Resistance	R_o	–	f = 4.5 MHz	–	100	–	kΩ	–
Parallel Output Capacitance	C_o	–	f = 4.5 MHz	–	4	–	pF	–
Input Limiting Voltage (Knee)	$V_{i(lim)}$	6	f = 4.5 MHz	–	150	200	μV (rms)	10
Amplitude-Modulation Rejection	AMR	7	f = 4.5 MHz	45	58	–	dB	8
IF-Amplifier Voltage Gain	$A_{(IF)}$	9	f = 4.5 MHz	–	67	–	dB	10
Recovered AF Voltage: 1. At FM-Detector Output	$V_{o(af)}$	–	f = 4.5 MHz; R_L = 50 kΩ, Δf = ±25 kHz; THD = 0.7% (typ.)	–	250	–	mV (rms)	–
2. At AF-Driver Output in Test Setup		–	f = 4.5 MHz; THD 5%	8	9	–	V (rms)	–
Total Harmonic Distortion	THD	6	f = 4.5 MHz; $V_{o(af)}$ = 8 V(rms)	–	1.5	5	%	–
Discriminator Output Resistance	$R_{o(dis)}$	–	f = 1 kHz	–	10	–	kΩ	–
AF-Amplifier Input Resistance	$R_{i(af)}$	–	f = 1 kHz	–	100	–	kΩ	–
AF-Amplifier Output Resistance	$R_{o(af)}$	–	f = 1 kHz	–	30	–	kΩ	–
AF-Driver Voltage Gain	A_{af}	11	f = 1 kHz	–	41	–	dB	12



* TRW Electronics, Des Plaines, Illinois. Part No. E023874, or equivalent.

Fig.2 - Block diagram of typical TV receiver using CA3041.



PROCEDURES:

Total Device Dissipation:

1. Close S_1, open S_2.
2. Measure and record V_{14} and I_T.
3. Determine Total Device Dissipation from $P_T = V_{14} I_T$.

Quiescent Operating Current into Terminal 11:

1. Close S_1, open S_2.
2. Measure I_{11} and record as Quiescent Operating Current into Terminal 11.

9-Volt Current Drain:

1. Open S_1, close S_2.
2. Measure I_{14} and record as 9-Volt Current Drain.

Fig.3 - Test setup for total dissipation, quiescent operating current into terminal No.11, and 9-volt current drain.

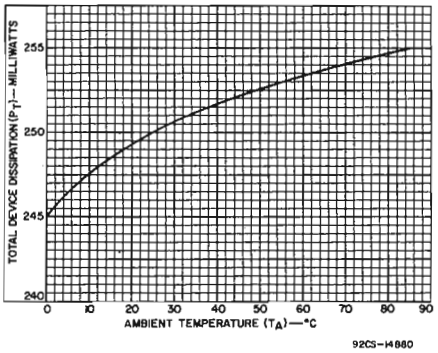


Fig.4 - Typical dissipation characteristic for CA3041.

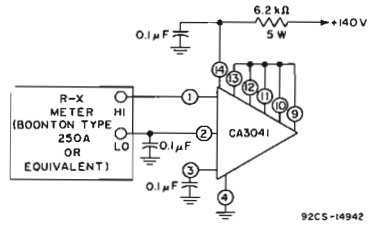
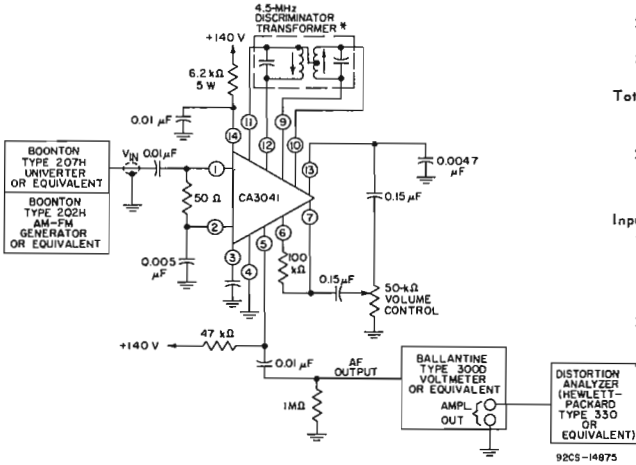


Fig.5 - Test setup for measurement of input-impedance components.



* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

Fig.6 - Test setup for measurement of input limiting voltage (Knee), recovered AF voltage, and total harmonic distortion.

PROCEDURES:

Recovered AF Voltage:

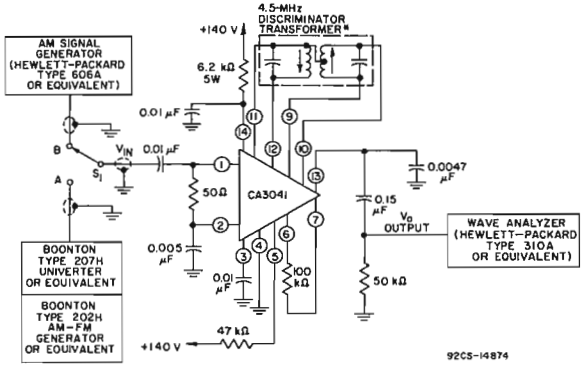
1. Set Input Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1 kHz
   Deviation = ± 25 kHz
   Output level for V_{in} = 100 mV rms
2. Set volume control for maximum af output.
3. Measure af output voltage and record as Recovered AF Voltage.

Total Harmonic Distortion:

1. Adjust volume control for an af output voltage of 300 mV rms.
2. Measure Total Harmonic Distortion of the output signal in accordance with the Operating Instructions for the Distortion Analyzer.

Input Limiting Voltage (Knee):

1. Decrease V_{in} until the af output voltage is 3 dB less than the value set in Step 1 of the procedure for measurement of Total Harmonic Distortion (300 mV - 3 dB = 210 mV)
2. Measure resulting value of V_{in} and record as Input Limiting Voltage (Knee).



PROCEDURES:

1. Set FM Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Deviation = ± 25 kHz
   Output level for V_{in} = 100 mV rms
2. Set AM Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Per cent modulation = 30
   Output level for V_{in} = 10 mV rms
3. With S_1 in Position A measure AF Output Voltage and record as $V_{o(FM)}$.
4. With S_1 in Position B measure AF Output Voltage and record as $V_{o(AM)}$.
5. Determine AM Rejection from AMR = $V_{o(FM)}/V_{o(AM)}$

* TRW Electronics, Des Plaines, Illinois. Part No. E023874, or equivalent.

Fig.7 - Test setup for measurement of AM rejection.

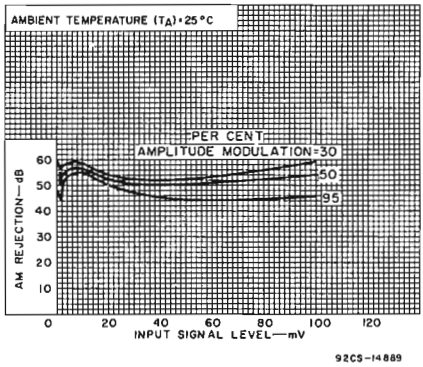
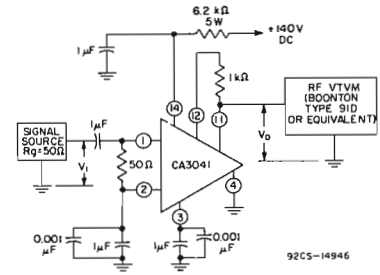


Fig.8 - Typical AM rejection characteristics for CA3041.



PROCEDURE:

A - Voltage Gain:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from A = 20 $\log_{10}$ v_o/v_i
4) Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

Fig.9 - Test setup for measurement of IF-amplifier voltage gain.

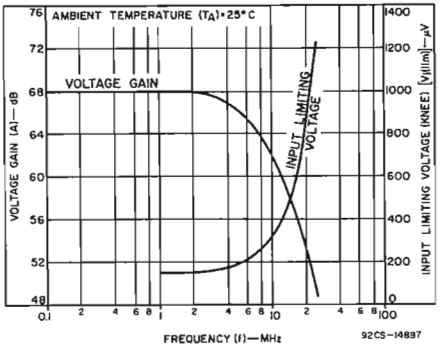


Fig.10 - Typical IF-amplifier voltage gain and input-limiting voltage (knee) charocteristics.

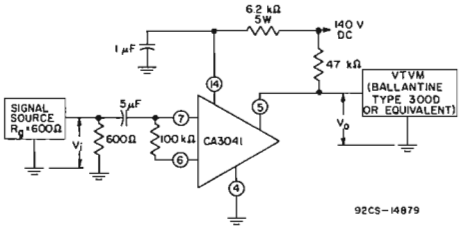


Fig.11 - Test setup for measurement of AF-amplifier voltage gain.

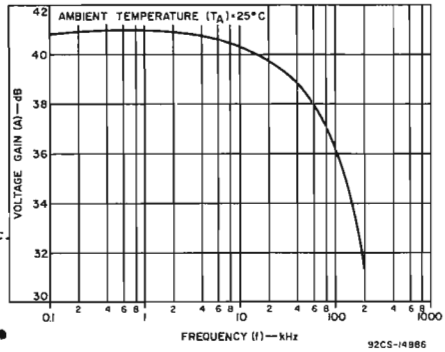


Fig.12 - Typical AF-driver voltage-goin characteristic.

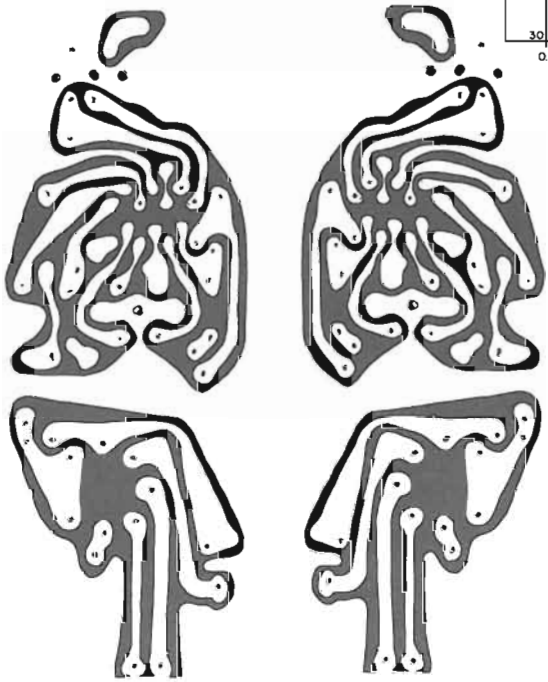


Fig.13 - Recommended layout of printed-circuit boord for complete TV-receiver sound strip utilizing RCA-CA3041 (Top View).

Fig.14 - Recommended layaut of printed-circuit board for complete TV-receiver sound strip utilizing RCA-CA3041 (Bottom View).

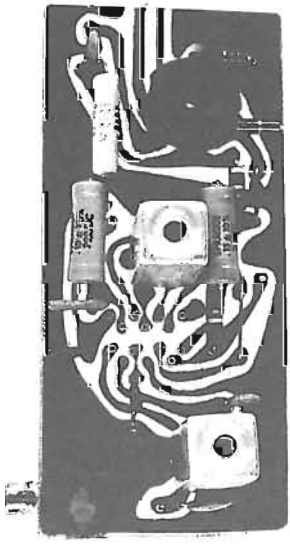


Fig.15 - Recommended parts layout for TV-receiver saund strip utilizing RCA-CA3041. (Top View)

RCA Solid State Division

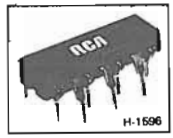
Linear Integrated Circuits

CA3042

WIDE-BAND AMPLIFIER, FM DETECTOR AF PREAMPLIFIER/DRIVER

Monolithic Silicon

For Sound Sections of TV Receivers Using Transistor-Type AF Output Amplifiers



RCA Integrated Circuit Type CA3042 provides, in a single monolithic silicon chip, a major sub-system for the sound sections of TV receivers. As shown in the Schematic Diagram (Fig.1) and the TV Receiver Block Diagrams (Figs.2A and 2B) the CA3042 contains a multistage wide-band if-amplifier section, an FM-detector stage, a Zener-diode-regulated power-supply section, and an af-amplifier section specifically designed to drive directly an n-p-n audio output transistor or a high-gain audio output pentode tube.

In FM receivers, the CA3042 can be used to provide if amplification and limiting, FM detection, and af preamplification.

The CA3042 provides exceptional versatility of circuit design because the if-amplifier-limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The CA3042 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device in suitably punched printed-circuit boards. Templates showing recommended layout of printed-circuit boards for the CA3042 are provided in this bulletin (Figs.13 & 14).

FEATURES

- high sensitivity – input limiting voltage (knee) = 150 μV typ. at 4.5 MHz
- 6-mA audio drive capability
- excellent AM rejection – 58 dB typ. at 4.5 MHz
- inherent high stability – internally shielded
- internally Zener-diode-regulated voltage supply
- low harmonic radiation
- wide frequency capability – 100 kHz to > 20 MHz
- low harmonic distortion

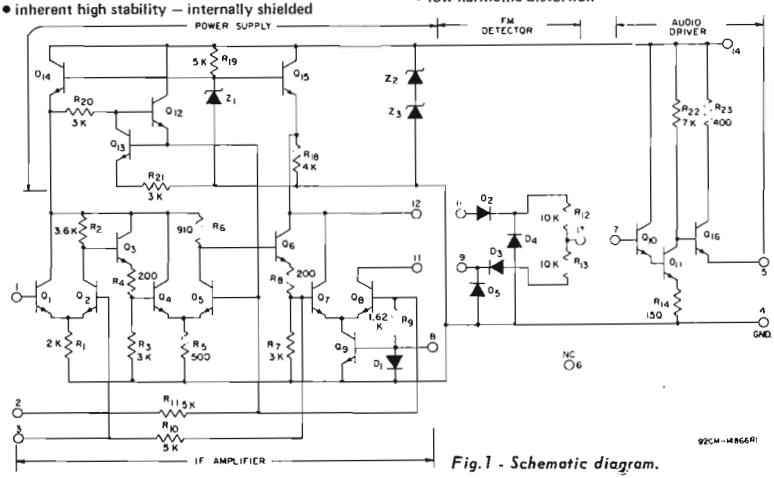


Fig.1 - Schematic diagram.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS AT T_A = 25°C

Indicated voltage or current limits for each terminal may be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 4).

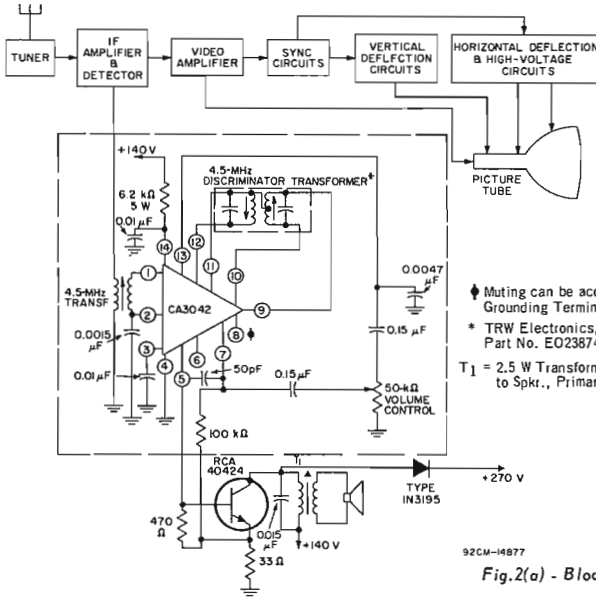
TERMINAL	VOLTAGE OR CURRENT LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS													
			1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	-3 V	+3 V	–	AT SAME DC VOLTAGE AS TERMINAL 1	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	GROUND (VOLTAGE REFERENCE TERMINAL)	AF-DRIVER OUTPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	NO CONNECTION	AF-INPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	MUTING TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL EXCEPT THAT TERMINAL MAY BE GROUNDED TO OBTAIN MUTING ACTION)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 9)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 10)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 11)	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AT TERMINAL 12 (EXCEPT TERMINAL 13)	CONNECTED TO +140 V DC THROUGH 6.2-kΩ RESISTOR*
2	-3 V	+3 V	-3 to +3													
3	-3 V	+3 V	-3 to +3													
4	GROUND (VOLTAGE REFERENCE TERMINAL)		-3 to +3													
5	20 mA		-3 to +3													
6	NO CONNECTION		-3 to +3													
7	10 mA		-3 to +3													
8	10 mA		-3 to +3													
9	10 mA		-3 to +3													
10	10 mA		-3 to +3													
11	+2 V	+10 V	-3 to +3													
12	+2.5 V	+10 V	-3 to +3													
13	0 V	+10 V	-3 to +3													
14	50 mA		-3 to +3													

* Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Device Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3042 to be exceeded may be used.

OPERATING-TEMPERATURE RANGE ..... −40° to +85°C
STORAGE-TEMPERATURE RANGE ..... −65° to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 seconds max. ..... +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE:
Between Terminals 1 and 3 ..... ±3 V
MAXIMUM DEVICE DISSIPATION:
At Ambient } up to +25°C ..... 950 mW
Temperatures } above +25°C ..... Derate at 10.8 mW/°C

ELECTRICAL CHARACTERISTICS, *at an Ambient Temperature, T_A, of 25°C, and a DC Supply Voltage, V_{CC}, of +140 Volts applied to Terminal 14 through a resistance of 6.2 kΩ, unless otherwise indicated. Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3042 to be exceeded may be used.*

CHARACTERISTICS (See Page 7 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS: SETUP AND PROCEDURE Fig.	TEST CONDITIONS: SPECIAL CONDITIONS	LIMITS: TYPE CA3042 Min.	Typ.	Max.	Units	TYPICAL CHARACTERISTICS CURVES Fig.
Total Device Dissipation	P_T	3	T_A = 0°C	200	230	260	mW	4
			T_A = +25°C	210	240	270	mW	
			T_A = +85°C	220	250	280	mW	
Zener Regulating Voltage (DC Supply Voltage at Terminal 14)	V_{14}	–		10.5	11.2	12.3	V	–
Quiescent Operating Current (into Terminal 11)	I_{11}	3		0.25	0.63	1	mA	–
9-Volt Current Drain (Quiescent Operating Current into Terminal 14)	I_{14}	3	V_{CC} = +9 V applied directly to Terminal 14	8	12	18	mA	–
Input-Impedance Components: Parallel Input Resistance	R_I	5	f = 4.5 MHz	–	11	–	kΩ	–
Parallel Input Capacitance	C_I	5		–	5	–	pF	–
Output-Impedance Components: Parallel Output Resistance	R_O	–		–	100	–	kΩ	–
Parallel Output Capacitance	C_O	–		–	4	–	pF	–
Input Limiting Voltage (Knee)	$V_{i(lim)}$	12		–	150	200	μV (rms)	9
Amplitude-Modulation Rejection	AMR	6		45	58	–	dB	7
IF-Amplifier Voltage Gain	$A_{(IF)}$	8		–	67	–	dB	9
Recovered AF Voltage: 1. At FM-Detector Output	$V_{o(af)}$	12	Δf = ±25 kHz; R_L = 50 kΩ, THD = 0.7% (typ.)	–	250	–	mV (rms)	–
2. At AF-Driver Output in Test Setup		12	R_L = 322 Ω, THD < 5%	500	800	–	mV (rms)	–
3. At AF-Driver Output in TV-Receiver Sound System		2A or 2B	R_L = 150 kΩ, THD = 1.5% (typ.)	–	3	–	V (rms)	–
Total Harmonic Distortion: 1. In Test Setup	THD	12	$V_{o(af)}$ = 500 mV (rms)	–	1.5	5	%	–
2. In TV Receiver Sound System		2A or 2B	$V_{o(af)}$ = 1.3 V (rms)	–	1	–	%	–
FM-Detector Output Resistance	$R_{o(det)}$	–	f = 1 kHz	–	10	–	kΩ	–
AF-Driver Input Resistance	$R_{I(af)}$	–		–	100	–	kΩ	–
AF-Driver Output Resistance	$R_{O(af)}$	–		–	250	–	Ω	–
AF-Driver Voltage Gain	A_{af}	10	R_S = 50 Ω, C_1 = 0	–	30	–	dB	11

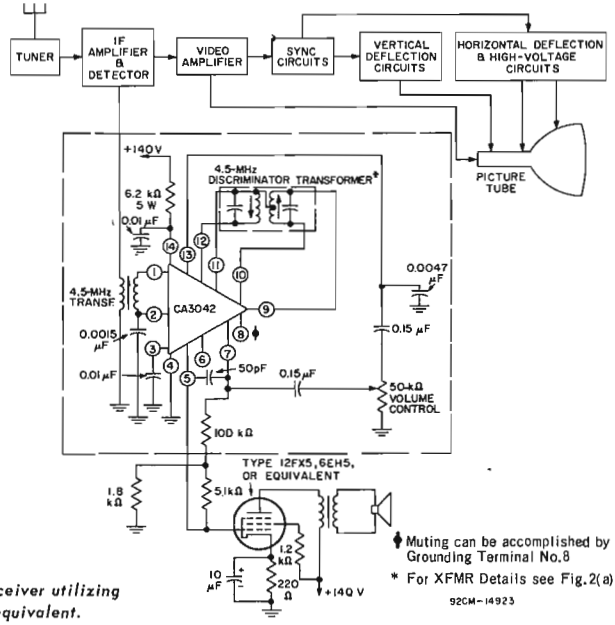


♦ Muting can be accomplished by Grounding Terminal No.8

* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

T_1 = 2.5 W Transformer, Impedance, 3500 Ω to Spkr., Primary DC = 40 mA

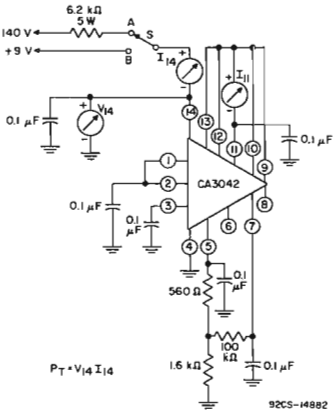
Fig.2(a) - Block diagram of typical TV receiver utilizing transistor RCA-40424.



♦ Muting can be accomplished by Grounding Terminal No.8

* For XFMR Details see Fig.2(a)

Fig.2(b) - Block diagram of typical TV receiver utilizing the CA3042 and a 12FX5, 6EH5, or equivalent.



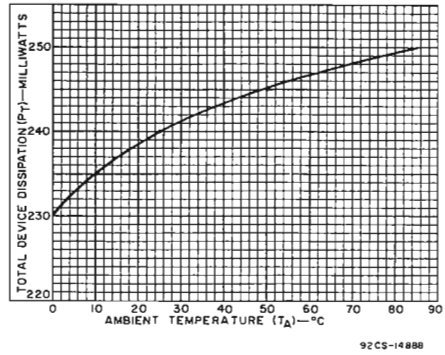


Fig.4 - Typical dissipation characteristic.

PROCEDURES:

Total Device Dissipation:

1. Set switch S in position A
2. Measure and record V_{14} and I_{14}.
3. Determine Total Device Dissipation from $P_T = V_{14} I_{14}$

Quiescent Operating Current into Terminal 11:

1. Turn switch S to position B
2. Measure I_{11} and record as Quiescent Operating Current into Terminal 11.

9-Volt Current Drain:

1. Set switch S in position B
2. Measure I_{14} and record as 9-Volt Current Drain.

Fig.3 - Test setup for meosurement of total device dissipation, quiescent current into terminal No.11, and 9-volt current drain.

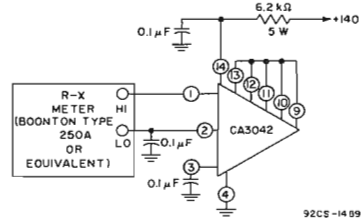
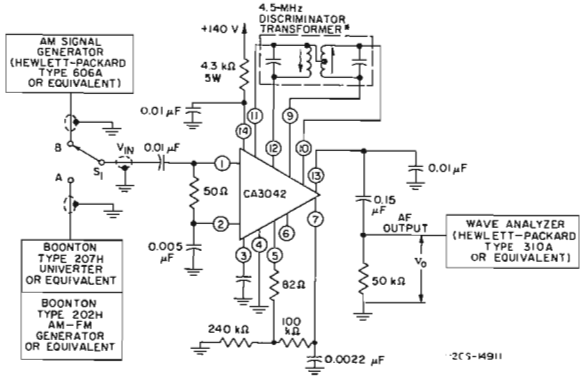


Fig.5 - Test setup for measurement of input-impedance components.



PROCEDURES:

1. Set FM Signal Generator as follows:
   Output Frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Deviation = ±25 kHz
   Output level for V_{in} = 100 mV rms
2. Set AM Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Per cent modulation = 30
   Output level for V_{in} = 10 mV rms
3. With S_1 in Position A measure AF Output Voltage and record as $V_{o(FM)}$.
4. With S_1 in Position B measure AF Output Voltage and record as $V_{o(AM)}$.
5. Determine AM Rejection from AMR = $\frac{V_{o(FM)}}{V_{o(AM)}}$

* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

Fig.6 - Test setup for measurement of AM rejection.

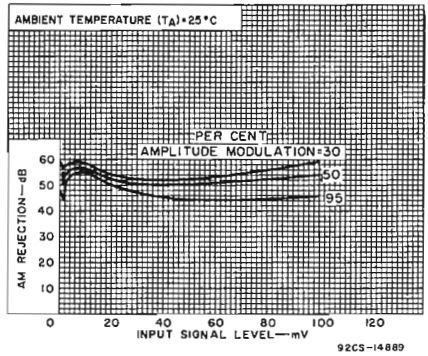
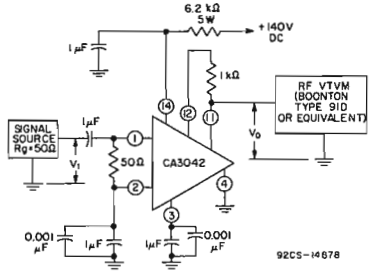


Fig.7 - Typical AM rejection characteristics.



PROCEDURE Voltage Gain:

1. Set input frequency at desired value, v_i = 100 μV rms.
2. Record v_o.
3. Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$.
4. Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

Fig.8 - Test setup for measurement of IF amplifier voltage gain.

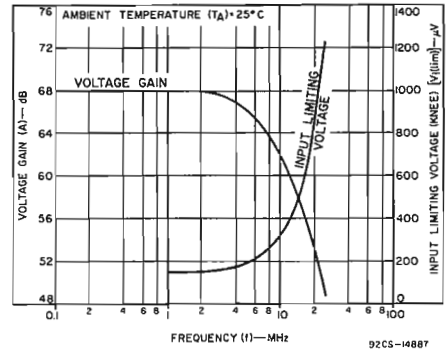


Fig.9 - Typical IF amplifier voltage gain and input limiting voltage (knee) characteristics.

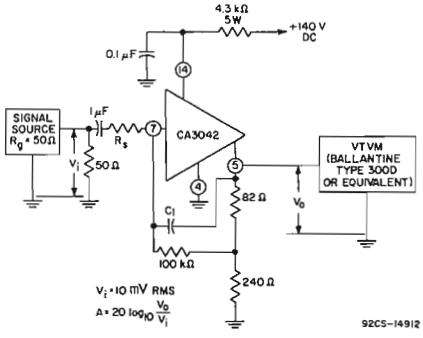


Fig.10 - Test setup for measurement of AF amplifier voltage gain.

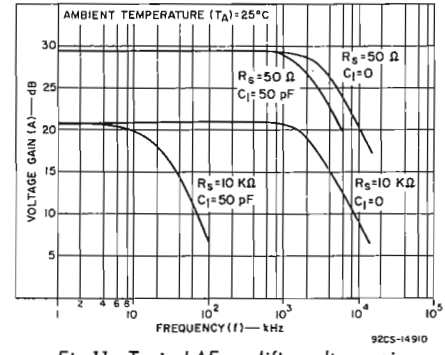
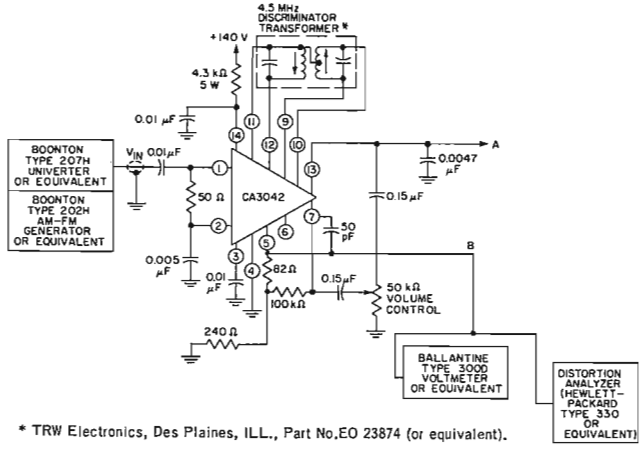


Fig.11 - Typical AF amplifier voltage gain characteristics.



* TRW Electronics, Des Plaines, ILL., Part No.EO 23874 (or equivalent).

PROCEDURES:

Recovered AF Voltage:

1. Set Input Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1 kHz
   Deviation = ±25 kHz
   Output level for V_{in} = 100 mV rms
2. Set volume control for maximum af output
3. Measure af output voltage and record as Recovered AF Voltage.

Total Harmonic Distortion:

1. Adjust volume control for an af output voltage of 500 mV rms.
2. Measure Total Harmonic Distortion of the output signal in accordance with the Operating Instructions for the Distortion Analyzer.

Input Limiting Voltage (Knee):

1. Decrease V_{in} until the af output voltage is 3 dB less than the value set in Step 1 of the procedure for measurement of Total Harmonic Distortion (500mV - 3 dB = 350 mV)
2. Measure resulting value of V_{in} and record as Input Limiting Voltage (Knee).

Fig.12 - Test setup for measurement of input limiting voltage (knee), recovered AF voltage, and total harmonic distortion.

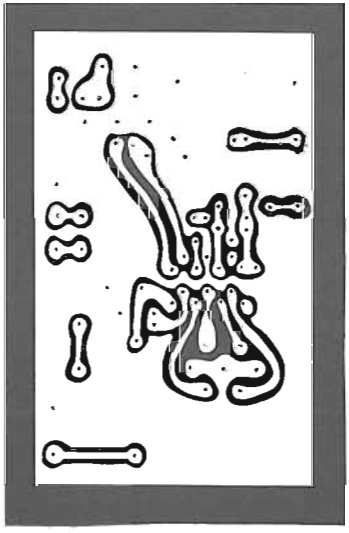


Fig.13 - Recommended layout of printed-circuit board for TV-receiver sound strip utilizing RCA-CA3042. (Bottom View)

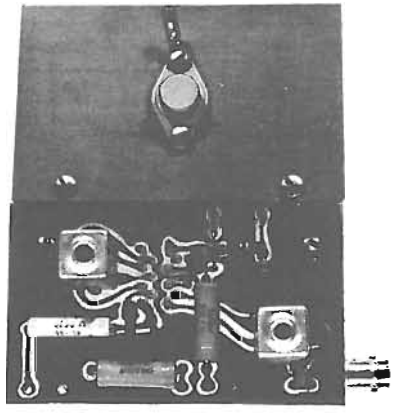


Fig.14 - Recommended parts layout for TV-receiver sound strip utilizing RCA-CA3042. (Top View)

RCA Solid State Division

Linear Integrated Circuits

CA3043

Special-Function Sub-System

Monolithic Silicon

HIGH-GAIN IF AMPLIFIER, LIMITER, FM DETECTOR, AND AF PREAMPLIFIER/DRIVER

For FM IF Amplifier Applications in Communications Receivers and High-Fidelity FM Receivers up to 20 MHz

RCA Integrated Circuit Type CA3043 provides in a single monolithic silicon chip, a major sub-system for the IF sections of Communications and high-fidelity FM receivers. As shown in the Schematic Diagram (Fig.2) and the FM Receiver Block Diagram (Fig.1), the CA3043 contains a multistage if-amplifier/limiter section, an FM-detector stage, a Zener-diode regulated power-supply section, and an af-amplifier section. In FM receivers, the CA3043 can be used to provide if amplification and limiting, FM detection, and af preamplification. The CA3043 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The four stage emitter-follower-coupled if amplifier section provides 80-dB voltage gain at 10.7 MHz, and features an output stage with exceptionally good limiting characteristics because of its transistor constant-current sink.

The FM detector section is distinguished by circuitry which provides forward bias to the detector diodes, D2 and D3, and also provides a reference voltage for AFC.

The audio amplifier provides a low-impedance drive for subsequent audio amplifiers.

The power supply section provides zener-regulated, decoupled voltages for the IF amplifier, detector, and audio amplifier sections.

FEATURES

- high sensitivity – – input limiting voltage (knee) 50 μV typ. at 10.7 MHz
- excellent AM rejection – – 58 dB typ. at 10.7 MHz
- inherent high stability – – internally shielded
- internal Zener-diode regulated voltage supply
- low harmonic radiation
- wide frequency capability – – <100 kHz to >20 MHz
- low harmonic distortion

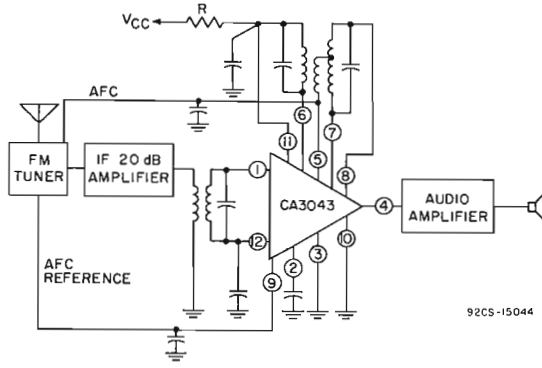


Fig.1 - Typical applicatian of the CA3043 as a high-gain limiter, amplifier-detectar in an FM receiver.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C

DISSIPATION:
At T_A = 25°C to T_A = 85°C . . . . . 450 mW
Above T_A = 85°C . . . . . Derate linearly 5 mW/°C

TEMPERATURE RANGE:
Operating . . . . . -55°C to + 125°C
Storage . . . . . -65°C to + 150°C

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 min)
from case for 10 seconds max . . . . . + 265°C

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range between horizontal terminal 5 and vertical terminal 3 is +6 to 0 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		+4 -4	0 -5	*	*	*	*	*	*	0 -5	*	Note(1)
2			0 -3	*	*	*	*	*	*	0 -3	*	*
3				+6 0	+6 0	+15 +2	+6 0	+6 0	+6 0	0	Note(2)	+3 0
4					+2 -4	*	*	*	*	0 -6	*	*
5						*	*	*	*	0 -6	+6 0	*
6							*	*	*	-2 -15	*	*
7								Note(1)	*	0 -6	*	*
8									*	0 -6	*	*
9										0 -6	*	*
10											Note(2) 0	+3 0
11												*
12												

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	-
2	-	-
3	0.1	40
4	-	20
5	-	-
6	-	-
7	-	-
8	-	-
9	-	20
10	0.1	40
11	40	0.1
12	-	-

Note 1: These terminals should be connected through a dc resistance to any terminal which does not exceed 100 ohms.

Note 2: Pin 11 may be connected to any positive voltage source through a suitable resistor provided its current rating is not exceeded.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUIT AND PROCEDURE	LIMITS TYPE CA3043			UNITS
			Fig.	Min.	Typ.	Max.	
STATIC CHARACTERISTICS							
Current Drain at 6V into Pin No.11	I_{11}	V_{CC} = +6V	3	10	16	20	mA
Regulator Voltage Pin No.11	V_{11}	V_{CC} = +30V, R_S = 750 Ω	3	6.9	7.4	8	V
Total Device Dissipation	P_T		3	200	225	260	mW
Quiescent Operating Current into Pin No.6	I_6		3	-	0.65	-	mA
DYNAMIC CHARACTERISTICS at V_{CC} = +30V, R_S = 750 Ω, f = 10.7 MHz							
Voltage Gain	A_v		4	72	80	-	dB
Input Limiting Voltage (knee)	v_i(lim)	v_o(af) at -3 dB point	6	-	50	-	μV (RMS)
Limiting Current from Pin No.6	I_6(lim)		4	-	0.42	-	mA (RMS)
Recovered AF Voltage	v_o(af)	v_i = 1 mV (RMS) f (modulating) = 1 kHz Deviation = ± 75 kHz	6	75	110	150	mV (RMS)
Amplitude-Modulation Rejection	AMR	v_i = 10 mV f (modulating) = 1 kHz % modulation = 50%	8	-	58	-	dB
Total Harmonic Distortion	THD	v_i = 1 mV (RMS)	6	-	0.3	-	%
Input Impedance Components:							
Parallel Input Resistance	R_I		-	-	7	-	kΩ
Parallel Input Capacitance	C_I		-	-	5	-	pF

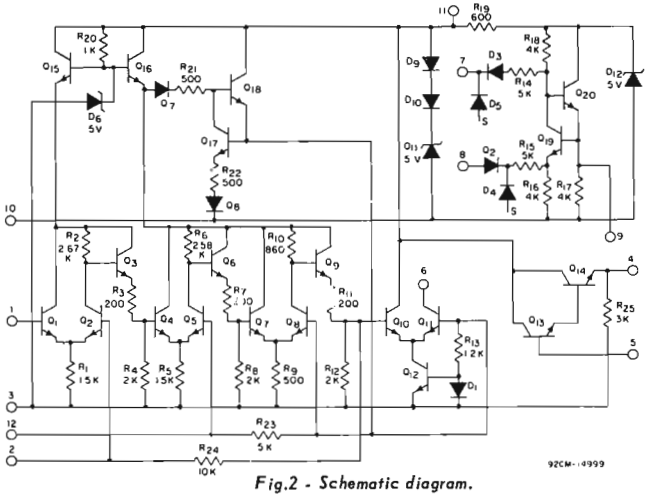


Fig.2 - Schematic diagram.

Notes:

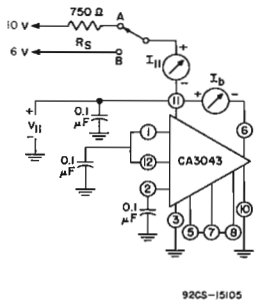
S = Substrate

Terminal No.3 wire-connected to the case.

Terminal No.10 connected to the case through the substrate.

Terminals No.3 and 10 which are connected to the substrate should be connected to the most negative point in the circuit.

Diodes D_4 and D_5, act as capacitors and are used to balance the detector substrate capacitances.

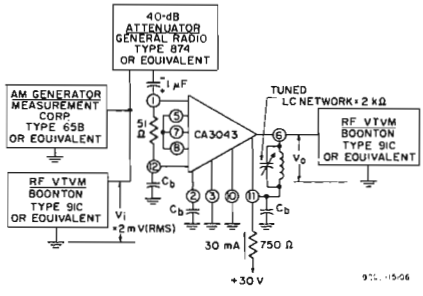


Switch in Position A for:

Regulator-Voltage, Quiescent-Operating-Current, and Device Dissipation Test

Switch in Position B for Current into Pin No. 11

Fig.3 - Regulator voltage, device dissipation, quiescent operating current, and current at 6 volts into Pin No. 11.



Voltage Gain = $20 \log_{10} 100 \frac{V_o}{V_i}$

C_b - Bypass Capacitor, 0.1 μF electrolytic in parallel with 0.01 μF

$I_{6(lim)} = \frac{V_o}{2K\Omega}$, v_i = 100 mV(RMS)

* Output circuit should be completely shielded from the input circuit at the socket.

Fig.4 - Voltage gain test circuit.

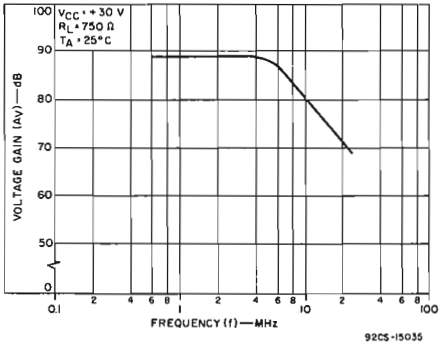
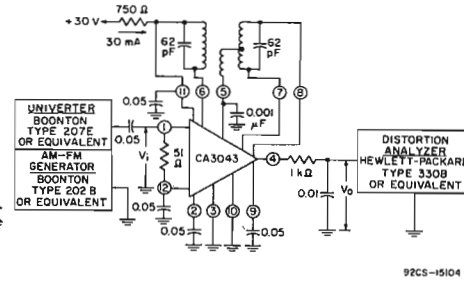


Fig.5 - Voltage gain vs frequency.



PROCEDURE:

1. Recovered Audio Voltage $v_{o(af)}$ –

   Set input frequency to 10.7 MHz,

   v_i = 1 mV(RMS), modulating frequency = 1 kHz

   Deviation = ±75 kHz

   Record v_o as measured on the Distortion Analyzer meter scale.

   This is the recovered Audio Voltage $v_{o(af)}$

2. 3 dB Limiting Sensitivity $v_{i(lim)}$ –

   Reduce v_i until $v_{o(af)}$ drops 3 dB.

   Record this value of v_i as $v_{i(lim)}$

3. Total Harmonic Distortion THD –

   Reset v_i to 1 mV(RMS) and operate Distortion Analyzer per manufacturer's instructions to measure THD.

* See Fig.9 for details on Discriminator Transformer.

Fig.6 - Input limiting voltage (knee), recovered AF voltage, and total harmonic distortion test circuit.

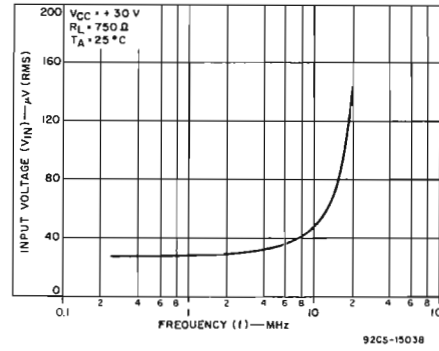
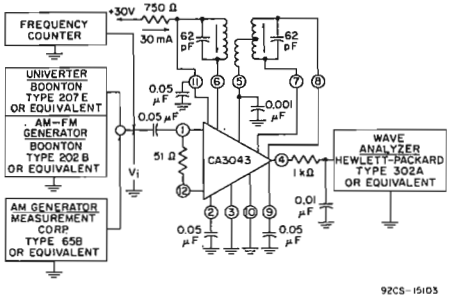


Fig.7 - Input limiting voltage (knee) at -3 dB point vs frequency.



PROCEDURE:

A. Connect FM Generator to CA3043 input.

Set frequency to 10.7 MHz, v_i = 10 mV, modulating frequency = 1 kHz

Deviation = ±75 kHz.

Tune Wave Analyzer to peak reading at 1 kHz and record recovered Audio Voltage $v_{o(af)FM}$.

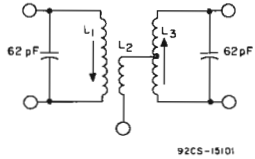
B. Disconnect FM Generator and Connect AM Generator to CA3043 input.

Set frequency to 10.7 MHz, v_i = 10 mV, modulating frequency = 1 kHz, percent modulation = 50%.

Tune Wave Analyzer to peak reading and record recovered audio voltage $v_{o(af)AM}$

Amplitude Modulation Rejection Ratio = $20 \log_{10} \frac{v_{o(af)FM}}{v_{o(af)AM}}$

Fig.8 - Amplitude modulation rejection test circuit.



Coil Form, Outside Diameter = 7/32"

Can = 1/2" square X 1-1/8" long

Slugs - Radio Industries Type MP34/MP100 Material

L_1 & L_3 = 20 Turns 5-44 litz wire universal wound

L_2 = 10 Turns 5-44 litz wire wound bifilar with L_1

L_1 & L_3 coupling adjusted to 520 kHz peak to peak separation on S curve when operated in circuit shown in Fig.6.

Fig.9 - 10.7-MHz discriminator transformer for CA3043.

RCA
Solid State
Division

Linear Integrated Circuits

CA3044
CA3044V1

Special-Function Sub-System

Manalithic Silican

The RCA CA3044 and CA3044V1 represent a second generation of integrated circuits designed primarily for AFC (Automatic-Frequency-Control) applications.

The CA3044V1 is electrically identical to the CA3044 but is supplied with formed leads for easier PC board design and construction.

CA3044

10-LEAD
TO-5

CA3044V1

FORMED
10-LEAD
TO-5

FEATURES

- Primarily intended for AFC (automatic frequency contral) Applications
- Internal Zener Diode Voltage Regulator
- Differential Input Amplifier/Limiter
- Full-Wave Diode Bridge Detector
- Differential Output Voltage Amplifier
- Available in Two Electrically Identical Versions,
  CA3044 With Straight Leads;
  CA3044V1 With Formed Leads
- Wide Operating Temperature Range; -55 to +125°C

WIDE-BAND AMPLIFIER/PHASE DETECTOR WITH ZENER DIODE VOLTAGE REGULATOR

For AFC (Automatic Frequency Control) Applications

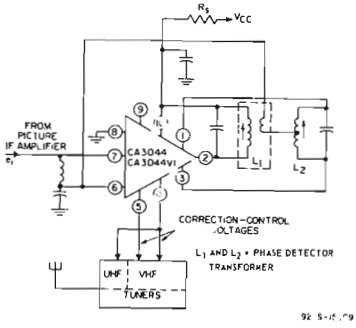


Fig.1 - Block diogram of Typical Autamatic Fine Tuning (AFT) Application using CA3044 or CA3044V1 in Calor-TV Receiver.

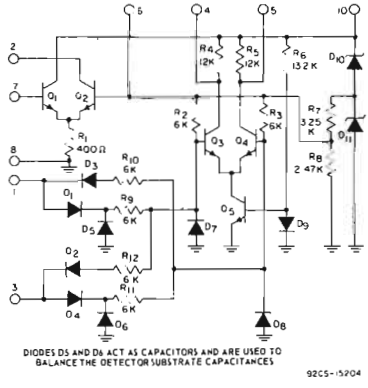


Fig.2 - Schematic diagram CA3044, CA3044V1

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION:
- At T_A = 25°C . . . . . 830 mW
- Above T_A = 25°C . . . . . Derate linearly 5.6 mW/°C

TEMPERATURE RANGE:
- Operating . . . . . -55°C to +125°C
- Storage . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . + 265C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 6 is +20 to 0 volts.

TERMINAL No.	9	10	1	2	3	4	5	6	7	8
9	NO INTERNAL CONNECTION									
10			+20 0	+20 -10	+20 0	+20 0	+20 0	+20 0	+20 0	▲
1				*	+12 -12	*	*	+6 -6	*	+6 0
2					*	*	*	+20 0	*	+20 0
3						*	*	+6 -6	*	+6 0
4							*	*	*	+12 0
5								*	*	+12 0
6									+5 -5	+5 0
7										+8 -5
8										REF. SUB-STRATE

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9	-	-
10	50	50
1	5	5
2	20	20
3	5	5
4	5	5
5	5	5
6	5	5
7	5	5
8	50	50

▲ Terminal No. 10 may be connected to any positive voltage source through a suitable dropping resistor—provided the dissipation rating is not exceeded.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS FIG.	TEST CONDITIONS	LIMITS CA3044 and CA3044V1 MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS								
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = -55°C	90	120	150	mW	-
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = 25°C	110	140	170	mW	-
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = +125°C	130	160	190	mW	-
9-Volt Current Drain	I_T	3	V_{10} = 9 V	2.5	4	5.5	mA	-
Zener Regulating Voltage - DC Supply Voltage at Terminal 10	V_{10}	3	V_{CC} = 30 V, R_S = 1.5 kΩ	10.5	11.2	11.9	V	-
Quiescent Operating Current into Terminal 2	I_2	3		1	2	4	mA	-
Quiescent Operating Voltage at Terminal 4	V_4	-		5.0	6.5	8.0	V	-
Quiescent Operating Voltage at Terminal 5	V_5	-		5.0	6.5	8.0	V	-
Output Offset Voltage between Terminals 4 and 5	V_{4-5}	-		-1.5	0	1.5	V	-
DYNAMIC CHARACTERISTICS (AS RF AMPLIFIER)								
Input Limiting Voltage (Knee)	V_i Limiting	4	f=45.75 MHz	-	75	-	mV	-
Input Admittance	y_{11}	-	f = 45.75 MHz, V_{CC} = 30 V, R_S = 1.5 kΩ	-	0.5+j1.1	-	mmho	-
Reverse Transfer Admittance	y_{12}	-		-	3.8+j3.4	-	μmho	-
Forward Transfer Admittance	y_{21}	-		-	-11.7 +10.1	-	mmho	-
Output Admittance	y_{22}	-		-	0.077+j0.9	-	mmho	-
OUTPUT vs FREQUENCY DEVIATION - AFC								
Correction-Control Voltage at Terminal 4	V corr. (4)	5	V_{CC} = +30 V, V_{in} = 200 mV RMS, f_o = MHz as indicated	% of V_{10}		% of V_{10}		
			45.750 - 0.025	85	-	-	V	6,7
			45.750 + 0.025	-	-	33	V	
			45.750 - 0.900	75	-	-	V	7
			45.750 + 0.900	-	-	43	V	
			45.750 - 1.500	-	-	85	V	
			45.750 + 1.500	33	-	-	V	
Correction-Control Voltage at Terminal 5	V corr. (5)	5	45.750 - 0.025	-	-	33	V	6,7
			45.750 + 0.025	85	-	-	V	
			45.750 - 0.900	-	-	43	V	7
			45.750 + 0.900	75	-	-	V	
			45.750 - 1.500	33	-	-	V	
			45.750 + 1.500	-	-	85	V	

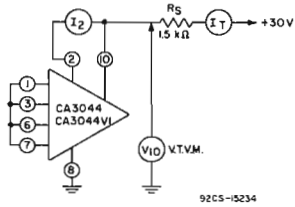


Fig.3 - Test setup: Measurement of total device dissipation, Zener regulating voltage, quiescent operating current (terminal 2).

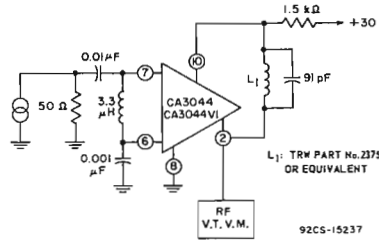


Fig.4 - Input limiting sensitivity test circuit.

DYNAMIC CONTROL VOLTAGE CHARACTERISTICS

The CA3044 and CA3044V1 are specifically intended for use in the AFT system of color television receivers. Each device is tested so that the control voltages generated by the circuit meet the critical requirements of the system. Figure 5 is the schematic diagram of the test circuit.

Figure 6 and 7 show the control voltages generated at terminals 4 and 5 of the Integrated Circuit as a function of the frequency deviation from the nominal center frequency. Figure 6 shows the region within 25 KHz of the center frequency while Figure 7 covers the entire bandwidth of the system. The horizontal reference lines on the figures are generated by a voltage divider connected between the power supply voltage on Terminal 10 and ground. The dynamic control voltages are compared with these references according to the Output vs Frequency Deviation Table. For example: when the frequency deviation is -25 KHz the control voltage at Terminal 4 is greater than the reference A voltage; the control voltage at Terminal 5 is less than the reference B voltage.

The shape of the correction voltage characteristics is dependent to a large degree upon transformer characteristics and the parts layout. In order to closely duplicate the curves shown, the printed circuit board shown in Figure 8 and the parts layout shown in Figure 9 should be followed as closely as possible.

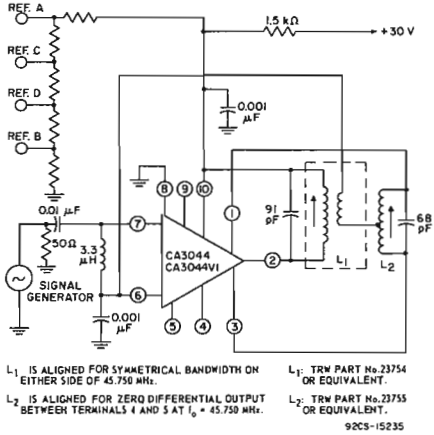


Fig.5 - Correction voltage test circuit for CA3044 and CA3044V1.

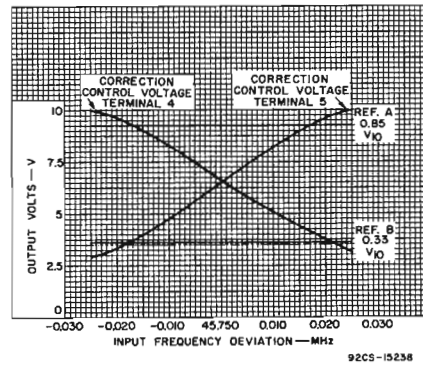


Fig.6 - Typical narrow-band dynamic control voltage characteristics.

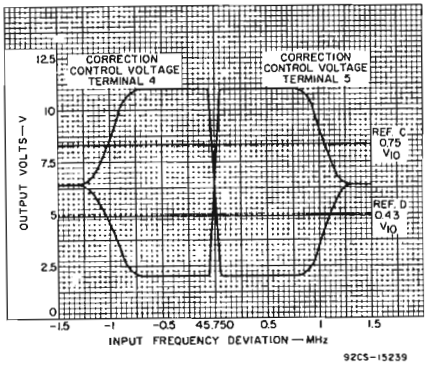


Fig.7 - Typical wide-band dynamic control voltage characteristics.

DEFINITIONS OF TERMS

Input Limiting Voltage (Knee) [v_i(lim)]

The input signal voltage which will cause the output signal to decrease 3 dB from its maximum level.

Total Device Dissipation (P_T)

The total power drain of the device with no signal applied and no external load current.

Quiescent Operating Voltage

The dc voltage at the output terminal, with respect to ground, with no signal applied.

Quiescent Operating Current

The average (dc) value of the current in either output, terminal, with no signal applied.

Output Offset Voltage

The dc voltage between output terminals with no signal applied.

Control Voltage

The dc voltage at either output terminal with respect to ground with an RF signal of specified frequency applied.

a) Top view b) Bottom view

Fig.8 - Printed Circuit Board for Test Circuit

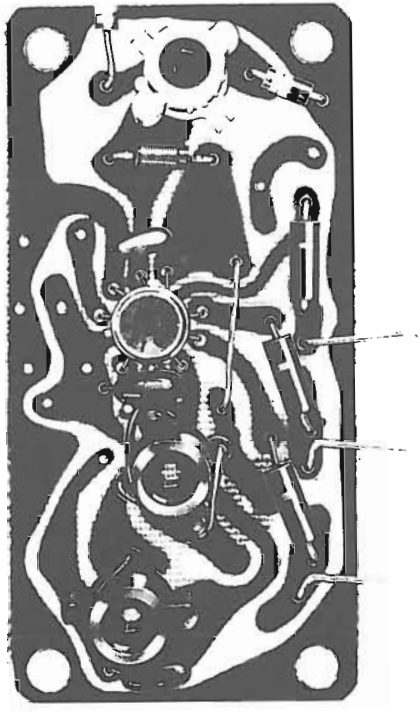


Fig.9 - Top view of wired test board.

RCA
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Monolithic Silicon

CA3045, CA3045F, CA3046

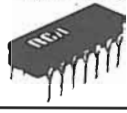
14-Lead Dual-In-Line Ceramic

H-1553

14-Lead Dual-In-Line Plastic

H-1517

14-Lead Dual-In-Line Frit-Seal



H-1806

General-Purpose Transistor Arrays

THREE ISOLATED TRANSISTORS AND ONE DIFFERENTIALLY-CONNECTED TRANSISTOR PAIR

For Low-Power Applications at Frequencies from DC through the VHF Range

The CA3045 and CA3046 each consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in a 14-lead dual-in-line hermetic (welded-seal) ceramic package and the CA3045F in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

The CA3046 is electrically identical to the CA3045 but is supplied in a dual-in-line plastic package for applications requiring only a limited temperature range.

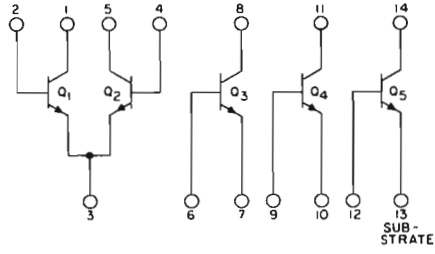


Fig.1 - Schematic diagram.

FEATURES

- Two matched pairs of transistors
  V_{BE} matched ±5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- 5 general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz
- Full military temperature range for CA3045
  -55 to +125°C

APPLICATIONS

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

	CA3045		CA3045F, CA3046		
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A up to 55°C	–	–	300	750	mW
T_A > 55°C	–	–	Derate at 6.67		mW/°C
T_A up to 75°C	300	750	–	–	mW
T_A > 75°C	Derate at 8		–	–	mW/°C
Collector-to-Emitter Voltage, V_{CEO}	15	–	15	–	V
Collector-to-Base Voltage, V_{CBO}	20	–	20	–	V
Collector-to-Substrate Voltage, V_{CIO}*	20	–	20	–	V
Emitter-to-Base Voltage, V_{EBO}	5	–	5	–	V
Temperature Range:					
Operating	–55 to +125		–55 to +125		°C
Storage	–65 to +150		–65 to +150		°C
Lead Temperature (During Soldering): At distance 1/16 ±1/32" (1.59 ±0.79 mm) from case for 10 seconds max.	+265		+265		°C

* The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046			UNITS
			MIN.	TYP.	MAX.	
STATIC CHARACTERISTICS						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10μA, I_{CI} = 0	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7	-	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	0.002	40	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	-	See curve	0.5	μA
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V, I_C = 10 mA	-	100	-	-
		V_{CE} = 3 V, I_C = 1 mA	40	100	-	-
		V_{CE} = 3 V, I_C = 10 μA	-	54	-	-
Input Offset Current for Matched Pair Q_1 and Q_2: $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.3	2	μA
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA	-	0.715	-	V
		V_{CE} = 3 V, I_E = 10 mA	-	0.800	-	
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	−1.9	-	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA	-	0.23	-	V
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	V_{CE} 3 V, I_C 1 mA	-	1.1	-	μV/°C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046			UNITS
			MIN.	TYP.	MAX.	
DYNAMIC CHARACTERISTICS						
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3V, I_C = 100 μA Source Resistance = 1 kΩ	-	3.25	-	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	-	31-j1.5	-	-
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550	-	-
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	-	2.8	-	pF

STATIC CHARACTERISTICS

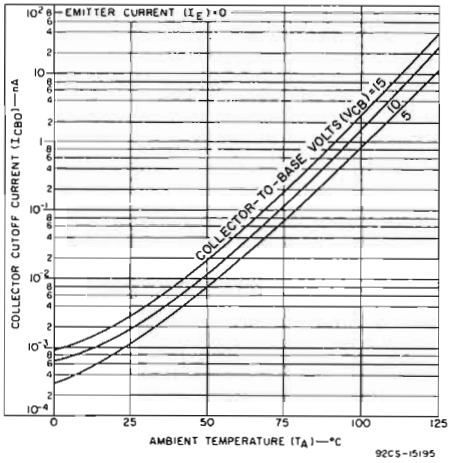


Fig.2 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

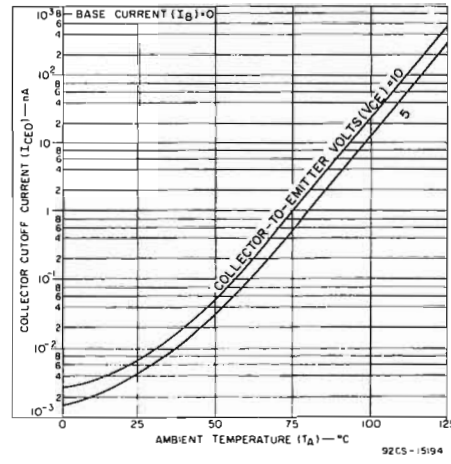


Fig.3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

STATIC CHARACTERISTICS

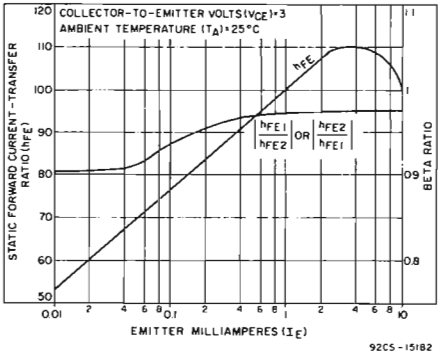


Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors Q_1 and Q_2 vs emitter current.

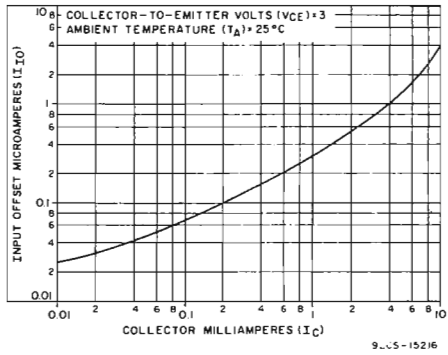


Fig.5 - Typical input offset current for matched transistor pair Q_1Q_2 vs collector current.

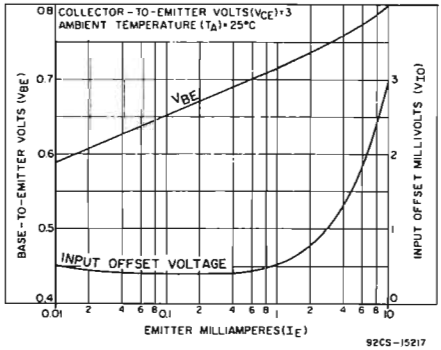


Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

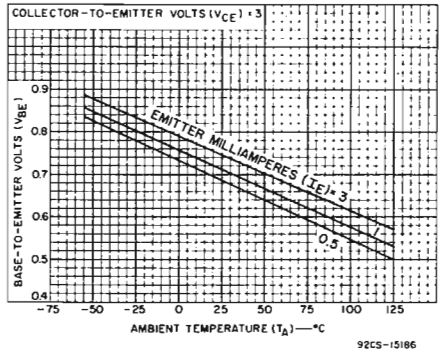


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

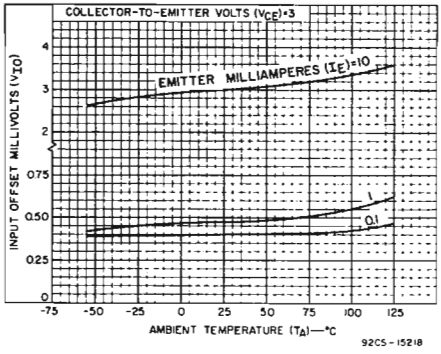


Fig.8 - Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

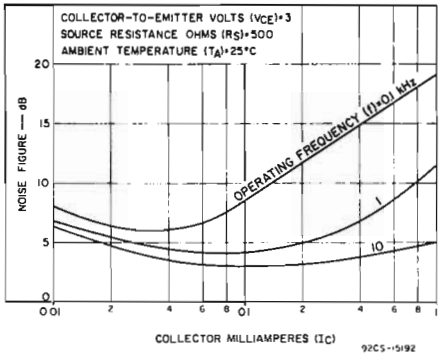


Fig.9(a) - Typical noise figure vs collector current.

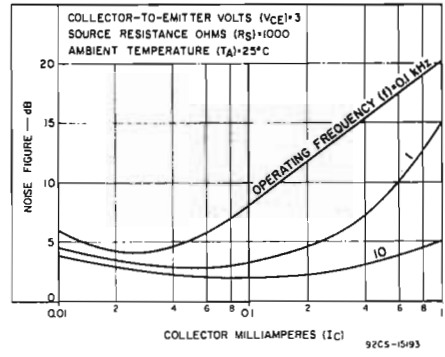


Fig.9(b) - Typical noise figure vs collector current.

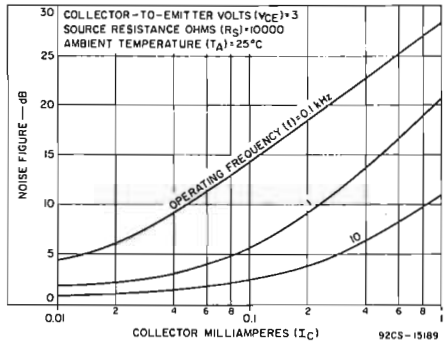


Fig.9(c) - Typical noise figure vs collector current.

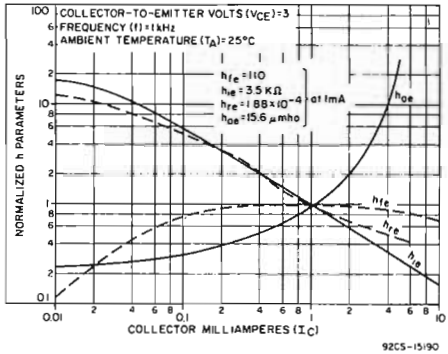


Fig.10 - Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

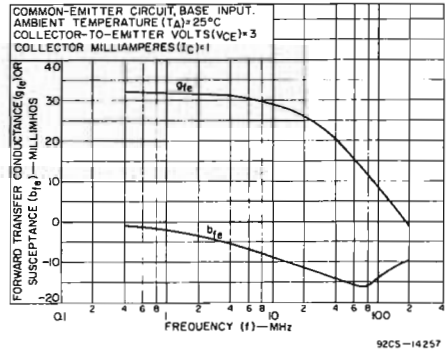


Fig.11 - Typical forward transfer admittance vs frequency.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

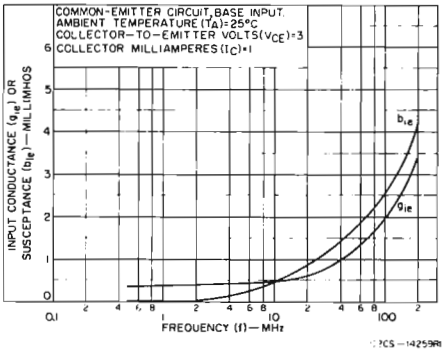


Fig.12 - Typical input admittance vs frequency.

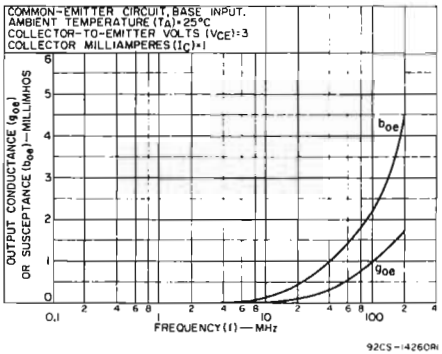


Fig.13 - Typical output admittance vs frequency.

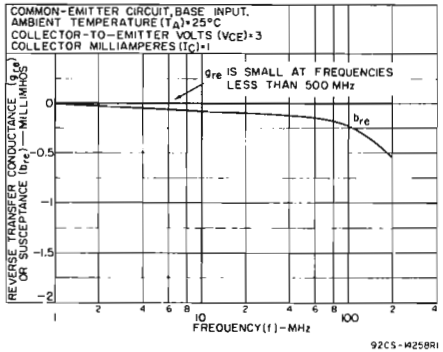


Fig.14 - Typical reverse transfer admittance vs frequency.

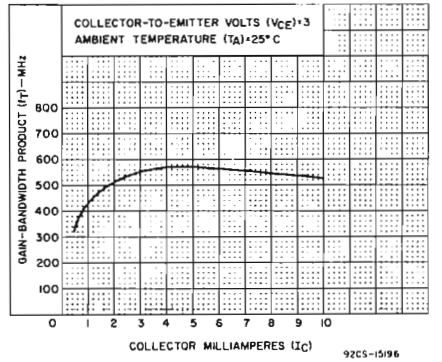


Fig.15 - Typical gain-bandwidth product vs collector current.

RCA
Solid State
Division

Linear Integrated Circuits

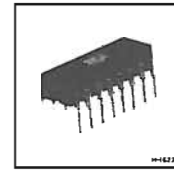
CA3048

Amplifier Array

Monolithic Silicon

FOUR INDEPENDENT AC AMPLIFIERS

For Low-Noise and General AC Applications In Industrial Service



CA3048

The RCA CA3048 is a silicon monolithic integrated circuit consisting of four independent identical AC amplifiers which can operate from a single-ended power supply.

The amplifiers include internal DC bias and feedback to provide temperature-stabilized operation. They may be used in a wide variety of AC applications in which operational amplifiers have previously been used.

Each high gain amplifier has a high impedance non-inverting input, and a lower impedance inverting input for the application of feedback. Two power-supply terminals and two ground terminals are provided to reduce internal and external coupling between amplifiers.

The CA3048 is supplied in a 16-lead dual-in-line plastic package.

APPLICATIONS

- Multi-channel or cascade operation
- Low-level preamplifiers
- Equalizers
- Linear signal mixers
- Tone generators
- Multivibrators
- AC integrators

FEATURES

- Four AC amplifiers on a common substrate
- Independently accessible inputs and outputs
- Operates from single-ended supply

EACH AMPLIFIER

- Noise figure at 1 kHz ..... 2 dB typ.
- High voltage gain ..... 53 dB min.
- High input resistance ..... 90 kΩ typ.
- Undistorted output voltage ..... 2 V rms min.
- Output impedance ..... 1 kΩ typ.
- Open-loop bandwidth ..... 300 kHz typ.

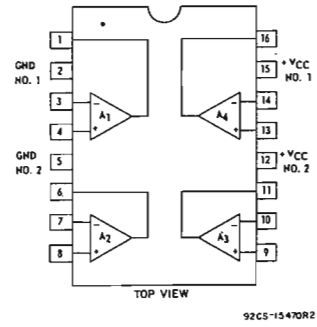


Fig.1 - Block diagram for CA3048.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:
- At T_A = 55°C . . . . . 750 mW
- Above T_A = 55°C. . . . . Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:
- Operating . . . . . -40°C to +85°C
- Storage . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ±0.79mm)
from case for 10 seconds max. . . . . +265°C

POWER SUPPLY VOLTAGE . . . . . +16 V
AC INPUT VOLTAGE . . . . . 0.5 V rms

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	-3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	-	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3048			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12V	3	9.5	13.5	17.5	mA	4,5
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12V	3	6.1	6.9	8.1	V	-
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12V	3	1.7	2.0	2.3	V	-
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12V	3	2.2	2.5	2.8	V	-
DYNAMIC (Characteristics given are for each amplifier with no AC feedback)								
Open-Loop Gain	A_{OL}	V_{CC} = +12V, E_{IN} = 2mV, f = 10kHz	6	53	58	-	dB	7,8
Output Voltage Swing	V_O(rms)	V_{CC} = +12V, f = 1kHz, THD = 5%	6	2.0	2.4	-	V	-
Open-Loop -3dB Bandwidth	BW	V_{CC} = +12V, E_{IN} = 2mV	6	250	300	-	kHz	9
Total Harmonic Distortion	THD	V_{CC} = +12V, f = 1kHz, E_{OUT} = 2V rms	6	-	0.65	-	%	10
Input Resistance	R_{IN}	OPEN LOOP Terminals 3, 7, 10, and 14 are by-passed to ground, f = 1kHz	-	-	90	-	kΩ	-
Input Capacitance	C_{IN}	f = 1MHz	-	-	9	-	pF	-
Output Resistance	R_{OUT}	Terminals 3, 7, 10 and 14 are by-passed to ground	-	-	1	-	kΩ	-
Output Capacitance	C_{OUT}	f = 1MHz	-	-	18	-	pF	-
Feedback Capacitance (Output to non-inverting input)	C_{FB}	V_{CC} = +12V, f = 1MHz	-	-	<0.1	-	pF	-
Broad-Band Output Noise Voltage	E_N	V_{CC} = +12V, R_S = 10kΩ, A = 40dB, Equivalent Noise BW = 50kHz	11	-	0.3	1	mV	-
Output Noise Voltage "Weighted"	$E_{N(WT)}$		12	-	0.5	2.2	mV	-
Noise Figure	NF (R_S = 5kΩ)	f = 10Hz	-	-	10	-	dB	-
		f = 100Hz	-	-	5.8	-	dB	
		f = 1kHz	-	-	2	-	dB	
		f = 10kHz	-	-	1.1	-	dB	
		f = 100kHz	-	-	0.6	-	dB	
Inter-Amplifier Audio Separation "Cross Talk"		V_{CC} = +12V, f = 1kHz, 0dB = 0.78V	13	-	<-45	-	dB	-
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12V, f = 1MHz	-	-	<0.02	-	pF	-

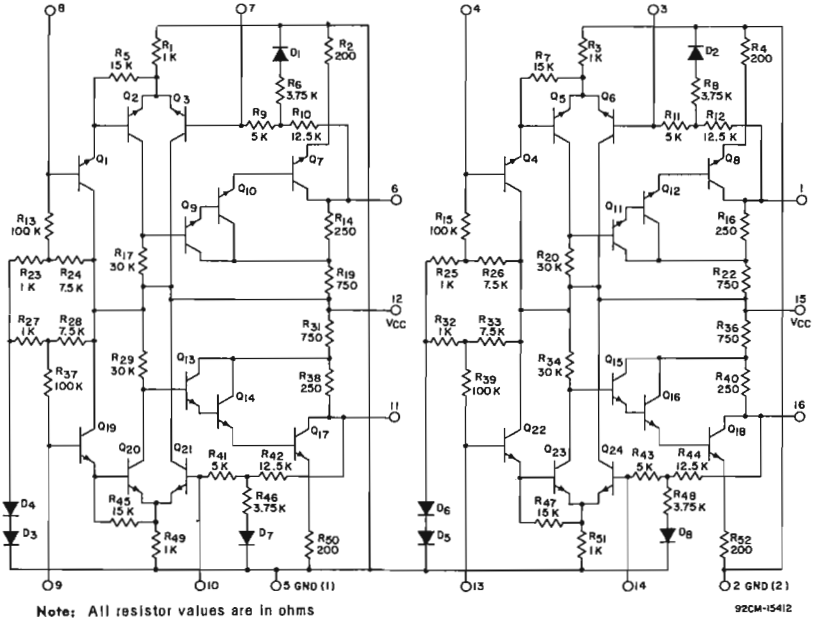


Fig.2 - Schematic diagram for CA3048.

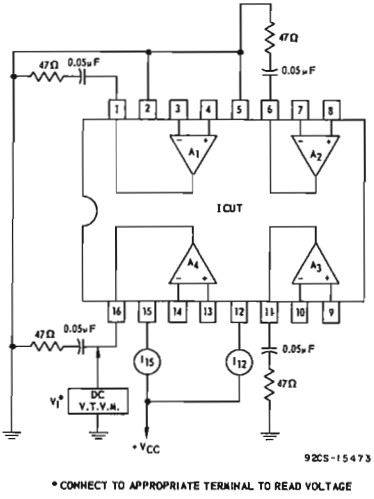


Fig.3 - Test circuit for measurement of collector supply voltage and currents.

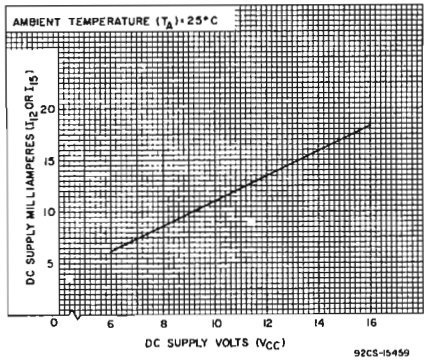


Fig.4 - Typical DC supply current vs supply voltage.

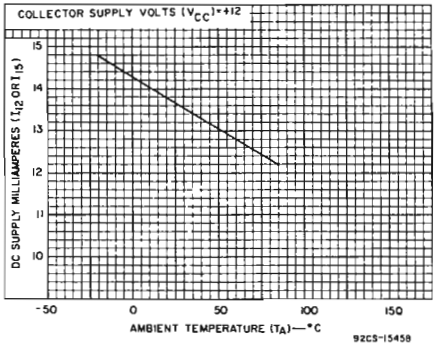


Fig.5 - Typical DC supply current vs ambient temperature.

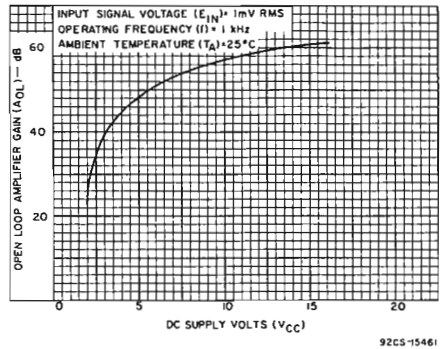
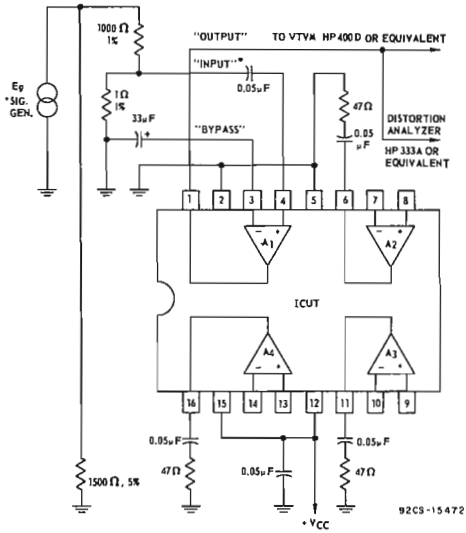


Fig.7 - Typical amplifier gain vs DC supply voltage.



* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make E_S = 2 mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.6 - Test circuit for measurement of distortion, open-loop gain and bandwidth characteristics.

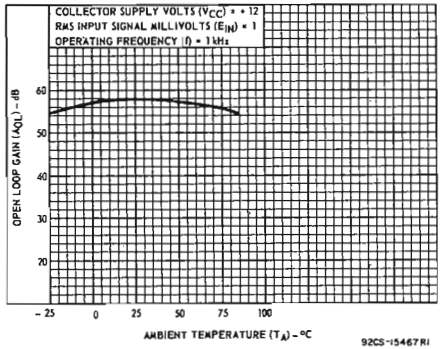


Fig.8 - Typical open-loop gain vs ambient temperature.

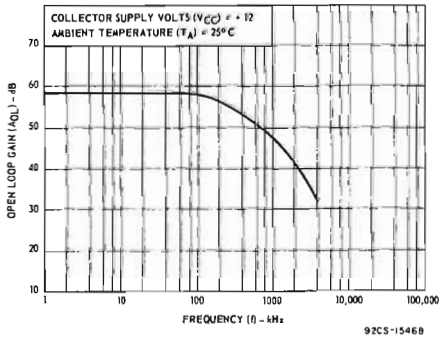


Fig.9 - Typical open-loop gain vs frequency.

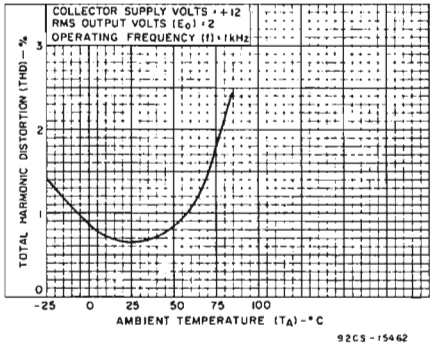
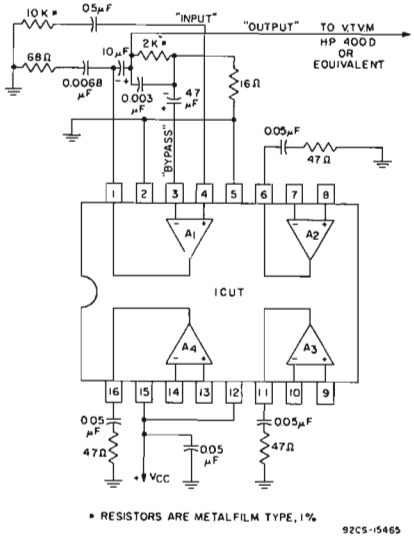


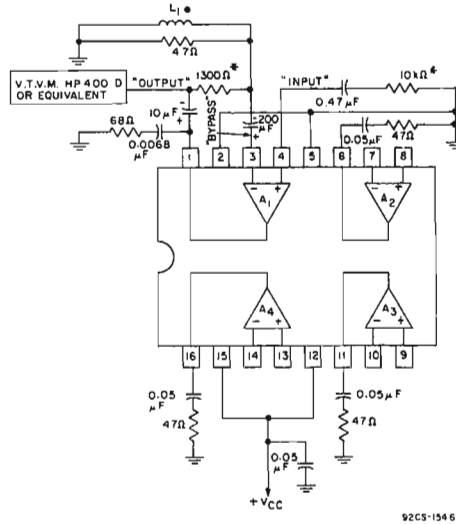
Fig.10 - Typical total harmonic distortion vs ambient temperature.



To test Amplifiers 1, 2, 3, or 4, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.11 - Test circuit for measurement of broadband noise characteristic.

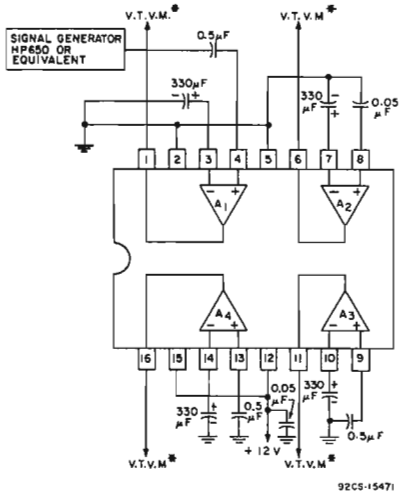


● L_1 - 2.5 millihenry inductor, dc resistance 0.3 ohms or less.

* Resistors metal film type, 1%. To test amplifiers, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.12 - Test circuit for measurement of "weighted" output noise voltage characteristic.



* V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig.13 - Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.

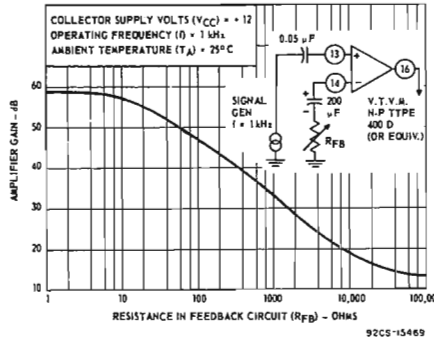


Fig.14 - Typical amplifier gain vs feedback resistance.

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3048 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig.14 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3048, as in other devices having high gain-bandwidth product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3048 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3049T CA3102E

14-Lead DIP
CA3102E

12-Lead TO-5

CA3049T

DUAL HIGH-FREQUENCY DIFFERENTIAL AMPLIFIERS

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- Power Gain 23 dB (typ.) at 200 MHz
- Noise Figure 4.6 dB (typ.) at 200 MHz
- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Full military-temperature-range capability- (−55°C to + 125°C) for the CA3102E and for the CA3049T

RCA-CA3049T and CA3102E* consist of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general-purpose devices which exhibit low I/f noise and a value of f_T in excess of 1 GHz. These features make the CA3049T and CA3102E useful from dc to 500 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

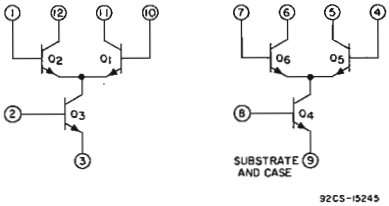
The monolithic construction of the CA3049T and CA3102E provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3102E is like the CA3049T except that it has a separate substrate connection for greater design flexibility. The CA3049T is supplied in the 12-lead TO-5 package; the CA3102E, in the 14-lead plastic dual-in-line package.

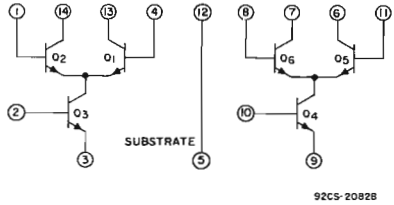
Applications

- VHF amplifiers
- VHF mixers
- Multifunction combinations — RF/Mixer/Oscillator; Converter/IF
- IF amplifiers (differential and/or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascade limiters
- Synchronous detectors
- Balanced mixers
- Synthesizers
- Balanced (push-pull) cascode amplifiers
- Sense amplifiers

*Formerly Developmental No. TA6228.



Schematic Diagram for CA3049T



Schematic Diagram for CA3102E

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIR-CUIT	CA3102E LIMITS			UNITS	TYPICAL CHARAC-TERISTICS CURVES
				FIG.	MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}			1	...	0.25	5	mV	-4
Input Offset Current	I_{IO}	$I_3 = I_9 = 2$ mA		1	...	0.3	3	μA	...
Input Bias Current	I_{IB}			1	...	13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$			1	...	1.1	...	μV/°C	4
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6$ V, $I_C = 1$ mA		...	674	774	874	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 6$ V, $I_C = 1$ mA		...	...	-0.9	...	mV/°C	6
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$		...	...	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$		...	15	24	...	V	...
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10$ μA, $I_E = 0$		...	20	60	...	V	...
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10$ μA, $I_B = 0$, $I_E = 0$		...	20	60	...	V	...
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10$ μA, $I_C = 0$		...	5	7	...	V	...
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor)	NF	f = 100 KH$_3$, $R_S = 500\ \Omega$ $I_C = 1$ mA		...	...	1.5	...	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 6$ V, $I_C = 5$ mA		...	...	1.35	...	GH$_z$	11
Collector-Base Capacitance	C_{CB}	$I_C = 0$	$V_{CB} = 5$V	*	...	0.28	...	pF	8
				**	...	0.15	...	pF	
Collector-Substrate Capacitance	C_{CI}	$I_C = 0$	$V_{CI} = 5$V		...	1.65	...	pF	8
For Each Differential Amplifier									
Common-Mode Rejection Ratio	CMR	$I_3 = I_9 = 2$ mA		...	...	100	...	dB	...
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	...	75	...	dB	...
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V f = 10 MHz		2	18	22	...	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	3	...	23	...	dB	...
Noise Figure	NF	$V_{CC} = 12$V	Cascode	3	...	4.6	...	dB	...
Input Admittance	Y_{11}	For Cascode Configuration $I_3 = I_9 = 2$ mA	Cascode	...	...	1.5 + j 2.45	...	mmho	14, 16, 18
			Diff.Amp.	...	...	0.878 + j 1.3	...		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration $I_3 = I_9 = 4$mA (each collector $I_C \simeq 2$mA)	Cascode	...	...	0 - j 0.008	...	mmho	...
			Diff.Amp.	...	...	0 - j 0.013	...		...
Forward Transfer Admittance	Y_{21}		Cascode	...	...	17.9 - j 30.7	...	mmho	26, 28, 30
			Diff. Amp.	...	...	- 10.5 + j 13	...		27, 29, 31
Output Admittance	Y_{22}		Cascode	...	...	- 0.503 - j 15	...	mmho	20, 22, 24
			Diff.Amp.	...	...	0.071 + j 0.62	...		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIR-CUIT	CA3049T LIMITS				TYPICAL CHARAC-TERISTICS CURVES
				FIG.	MIN.	TYP.	MAX.	UNITS	FIG.
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}			1	---	0.25	---	mV	-4
Input Offset Current	I_{IO}	$I_3 = I_9 = 2$ mA		1	---	0.3	---	µA	---
Input Bias Current	I_{IB}			1		13.5	33	µA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$			1	---	1.1	---	µV/°C	4
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6$ V, $I_C = 1$ mA		---	---	774	---	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 6$ V, $I_C = 1$ mA		---	---	-0.9	---	mV/°C	6
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$		---	---	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$		---	15	24	---	V	---
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10$ µA, $I_E = 0$		---	20	60	---	V	---
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10$ µA, $I_B = 0$, $I_E = 0$		---	20	60	---	V	---
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10$ µA, $I_C = 0$		---	5	7	---	V	---
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor)	NF	f = 100 KH$_3$, $R_S = 500\ \Omega$ $I_C = 1$ mA		---	---	1.5	---	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 6$ V, $I_C = 5$ mA		---	---	1.35	---	GH$_z$	11
Collector-Base Capacitance	C_{CB}	$I_C = 0$	$V_{CB} = 5$V	*	---	0.28	---	pF	8
				**	---	0.28	---	pF	
Collector-Substrate Capacitance	C_{CI}	$I_C = 0$	$V_{CI} = 5$V		---	1.65	---	pF	8
For Each Differential Amplifier									
Common-Mode Rejection Ratio	CMR	$I_3 = I_9 = 2$ mA		---	---	100	---	dB	---
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	---	75	---	dB	---
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V f = 10 MHz		2	---	22	---	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	3	---	23	---	dB	---
Noise Figure	NF	$V_{CC} = 12$V	Cascode	3	---	4.6		dB	---
Input Admittance	Y_{11}	For Cascode Configuration $I_3 = I_9 = 2$ mA	Cascode	---	---	1.5 + j 2.45	---	mmho	14, 16, 18
			Diff.Amp.	---	---	0.878 + j 1.3	---		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff Amplifier Configuration $I_3 = I_9 = 4$mA (each collector $I_C \simeq 2$mA)	Cascode	---	---	0 - j 0.008	---	mmho	---
			Diff.Amp.	---	---	0 - j 0.013	---		---
Forward Transfer Admittance	Y_{21}		Cascode	---	---	17.9 - j 30.7	---	mmho	26, 28, 30
			Diff. Amp.	---	---	- 10.5 + j 13	---		27, 29, 31
Output Admittance	Y_{22}		Cascode	---	---	- 0.503 - j 15	---	mmho	20, 22, 24
			Diff.Amp.	---	---	0.071 + j 0.62	---		21, 23, 26

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

MAXIMUM RATINGS, *ABSOLUTE-MAXIMUM VALUES, AT $T_A = 25°C$*

	CA3049T	CA3102E	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55°C$ Derate at:	5	6.67	mW/°C
Temperature Range:			
Operating	−55 to + 125	−55 to + 125	°C
Storage	−65 to + 150	−65 to + 150	°C

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C

The following ratings apply for each transistor in the devices

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049T and CA3102E is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

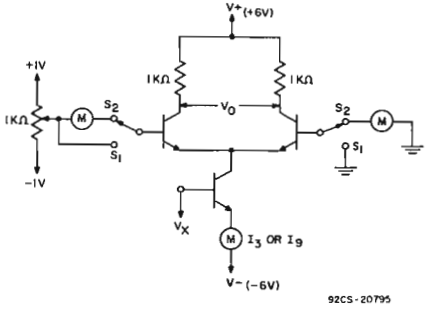


Fig. 1—Static characteristics test circuit for CA3102E.

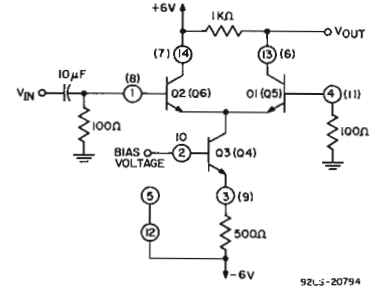
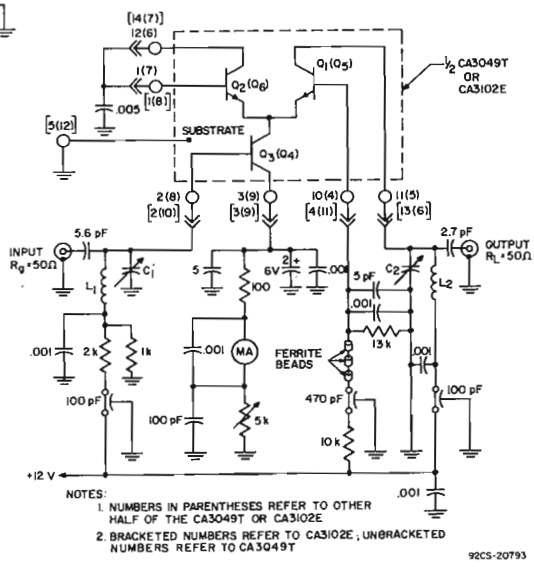


Fig. 2—AGC range and voltage gain test circuit for CA3102E.



L_1, L_2 – Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.
C_1, C_2 – 15 pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)
All Capacitors in μF Unless Otherwise Indicated
All Resistors in Ohms Unless Otherwise Indicated

Fig. 3—200 MHz cascode power gain and noise figure test circuit.

Typical Characteristics for CA3049T and CA3102E

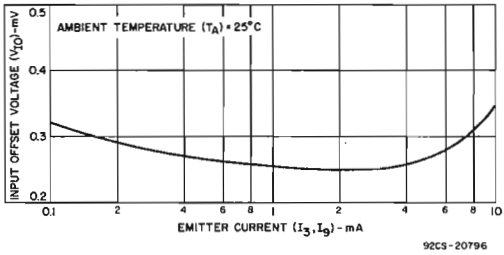


Fig. 4—Input offset voltage vs. emitter current.

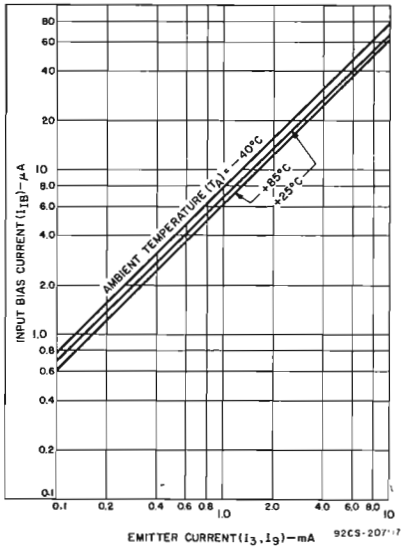


Fig. 5—Input bias current vs. emitter current.

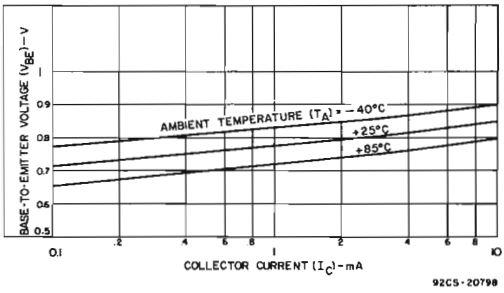


Fig. 6—Base-to-emitter voltage vs. collector current.

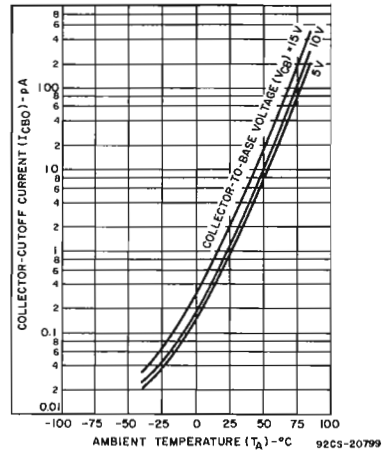


Fig. 7—Collector-cutoff current vs. temperature.

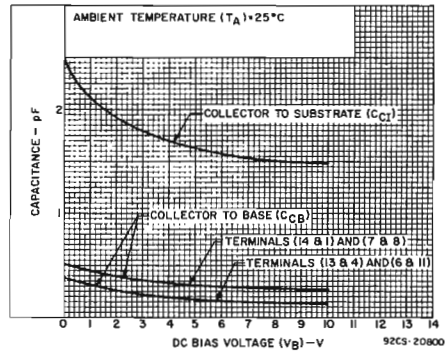


Fig. 8—Capacitance vs. dc bias voltage.

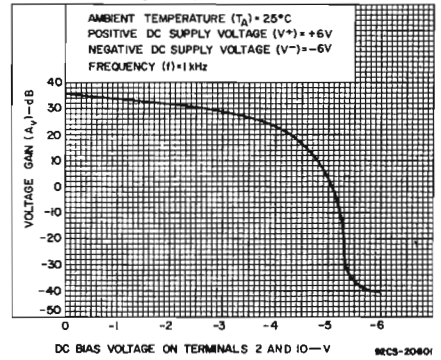


Fig. 9—Voltage gain vs. dc bias voltage.

Typical Characteristics for CA3049T and CA3102E (cont'd)

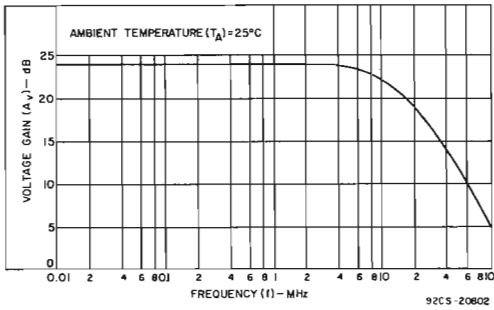


Fig. 10—Voltage gain vs. frequency.

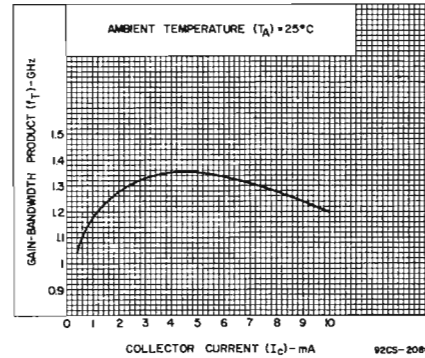


Fig. 11—Gain-bandwidth product vs. collector current.

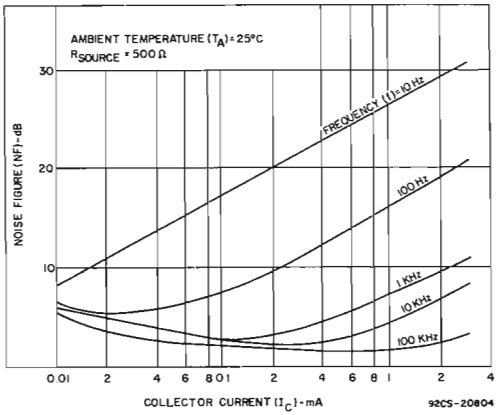


Fig. 12—1/f noise figure vs. collector current.

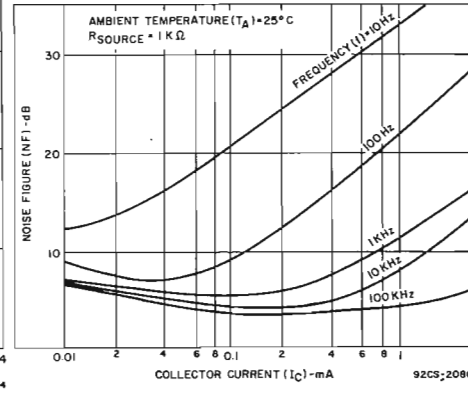


Fig. 13—1/f noise figure vs. collector current.

Typical Input Admittance Characteristics for CA3049T and CA3102E

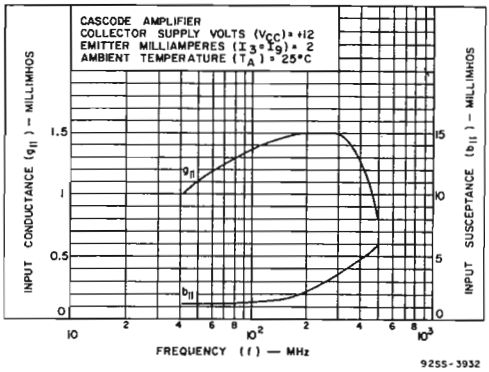


Fig. 14—Input admittance (Y_{11}) vs. frequency.

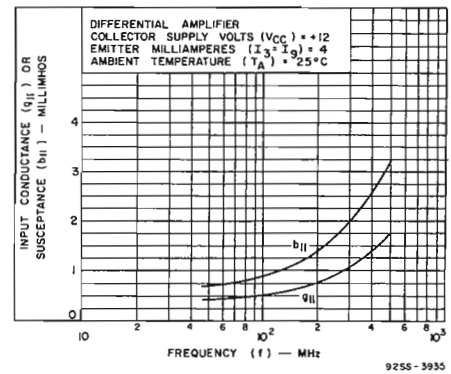


Fig. 15—Input admittance (Y_{11}) vs. frequency.

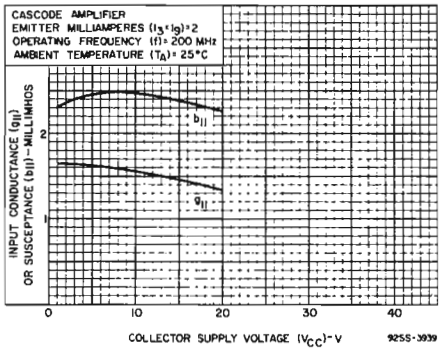


Fig. 16—Input admittance (Y_{11}) vs. collector supply voltage.

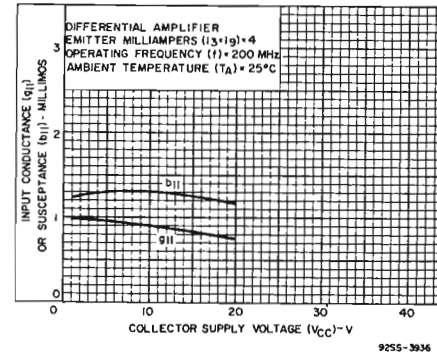


Fig. 17—Input admittance (Y_{11}) vs. collector supply voltage.

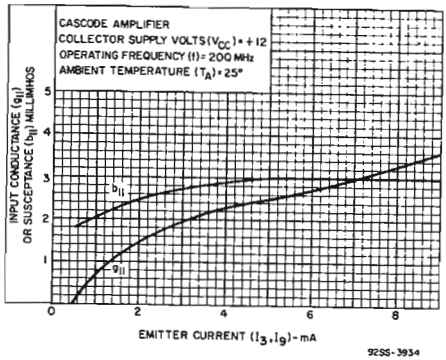


Fig. 18—Input admittance (Y_{11}) vs. emitter current.

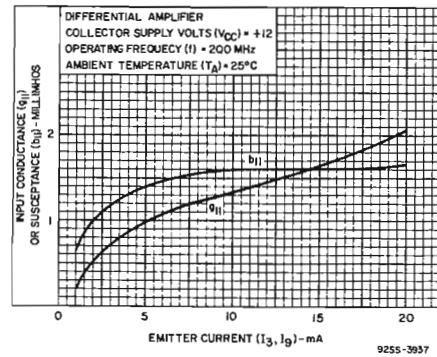


Fig. 19—Input admittance (Y_{11}) vs. emitter current.

Typical Output Admittance Characteristics for CA3049T and CA3102E

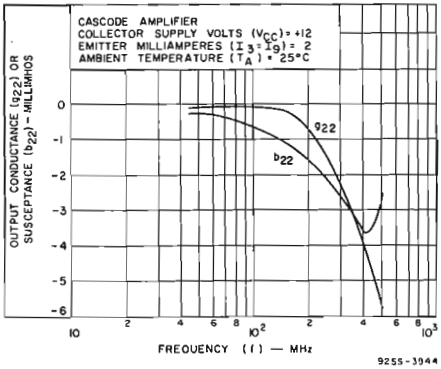


Fig. 20—Output admittance (Y_{22}) vs. frequency.

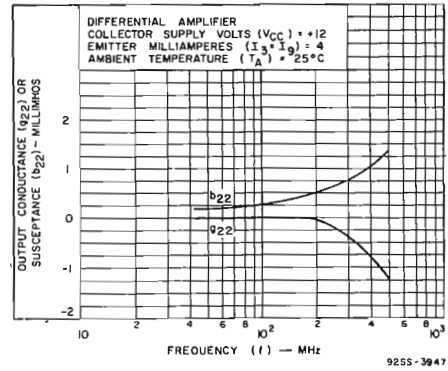


Fig. 21—Output admittance (Y_{22}) vs. frequency.

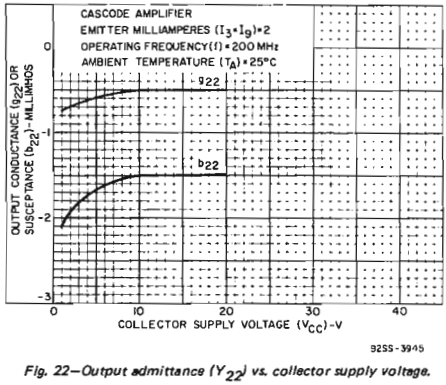


Fig. 22—Output admittance (Y_{22}) vs. collector supply voltage.

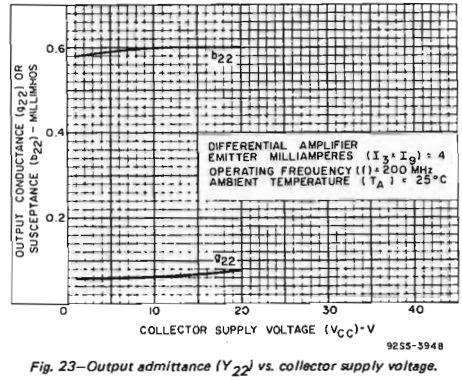


Fig. 23—Output admittance (Y_{22}) vs. collector supply voltage.

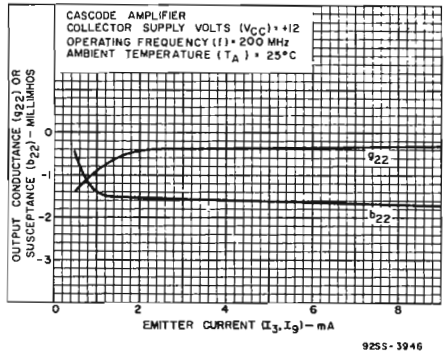


Fig. 24—Output admittance (Y_{22}) vs. emitter current.

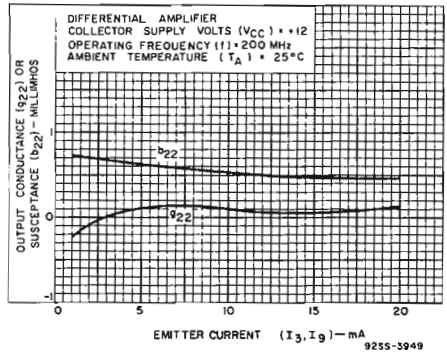


Fig. 25—Output admittance (Y_{22}) vs. emitter current.

Typical Forward Transfer Characteristics for CA3049T and CA3102E

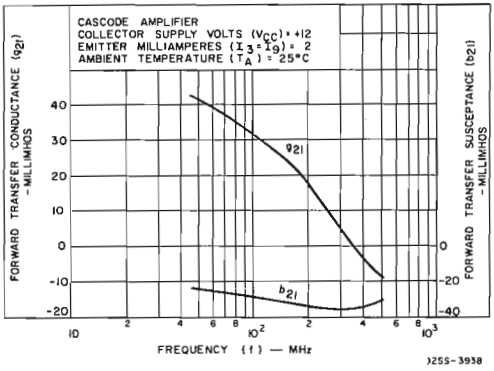


Fig. 26—Forward transfer admittance (Y_{21}) vs. frequency.

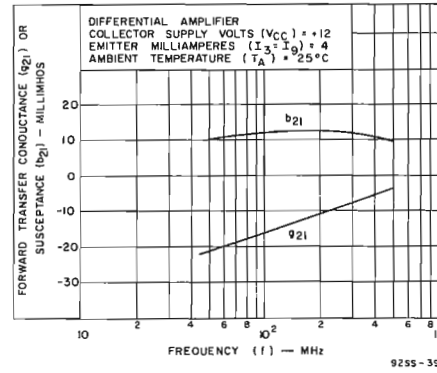


Fig. 27—Forward transfer admittance (Y_{21}) vs. frequency.

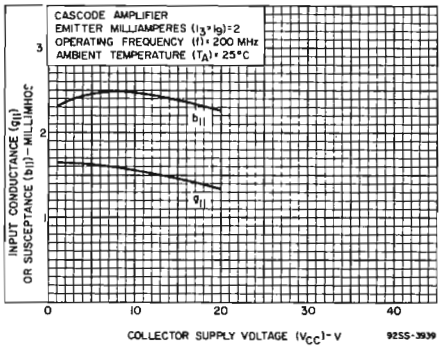


Fig. 28—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

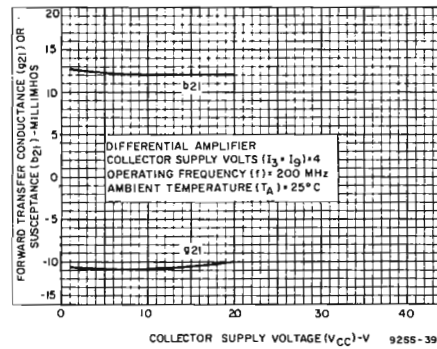


Fig. 29—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

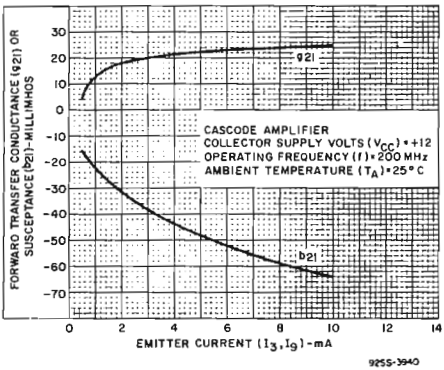


Fig. 30—Forward transfer admittance (Y_{21}) vs. emitter current.

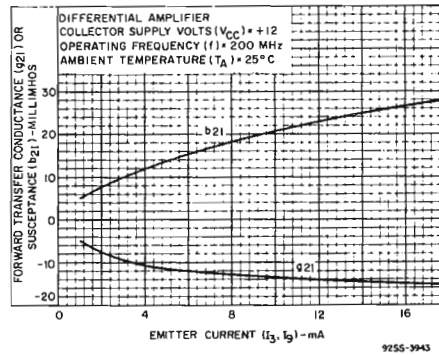


Fig. 31—Forward transfer admittance (Y_{21}) vs. emitter current.

RCA
Solid State
Division

Linear Integrated Circuits

CA3050
CA3051

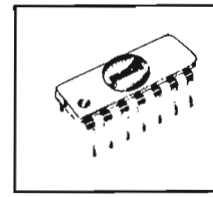
Dual Differential Amplifiers

Monolithic Silicon

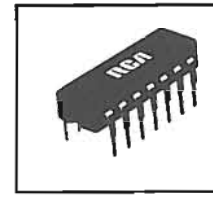
The CA3050 and CA3051 each consists of two differential amplifiers with associated constant current transistors on a common substrate. Each amplifier is driven by Darlington-connected emitter follower inputs to provide high input impedance, low bias current, and low offset current. A string of diodes is included to provide temperature-compensated bias to the constant current transistors and a low impedance bias point for the inputs to the differential amplifiers when a single power supply is used.

TWO DARLINGTON-CONNECTED DIFFERENTIAL AMPLIFIERS WITH DIODE BIAS STRING

For Low-Power Applications at Frequencies from DC to 20 MHz



CA3050 14-Lead Dual-in-Line Ceramic Package



CA3051 14-Lead Dual-in-Line Plastic Package

FEATURES

- Input offset current . . . . . 70 nA max.
- Input bias current . . . . . 500 nA max.
- Input offset voltage . . . . . 5 mV max.
- Input impedance . . . . . 460 kΩ typ.
- Independently accessible inputs and outputs

APPLICATIONS

- Matched dual amplifiers
- Dual sense amplifiers
- Dual Schmitt triggers
- Dual multivibrators
- Doubly balanced detectors and modulators
- Balanced quadrature detectors
- Synthesizer mixers
- Product detectors

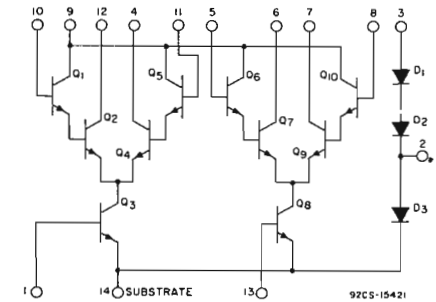


Fig.1 - Schematic diagram.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

	CA3050	CA3051	
Power Dissipation, P:			
Any one transistor	150	150	mW
Total package	900	750	mW
For T_A > 55°C, Derate at	8	6.67	mW/°C
Temperature Range:			
Operating	-55 to +125		°C
Storage	-65 to +150		°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265		°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3050 and CA3051 is isolated from the substrate by an integral diode. *The substrate (terminal 14) must be more negative than all collectors to maintain isolation between transistors and to provide for normal transistor action.*

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 3 is +5 to −2 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	—	*	*	*	*	*	*	*	*	*	*	*	*	+1 -5
2			+5 -2	*	*	*	*	*	*	*	*	*	*	+1 -1
3				*	*	*	*	*	*	*	*	*	*	+3 -1
4					*	*	*	*	*	+14 -2.5 Note 3	+14 -2.5 Note 4	*	*	+20 -1
5						+2.5 -14 Note 1	+2.5 -14 Note 1	+10 -10	+1 -20	*	*	*	*	+16 -1
6							*	+14 -2.5 Note 2	*	*	*	*	*	+20 -1
7								+14 -2.5 Note 2	*	*	*	*	*	+20 -1
8									+1 20	*	*	*	*	+16 -1
9										+20 -1	+20 -1	*	*	+20 -1
10											+10 -10	+2.5 -14 Note 3	*	+16 -1
11												+2.5 -14 Note 4	*	+16 -1
12														+20 -1
13														+1 -5
14														Ref. Substrate

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	0.1
2	50	50
3	50	1
4	50	1
5	5	0.1
6	50	1
7	50	1
8	5	0.1
9	50	1
10	5	0.1
11	5	0.1
12	50	1
13	5	0.1
14	100	5

NOTE 1: This rating is important only when terminal 5 is more positive than terminal 8.

NOTE 2: This rating is important only when terminal 8 is more positive than terminal 5.

NOTE 3: This rating is important only when terminal 10 is more positive than terminal 11.

NOTE 4: This rating is important only when terminal 11 is more positive than terminal 10.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIRCUIT FIG.	LIMITS CA3050/CA3051 MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC								
Amplifier Characteristics								
Input Offset Voltage	V_{IO}		–	–	1.5	5	mV	2a,b
Input Offset Current	I_{IO}		–	–	7	70	nA	3a,b
Input Bias Current	I_{IB}		–	–	200	500	nA	4a,b
Quiescent Operating Current Ratio	$\frac{(I_4+I_{12})}{I_3}$ or $\frac{(I_6+I_7)}{I_3}$	V_{CC} = + 6 V, I_3 = 2 mA	–	0.9	1.00	1.13	–	5a,b
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 50 μA	–	–	0.645	0.700	V	6
		V_{CE} = 3 V, I_C = 1 mA	–	–	0.725	0.800		
		V_{CE} = 3 V, I_C = 3 mA	–	–	0.760	0.850		
		V_{CE} = 3 V, I_C = 10 mA	–	–	0.805	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	–	–	-1.9	–	mV/°C	7
Transistor Characteristics								
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	0.002	100	nA	8
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V	–
DYNAMIC								
Transistor Characteristics								
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	–	–	0.78	–	pF	9
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	–	–	0.47	–	pF	9
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	–	–	1.92	–	pF	9
Amplifier Characteristics								
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 5 V, I_C = 3 mA	–	–	600	–	MHz	10
Forward Transadmittance (With single-ended input and output)	$\lvert y_{21} \rvert$	V_{CC} = 10 V, I_3 = 2 mA f = 1 MHz	11	7	9	11	mmho	11
Bandwidth at -3 dB Point	BW	V_{CC} = 10 V, I_3 = 2 mA	11	–	4.3	–	MHz	11
Input Impedance	Z_I	V_{CC} = 10 V, I_3 = 2 mA f = 1 KHz	12	–	460	–	kΩ	12
Output Impedance	Z_O	I_3 = 2 mA, f = 1 KHz	13	–	170	–	kΩ	13
Common-Mode Rejection Ratio	CMR	I_3 = 2 mA, f = 1 KHz	–	–	65	–	dB	–
AGC Range	AGC	I_3 = 2 mA, f = 1 KHz Terminal No.3 Grounded	11	–	60	–	dB	–

TYPICAL STATIC CHARACTERISTICS

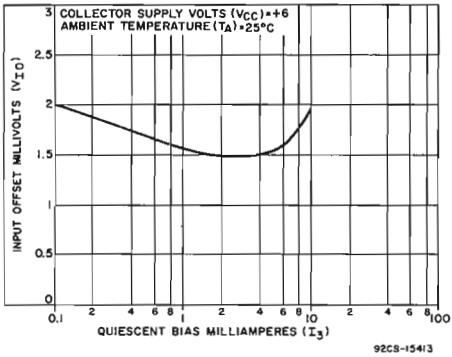


Fig.2(a) - Typical input offset voltage vs quiescent bias current.

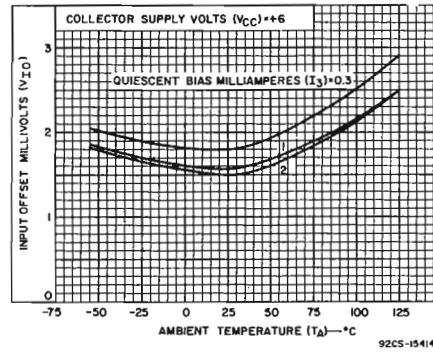


Fig.2(b) - Typical input offset voltage vs ambient temperature.

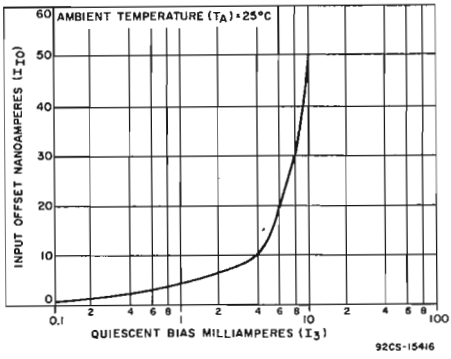


Fig.3(a) - Typical input offset current vs quiescent bias current.

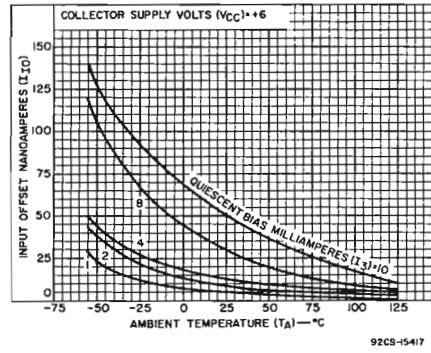


Fig.3(b) - Typical input offset current vs ambient temperature.

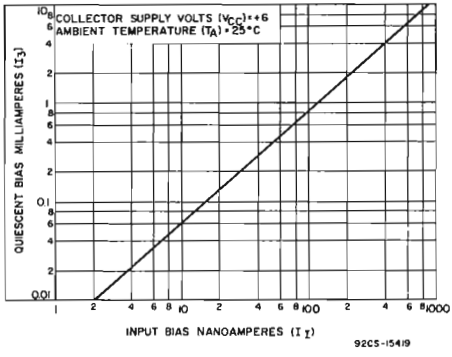


Fig.4(a) - Typical quiescent bias current vs input bias current.

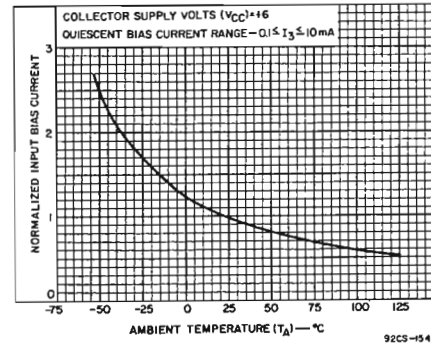


Fig.4(b) - Typical normalized input bias current vs ambient temperature.

STATIC CHARACTERISTICS

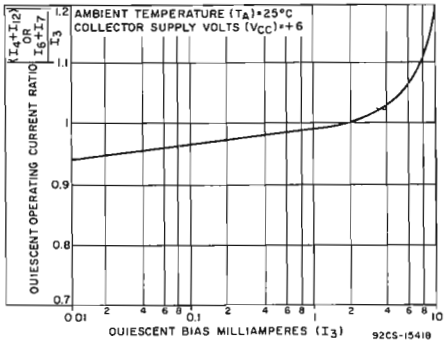


Fig.5(a) - Typical quiescent operating current ratio vs quiescent bias current.

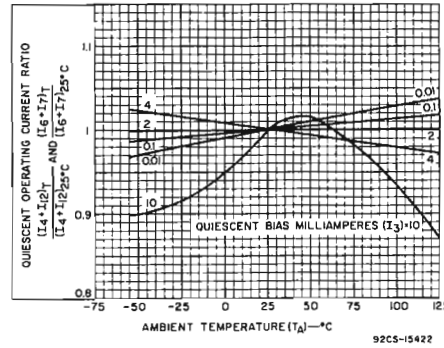


Fig.5(b) - Typical quiescent operating current ratio vs ambient temperature.

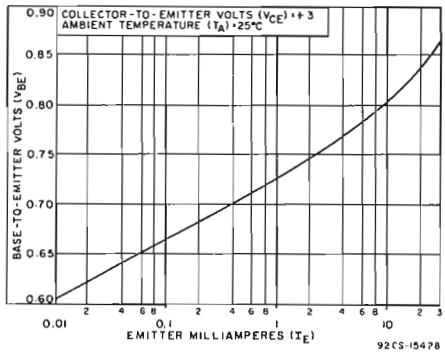


Fig.6 - Typical static base-to-emitter voltage characteristic vs emitter current for all transistors and forward diode voltage drops.

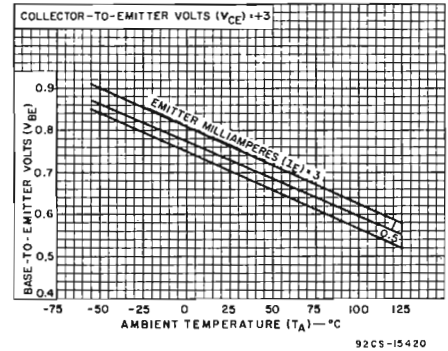


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

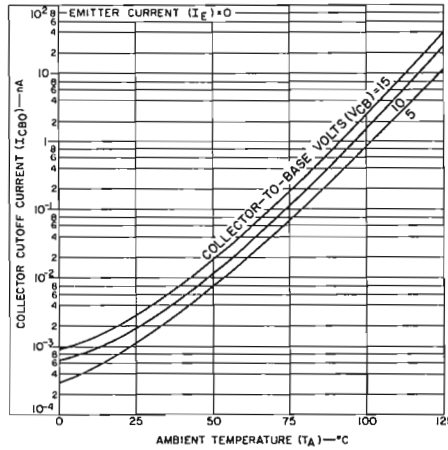


Fig.8 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

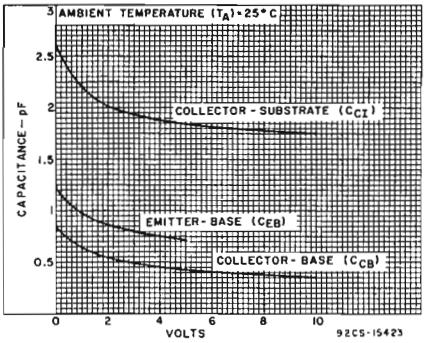


Fig.9 - Typical capacitance for each transistor.

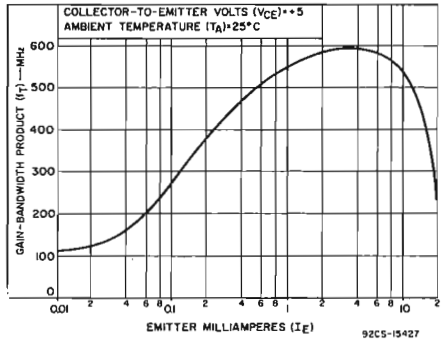


Fig.10 - Typical gain-bandwidth product (f_T) for each transistor vs emitter current.

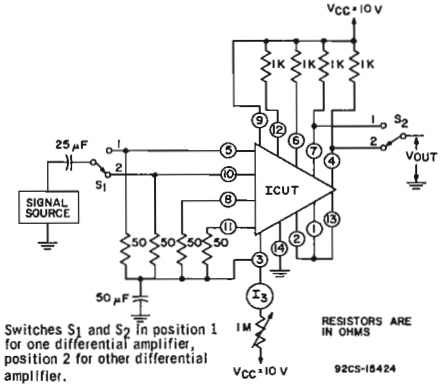


Fig.11(a) - Test circuit for forward transadmittance, -3 dB bandwidth, and AGC range.

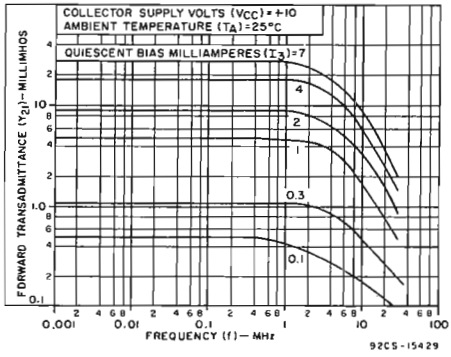


Fig.11(b) - Typical differential amplifier forward transadmittance with single-ended output vs frequency.

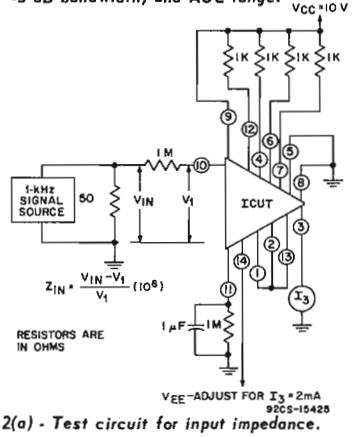


Fig.12(a) - Test circuit for input impedance.

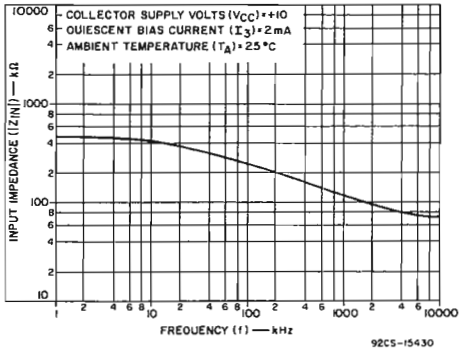
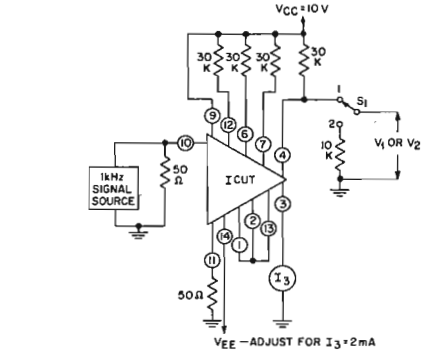


Fig.12(b) - Typical input impedance vs frequency with output short-circuited.

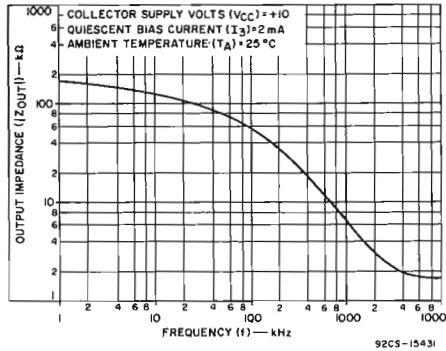
DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR



$$Z_{OUT} = \frac{(30K \times 10K)\frac{V_2}{V_1}}{\frac{V_2}{V_1}(30K+10K)-10K}$$

92CS-15426

Fig.13(a) - Test circuit for output impedance.



92CS-15431

Fig.13(b) - Typical output impedance vs frequency with input short-circuited.

RCA Solid State Division

Linear Integrated Circuits

CA3052

Special-Function Sub-System Stereo Preamplifier

The RCA CA3052 is a silicon monolithic integrated circuit designed specifically for stereo preamplifier service. The circuit consists of four independent AC amplifiers which can operate from a single-ended supply.

The CA3052 can operate as an equalizer amplifier in tape recorders, magnetic cartridge phonograph applications, and tone control amplifiers. The CA3052 can provide all of the amplification necessary for a full-function stereo preamplifier.

The CA3052 is supplied in a 16-lead dual-in-line plastic package.

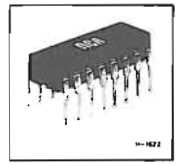
APPLICATIONS

- Full-function stereo preamplifiers
- Tape recorder and playback preamplifiers
- Tone Generators

RCA CA3048 Amplifier Array (File No.377) is schematically identical with the CA3052. Each amplifier of the CA3048 is tightly specified for equivalent output noise under a variety of test methods. The CA3052 is specified using RIAA test methods for equivalent input noise using one test method for amplifiers 1 and 4, and an appropriately different method for amplifiers 2 and 3.

FOUR INDEPENDENT AC AMPLIFIERS

For Stereo Preamplifiers, Magnetic Pickups, Tape Heads, etc.



CA3052

FEATURES

- Four AC amplifiers on a common substrate
- Independently accessible inputs and outputs
- Operates from single-ended supply

EACH AMPLIFIER

- High voltage gain . . . . . 53 dB min.
- High input resistance . . . . . 90 k Ω typ.
- Undistorted output voltage . . . . . 2 V rms min.
- Output Impedance . . . . . 1 kΩ typ.
- Open-loop bandwidth . . . . . 300 kHz typ.

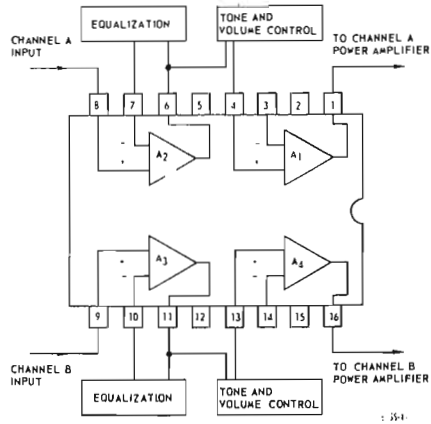


Fig.1 — Block diagram of stereo preamplifier using CA3052.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:

Up to T_A = 55°C . . . . . 750 mW
Above T_A = 55°C . . . . . Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:

Operating . . . . . −40°C to +85°C
Storage . . . . . −65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +255°C

POWER SUPPLY VOLTAGE . . . . . +16 V

AC INPUT VOLTAGE . . . . . 0.5 V rms

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 −16	*
2			*	+2 −3.6	0	*	*	+2 −3.6	+2 −3.6	*	*	+16 0	+2 −3.6	*	+16 0	0 −16
3				+5 −5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 −2	*	*	*	*	*	*	*	*	*	*	*
5						0 −16	*	+2 −3.6	+2 −3.6	*	0 −16	+16 0	+2 −3.6	*	+16 0	*
6							*	*	*	*	*	*	0 −16	*	*	*
7								+5 −5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 −5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 −16	*	*	*
13														+5 −5	*	*
14															*	*
15																+16 0
16																

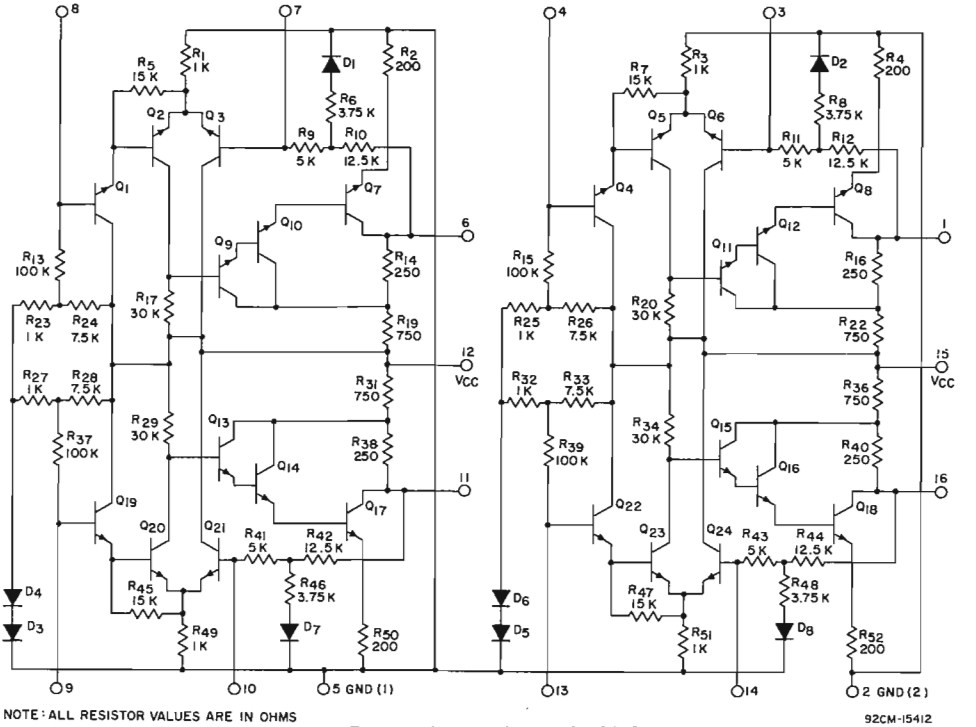
* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3052			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Current drain per amplifier pair	I_{12} or I_{15}	$V_{CC} = +12$ V	3	9.5	13.5	17.5	mA	4, 5
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	$V_{CC} = +12$ V	3	6.1	6.9	8.1	V	–
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	$V_{CC} = +12$ V	3	1.7	2.0	2.3	V	–
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	$V_{CC} = +12$ V	3	2.2	2.5	2.8	V	–
DYNAMIC each amplifier with no AC feedback unless otherwise noted–terminals 3, 7, 10, & 14 bypassed to ground								
Open-Loop Gain	A_{OL}	$V_{CC} = +12$ V $E_{IN} = 2$ mV $f = 10$ kHz	6	53	58	–	dB	7, 8
Open-Loop Output Voltage Swing	V_O(rms)	$V_{CC} = +12$ V $f = 1$ kHz THD = 5%	6	2.0	2.4	–	V	—
Open-Loop -3 dB Bandwidth	BW	$V_{CC} = +12$ V $E_{IN} = 2$ mV	6	–	300	–	kHz	9
Open-Loop Total Harmonic Distortion	THD	$V_{CC} = +12$ V, $f = 1$ kHz $E_{OUT} = 2$ V rms	6	–	0.65	–	%	10
Input Resistance	R_I	$V_{CC} = +12$ V, $f = 1$ kHz	–	–	90	–	kΩ	–
Input Capacitance	C_I	$V_{CC} = +12$ V, $f = 1$ MHz	–	–	9	–	pF	–
Output Resistance	R_O	$V_{CC} = +12$ V, $f = 1$ kHz	–	–	1	–	kΩ	–
Feedback Capacitance (Output to non-inverting Input)	C_{FB}	$V_{CC} = +12$ V $f = 1$ MHz	–	–	<0.1	–	pF	–
Equivalent Input Noise Voltage (Amplifiers 1 & 4), "C" Filter at Output*	E_{N1}‡	$V_{CC} = +10$ V $R_S = 5$ kΩ A = 45 dB	12	–	1.7	6.4	μV	–
Equivalent Input Noise Voltage (Amplifiers 2 & 3) RIAA Compensated*	E_{N2}‡	$V_{CC} = +10$ V $R_S = 5$ kΩ A = 64 dB (1 kHz)	11	–	4	15.0	μV	–
Inter-Amplifier Audio Separation "Cross Talk"		$V_{CC} = +12$ V $f = 1$ kHz 0 dB = 0.78 V	13	–	<-45	–	dB	–
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	$V_{CC} = +12$ V $f = 1$ MHz	–	–	< 0.02	–	pF	–

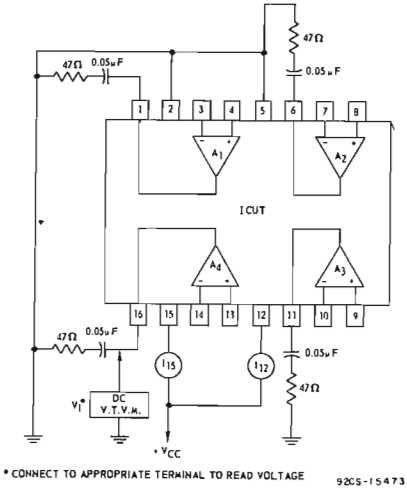
*Per IHF Standard Methods of Measurement for Audio Amplifiers IHF–A–201, 1966

‡ ac feedback included in test circuit



NOTE: ALL RESISTOR VALUES ARE IN OHMS

Fig. 2 - Schematic diagram for CA3052.



* CONNECT TO APPROPRIATE TERMINAL TO READ VOLTAGE

Fig. 3 - Test circuit for measurement of collector supply voltage and currents.

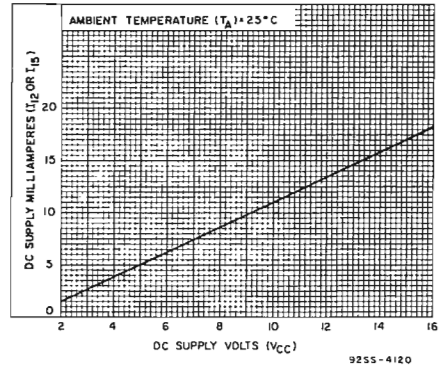


Fig. 4 - Typical DC supply current vs supply voltage.

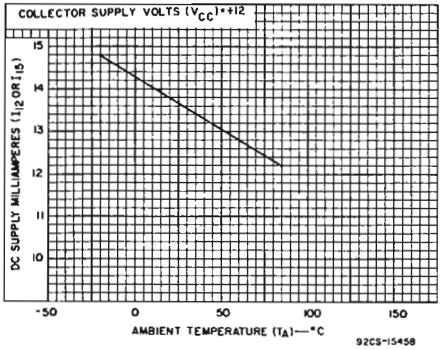


Fig. 5 - Typical DC supply current vs ambient temperature.

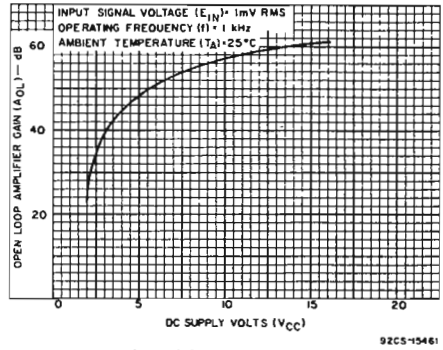
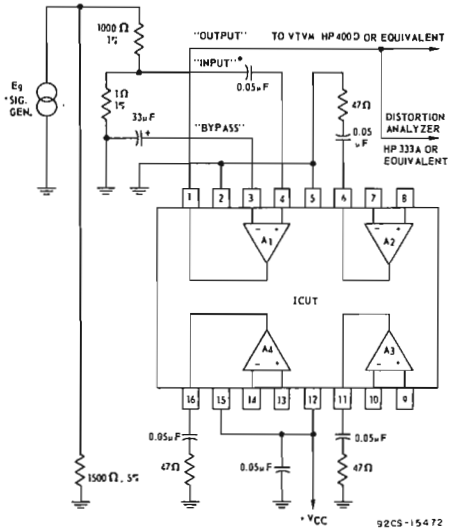


Fig. 7 - Typical amplifier gain vs DC supply voltage.



* Sig. Gen. should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make E_S = 2mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig. 6 - Test circuit for measurement of distortion, open-loop gain, and bandwidth characteristics.

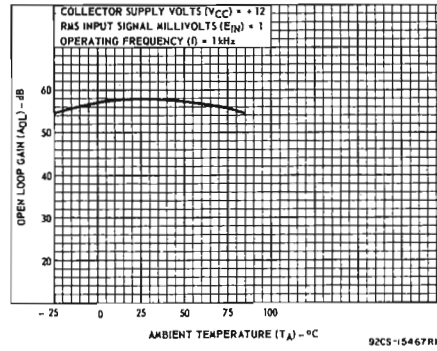


Fig. 8 - Typical open-loop gain vs ambient temperature.

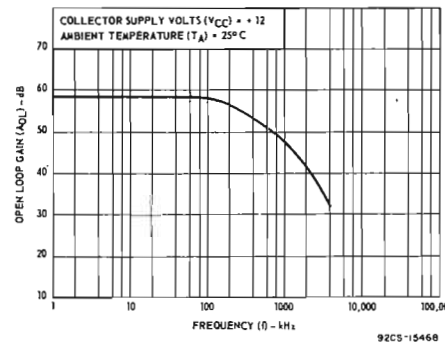


Fig. 9 - Typical open-loop gain vs frequency.

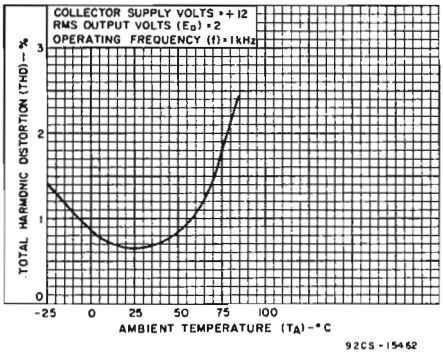
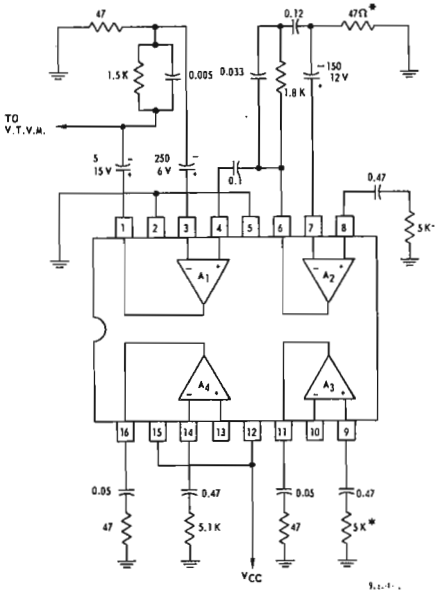
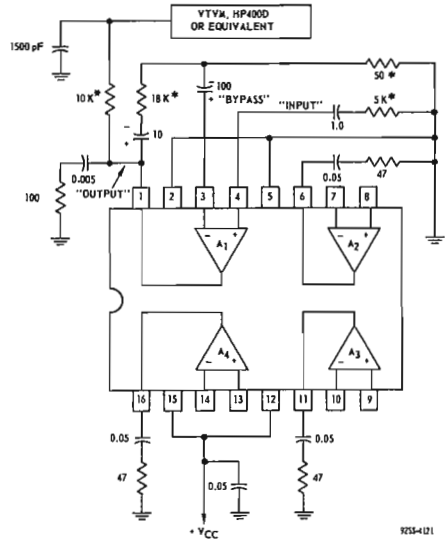


Fig. 10. - Typical total harmonic distortion vs ambient temperature.



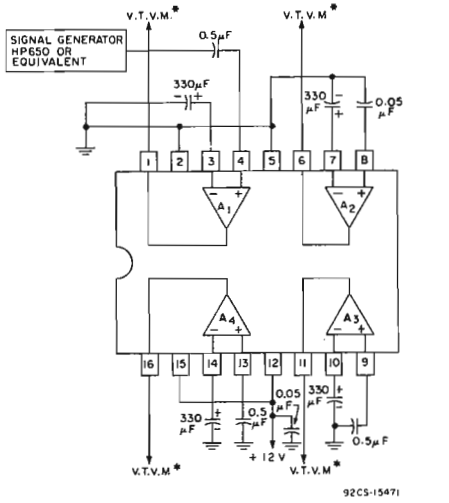
*Resistors are low noise precision (1%) Metal Film type.

Fig. 11 - Test circuit for equivalent input noise voltage measurement, RIAA compensated.



*Resistors are low noise precision, (1%) Metal Film type. Resistor values are in ohms; capacitance values are in microfarads, unless otherwise specified.

Fig. 12 - Test circuit for measurement of equivalent input noise voltage of amplifiers 1 and 4.

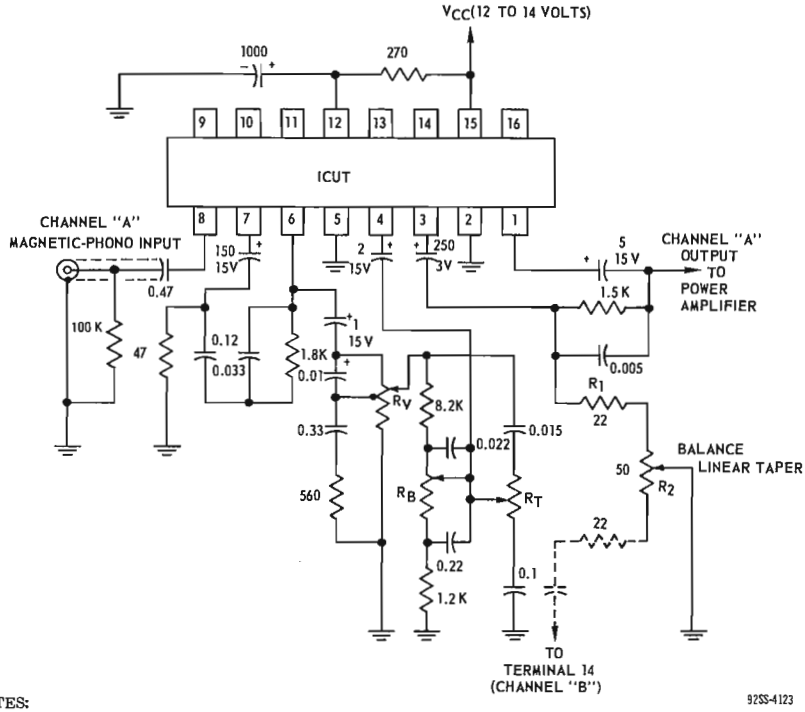


*V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig. 13 - Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.



NOTES:

1) Resistor values are in ohms, capacitance values are in microfarads, unless otherwise specified.
2) R_1 and R_2 resistor values are selected for a sensitivity of 3 mV input at 1 kHz.
3) R_V, volume control potentiometer, 15000 ohms tap at 6000 ohms with logarithmic taper*
4) R_B, bass control potentiometer, 25000 ohms.
5) R_T, treble control potentiometer, 25000 ohms.

Fig. 14 - Typical magnetic phono pre-amplifier using CA3052.

*This control, (part No. 11782-JM, type Q-T4-2G) may be obtained by contacting CTS Asheville Inc., Mills Gap Rd., Skyland, N. C. 28872. Guide for potentiometer manufacturers refer to Buyers'.

Typical Performance Data/Channel For Stereo Preamplifier

Magnetic-Phono Input

Voltage Gain at f = 1 kHz . . . . . 47 dB

Noise and Hum:*
- Full volume . . . . . -60 dB below 40 W
- Zero volume . . . . . -80 dB below 40 W

Boost and Cut:
- Bass at f = 100 Hz . . . . . ± 10 dB
- Treble at f = 10 kHz . . . . . ± 10 dB

Channel Separation at f = 1 kHz . . . . . > 40 dB

Input Equalization, RIAA . . . . . ± 2 dB

*Measurement made with preamplifier connected to 40-watt Quasi-Complementary Symmetry audio amplifier circuit. For circuit details see RCA publication, Form No. 2L1111.

To construct channel B circuit, duplicate channel A component circuit values to the appropriate channel B terminal as shown in table.

Channel B Terminal No.	Channel A Terminal No.	Circuit Description
9	8	input
10	7	feedback
11	6	interstage output
13	4	interstage input
14	3	feedback
16	1	output

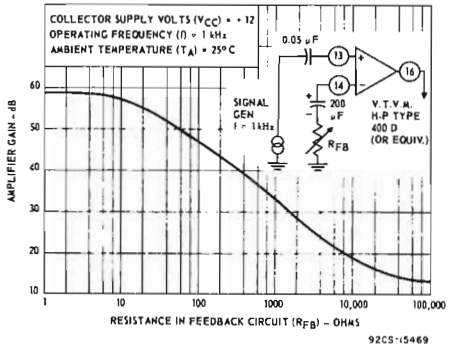


Fig. 15 - Typical amplifier gain vs feedback resistance

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3052 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig. 15 shows a curve of the gain of an amplifier when when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3052, as in other devices having high gain-band-width product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3052 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

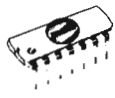
RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3058,CA3059,CA3079

CA3058



14-Lead Dual-In-Line Ceramic Package H-1553

CA3059
CA3079

14-Lead Dual-In-Line Plastic Package H-1517

Zero-Voltage Switches

For 50/60 and 400 Hz Thyristor Control Applications

Features	CA3058	CA3059	CA3079
■ 24V, 120V, 208/230V, 277V at 50 60, or 400 Hz operation	√	√	√
■ Differential Input	√	√	√
■ Low Balance Input Current (max.) -μA	1	1	2
■ Built-in Protection Circuit for opened or shorted sensor (Term. 14)	√	√	
■ Sensor Range (R_X) - kΩ	2 to 100	2 to 100	2 to 50
■ DC Mode (Term 12)	√	√	
■ External Trigger (Term. 6)	√	√	
■ External Inhibit (Term. 1)	√	√	
■ DC Supply Volts (max.)	14	14	10
■ Operating Temperature Range - °C	-55 to 125	-40 to 85	-40 to 85

RCA CA3058, CA3059, and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz. Each of the zero-voltage switches incorporates 4 functional blocks (See Fig. 2) as follows:

1. Limiter-Power Supply - - Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier - - Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector - - Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit - - Provides high-current pulses to the gate of the power controlling thyristor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (See Fig. 2):

1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

For an explanation of these functions see Operating Considerations, page 8. For detailed application information, see companion Application Note ICAN-6182, "Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)".

Applications

- Relay control ■ Heater control ■ Photosensitive control
- Valve control ■ Lamp control ■ Power one-shot control
- Synchronous switching of flashing lights
- On-off motor switching
- Differential comparator with self-contained power supply for industrial applications

MAXIMUM RATINGS, *Absolute Maximum Values, at* $T_A = 25^oC$

DC Supply Voltage (between Terms. 2 and 7):		
CA3058, CA3059	14	V
CA3079	10	V
DC Supply Voltage (between Terms. 2 and 8):		
CA3058, CA3059	14	V
CA3079	10	V
Peak Supply Current (Terms. 5 and 7)	±50	mA
Output Pulse Current (Term. 4)	150	mA
Power Dissipation:		
Up to T_A = 75°C - - CA3058	700	mW
Up to T_A = 55°C - - CA3059, CA3079	700	mW
Above T_A = 75°C - - CA3058	Derate Linearly 8	mW/°C
Above T_A = 55°C - CA3059, CA3079	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	-55 to +125	°C
Storage	-65 to +150	°C
Lead Temperature (During Soldering) At distance 1/16 ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

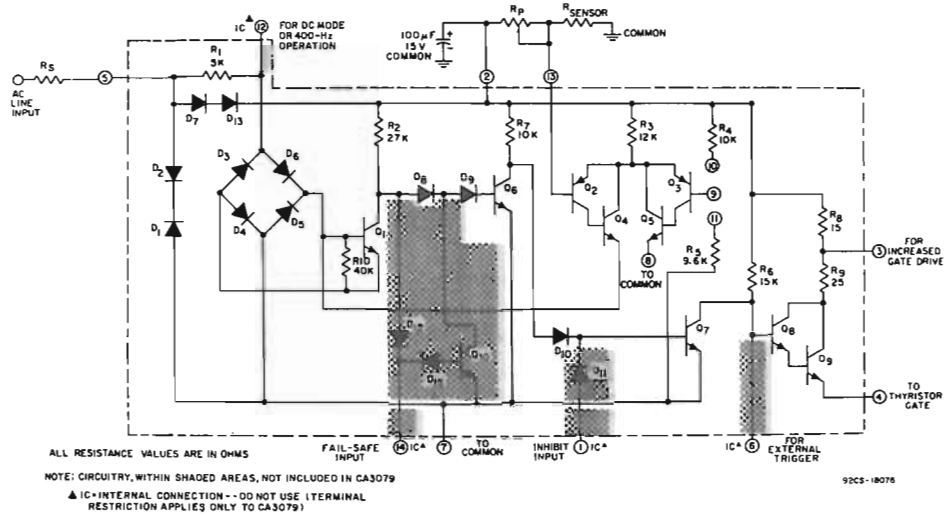


Fig.1—Schematic diagram of zero-voltage switches CA3058, CA3059 and CA3079. For functional block diagram see Fig. 2.

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL NO.	1 Note 3	2	3	4	5 Note 1	6 Note 3	7	8	9	10	11	12 Note 3	13	14 Note 2,3
1 Note 3		*	*	*	*	15 0	10 −2	*	*	*	*	*	*	*
2			0 −15	0 −15	2 −14	0 −14	0 ▲ −14	0 ▲ −14	0 −14	0 −14	0 −14	* .	0 −14	0 −14
3				0 −15	*	*	*	*	*	*	*	*	*	*
4					*	2 −10	*	*	*	*	*	*	*	*
5 Note 1						*	7 −7	*	*	*	*	*	*	*
6 Note 3							14 0	*	*	*	*	*	*	*
7								*	14 0	*	20 0	2.5 −2.5	14 0	6 −6
8									10 0	*	*	*	*	*
9										*	*	*	*	*
10											*	*	*	*
11												*	*	*
12 Note 3													*	*
13														*
14 Note 3														

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to −10 volts.

Note 1 – Resistance should be inserted between Term. 5 and external supply or line voltage for limiting current into Term. 5 to less than 50 mA.

Note 2 – Resistance should be inserted between Term. 14 and external supply for limiting current into Term. 14 to less than 2mA.

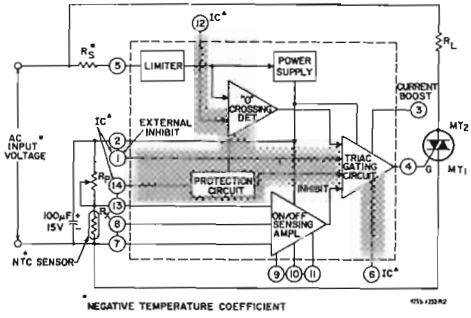
NOTE 3: For the CA3079 indicated terminal is internally connected and therefore, should not be used.

▲For CA3079 (0 to-10V)

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

MAXIMUM CURRENT RATINGS

I_{IN} mA	I_{OUT} mA
10	0.1
150	10
*	*
0.1	150
50	10
*	*
*	*
0.1	2
*	*
*	*
*	*
50	50
*	*
2	2



AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE:

Circuitry, within shaded areas, not included in CA3079

■ See chart above

▲ IC = Internal Connection -- DO NOT USE (Terminal Restriction applies only to CA3079).

Fig.2—Functional block diagrams of the zero-voltage switches CA3058, CA3059 and CA3079. For schematic diagram see Fig. 1.

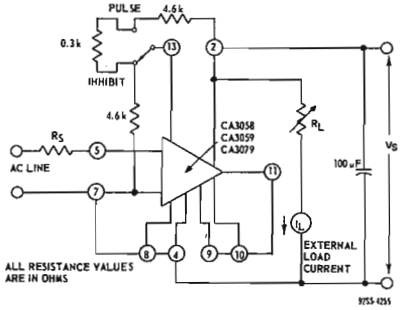


Fig.3a—DC supply voltage test circuit for CA3058, CA3059 and CA3079.

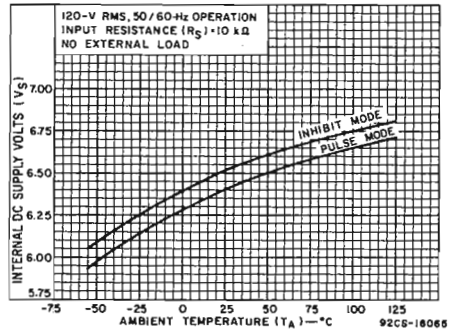


Fig.3b—DC supply voltage vs. T_A for CA3058, CA3059 and CA3079.

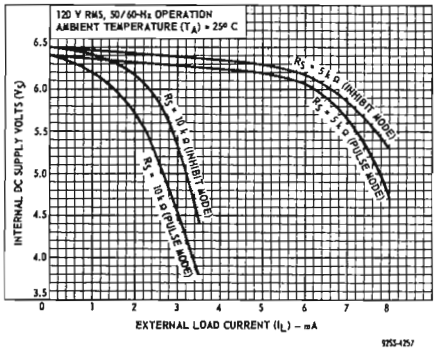


Fig.3c—DC supply voltage vs. external load current for CA3058, CA3059 and CA3079.

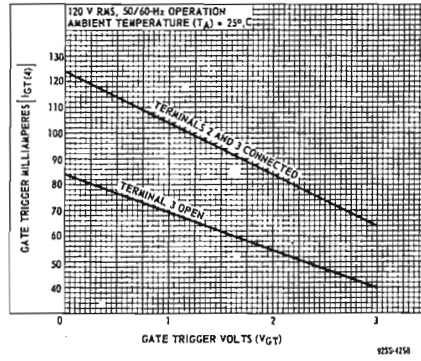


Fig.4—Gate trigger current vs. gate trigger voltage for CA3058, CA3059 and CA3079.

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
		CIRCUIT Fig. No.	T_A = 25°C (Unless Indicated Otherwise)	Typical Characteristics Curves Fig. No.	Min.	Typ.	Max.	
For Operating at 120V rms, 50-60 Hz (AC Line Voltage)•								
DC Supply Voltage: Inhibit Mode								
At 50/60 Hz	V_S	3a	R_S = 10 kΩ, I_L = 0	3b	6.1	6.5	7	V
At 400 Hz			R_S = 10 kΩ, I_L = 0	–	–	6.8	–	V
At 50/60 Hz			R_S = 5 kΩ, I_L = 2 mA	3c	–	6.4	–	V
Pulse Mode								
At 50/60 Hz			R_S = 10 kΩ, I_L = 0	3b	6	6.4	7	V
At 400 Hz			R_S = 10 kΩ, I_L = 0	–	–	6.7	–	V
At 50/60 Hz			R_S = 5 kΩ, I_L = 2 mA	3c	–	6.3	–	V
At 50/60 Hz (CA3058)			R_S = 10 kΩ, I_L = 0 T_A = -55 to 125°C	–	5.5	–	7.5	V
Gate Trigger Current	I_{GT}(4)	5a	Terms 3 and 2 connected, V_{GT}=1V	4	–	105	–	mA
Peak Output Current (Pulsed): With Internal Power Supply	I_{OM}(4)	5a	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	5b	50	84	–	mA
			Terms.3 and 2 connected, Gate Trigger Voltage (V_{GT}) = 0	5b	90	124	–	mA
With External Power Supply	I_{OM}(4)	6a	Term. 3 open, V^+ = 12V, V_{GT} = 0	6b, c	–	170	–	mA
			Terms 3 and 2 connected V^+ = 12V, V_{GT} = 0	6b, c	–	240	–	mA
Inhibit Input Ratio: All Types	V_9/V_2	7a	Voltage Ratio of Term. 9 to 2	7b	0.465	0.485	0.520	–
CA3058			T_A = -55 to 125°C		0.450	–	0.520	
Total Gate Pulse Duration:* For positive dv/dt								
50-60 Hz	t_P	8a	C_{EXT} = 0	8b	70	100	140	μs
400 Hz	t_P		C_{EXT} = 0, R_{EXT} = ∞	8d	–	12	–	μs
For negative dv/dt								
50-60 Hz	t_N	8a	C_{EXT} = 0	8b	70	100	140	μs
400 Hz	t_N		C_{EXT} = 0, R_{EXT} = ∞	8d	–	10	–	μs
Pulse Duration After Zero Crossing (50-60Hz):								
For positive dv/dt	t_{P1}	8a	C_{EXT} = 0 R_{EXT} = ∞	8c	–	50	–	μs
For negative dv/dt	t_{N1}	8a		8c	–	60	–	μs
Output Leakage Current Inhibit Mode:								
All Types	I_4	–		9	–	0.001	10	μA
CA3058			T_A = -55 to 125°C		–	–	20	μA
Input Bias Current:								
CA3058, CA3059,	I_{IB}	10			–	220	1000	nA
CA3079						220	2000	nA
Common-Mode Input Voltage Range	V_{CMR}		Terms. 9 and 13 connected		–	1.5 to 5	–	V
Sensitivity ≠ (Pulse Mode)	ΔV_{13}	5a	Term. 12 open	12	–	6	–	mV

≠Required voltage change at Term.13 to either turn OFF the triac when ON or turn ON the triac when OFF.

*Pulse duration in 50 Hz applications is approximately 15% longer than shown in Fig. 8b

•The values given in the Electrical Characteristics Chart at 120V also apply for operation at input voltages of 24V, 208/230V, and 277V , except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in Fig. 2, for the specified input voltage.

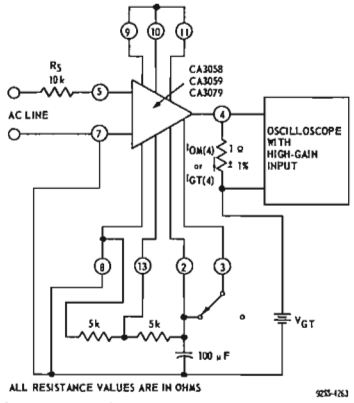


Fig.5a—Peak output (pulsed) and gate trigger current with internal power supply test circuit for CA3058, CA3059 and CA3079.

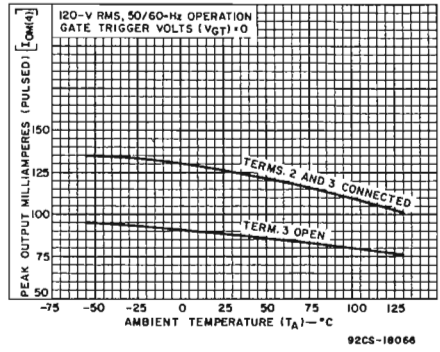


Fig.5b—I_{OM} vs. T_A for CA3058, CA3059 and CA3079.

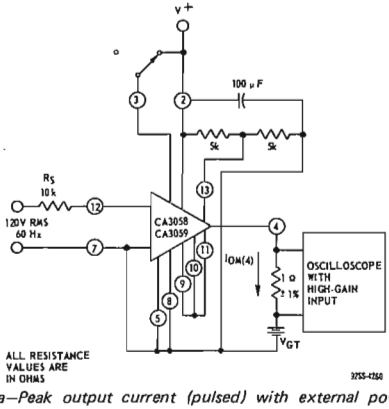


Fig.6a—Peak output current (pulsed) with external power supply test circuit for CA3058 and CA3059.

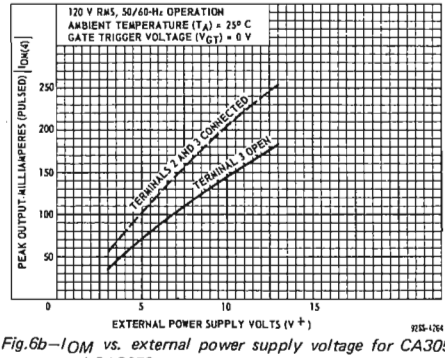


Fig.6b—I_{OM} vs. external power supply voltage for CA3058 and CA3059.

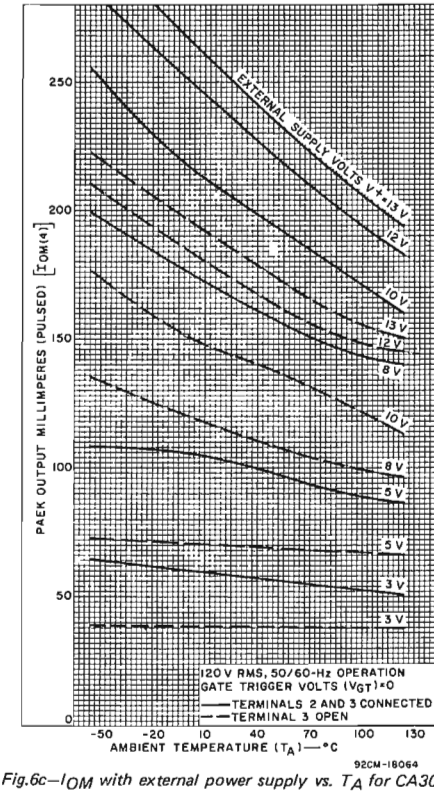


Fig.6c—I_{OM} with external power supply vs. T_A for CA3058 and CA3059.

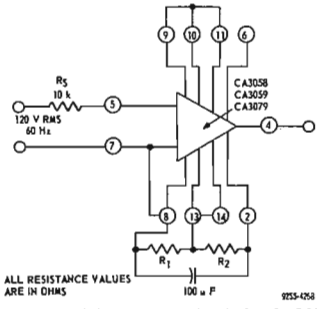


Fig.7a—Input inhibit ratio test circuit for CA3058, CA3059 and CA3079.

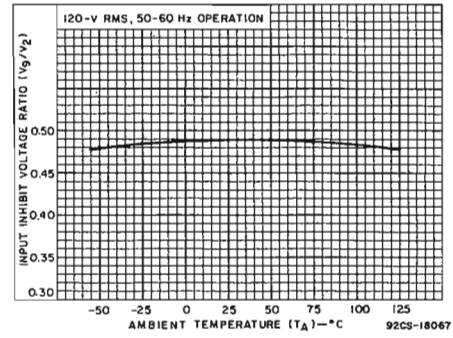


Fig.7b—Input inhibit voltage ratio vs. T_A for CA3058, CA3059 and CA3079.

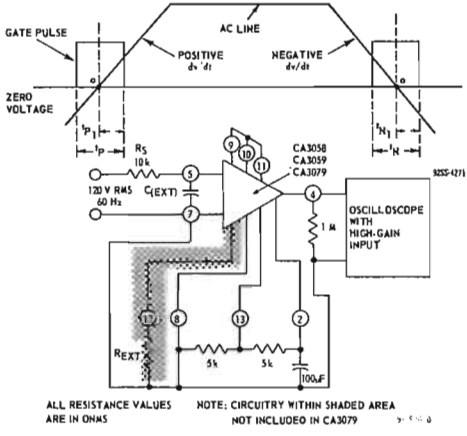


Fig.8a—Gate pulse duration test circuit with associated waveform for CA3058, CA3059 and CA3079.

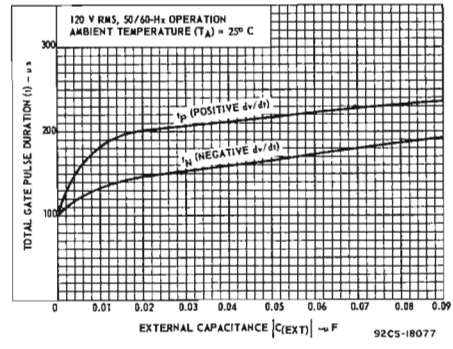


Fig.8b—Total gate pulse duration vs. external capacitance for CA3058, CA3059 and CA3079.

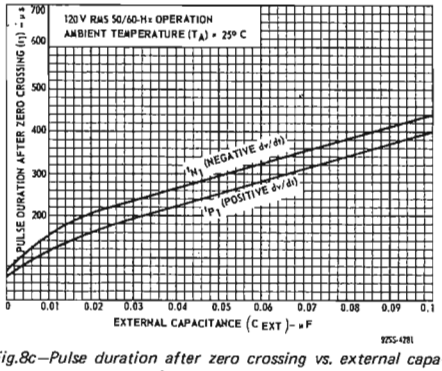


Fig.8c—Pulse duration after zero crossing vs. external capacitance for CA3058, CA3059 and CA3079.

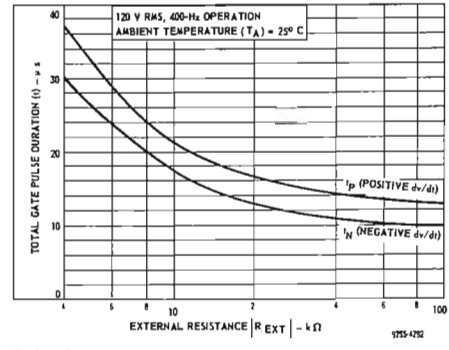


Fig.8d—Total gate pulse duration vs. external resistance for CA3058 and CA3059.

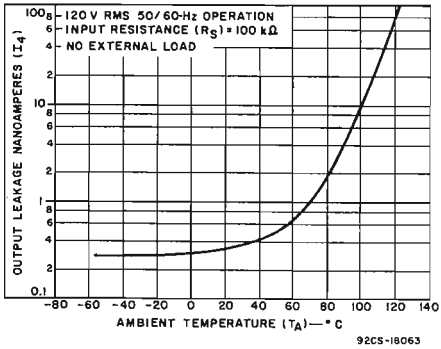


Fig.9—Output leakage current (inhibit mode) vs. T_A for CA3058, CA3059 and CA3079.

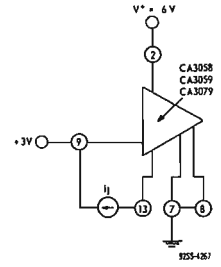
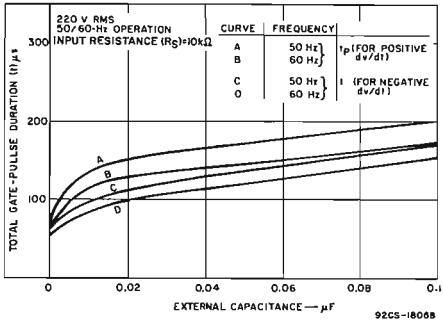
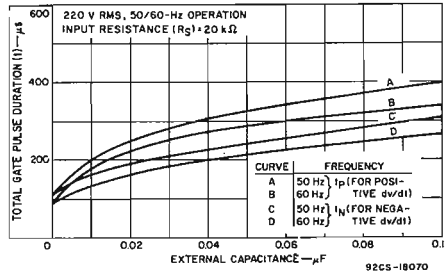
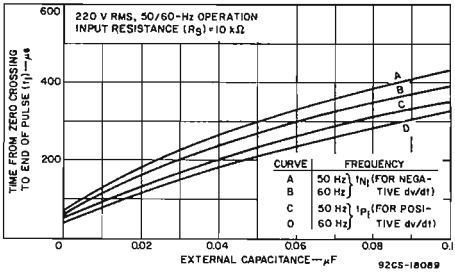


Fig.10—Input bias current test circuit for CA3058, CA3059 and CA3079.







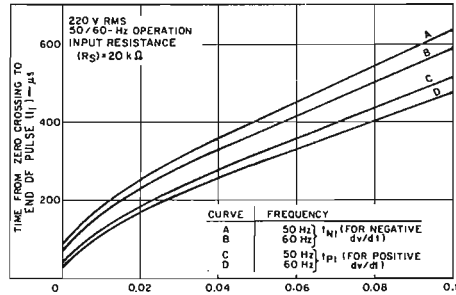


Fig.11—Relative pulse width and location of zero-voltage crossing for 220-volt operation for CA3058, CA3059 and CA3079.

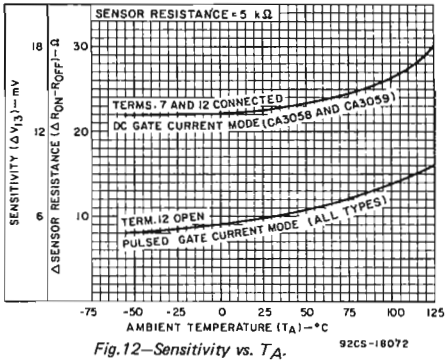


Fig.12—Sensitivity vs. T_A.

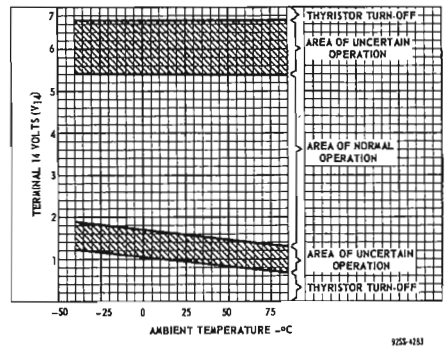


Fig.13—Operating regions for built-in protection circuit for CA3058 and CA3059.

OPERATING CONSIOERATIONS

Power Supply Considerations for CA3058, CA3059 and CA3079

The CA3058, CA3059 and CA3079 are intended for operetion as self-powered circuits with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for soma current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figs. 3b and 3c.

Power Supply Considerations for CA3058 and CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Fig. 5 for the peak output current characteristics). When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Fig. 5a.

Operation of Built-in Protection for the CA3058, CA3059

A special feature of the CA3058 and CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in Fig. 2. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2mA with a 5k Ω dropping resistor.
2. Set the value of Rp and sensor resistance (R_X) between 2k Ω and 100k Ω.
3. The ratio of R_X to Rp, typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series of shunt resistor must be added to avoid undesired activation of the circuit.

If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Fig. 13.

External Inhibit Function for the CA3058 and CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least + 1.2V at 10 μA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3058 and CA3059

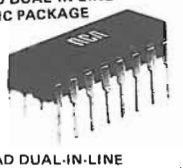
Connecting Terminals 7 and 12 disables the zero-crossing detector end permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be axercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.

Companion Application Notes, ICAN-6168 and ICAN-6268 provide detailed descriptions of the circuit operation and include many useful control epplications for the zero-voltage switches.

RCA
Solid State Division

Linear Integrated Circuits

CA3060AD CA3060BD CA3060D CA3060E



Operational Transconductance Amplifier Arrays

APPLICATIONS

- For low power conventional operational amplifier applications
- Active filters
- Comparators
- Gyrators
- Mixers
- Modulators
- Multiplexers
- Multipliers
- Strobing and gating functions
- Sample and hold functions

FEATURES

- Low power consumption -- as low as 100 μW per amplifier
- Independent biasing for each amplifier
- High forward transconductance
- Programmable range of input characteristics
- Low input bias and input offset current
- High input and output impedance
- No effect on device under output short-circuit conditions
- Zener diode bias regulator

RCA-CA3060AD, CA3060BD, CA3060D, and CA3060E, monolithic integrated circuits, are arrays of three independent Operational Transconductance Amplifiers. This type of amplifier is a new circuit concept that has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance, $g_m R_L$). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filters.

The three amplifiers in the CA3060 family are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific applications. The electrical characteristics of each amplifier are a function of the amplifier bias current (I_{ABC}). This feature offers the system designer maximum flexibility with regard to output current capability, power consumption, slew rate, input resistance, input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant dc level between input and output of each amplifier also makes the CA3060 suitable for a variety of non-linear applications such as mixers, multipliers, and modulators.

In addition, the types in the CA3060 family incorporate a unique Zener diode regulator system that permits current regulation below supply voltages normally associated with such systems.

Generic applications of the OTA are described in ICAN-6668, Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers.

The CA3060AD, CA3060BD, and CA3060D are supplied in a hermetic 16-lead dual-in-line ceramic package which can be operated over the full military temperature range, -55°C to +125°C. The CA3060E is supplied in a 16-lead dual-in-line plastic package and is operational from -40°C to +85°C.

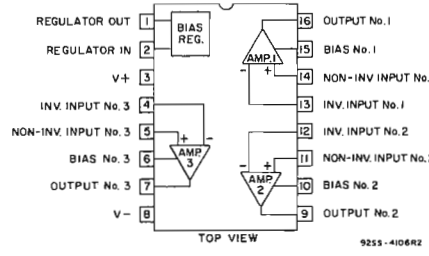


Fig. 1—Functional block diagram for each type in the CA3060 family.

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

DC Supply Voltage (between V^+ and V^- terminals):
CA3060AD, CA3060BD, CA3060E ..... 36V (±18V)
CA3060D ..... 14 V (±7V)

Differential Input Voltage (each amplifier):
CA3060AD, CA3060BD, CA3060E ..... ±5V
CA3060D ..... ±5V

DC Input Voltage ..... V^+ to V^-

Input Signal Current (each amplifier of each type): ..... ±1 mA

Amplifier Bias Current (each amplifier of each type) ..... 2 mA

Bias Regulator Input Current ..... -5 mA

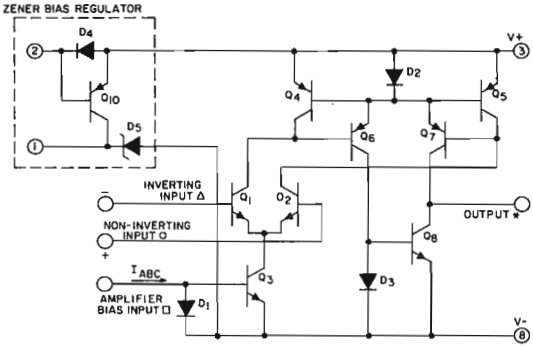
Output Short-Circuit Duration* ..... No limitation

Device Dissipation:
Total Package of each type up to T_A = 75°C ..... 490 mW
Above T_A = 75°C ..... Derate linearly 6.67 mW/°C

Temperature Range:
Operating –
CA3060AD, CA3060BD, CA3060D ..... -55 to +125°C
CA3060E ..... -40 to +85°C
Storage –
CA3060AD, CA3060BD, CA3060D,
CA3060E ..... -65 to +150°C

Lead Temperature (During Soldering):
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm)
from case for 10s max ..... +300°C

*Short circuit may be applied to ground or to either supply.



Δ INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 13, 12 AND 4, RESPECTIVELY
O NON-INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS TERMINAL Nos. 14, 11, AND 5, RESPECTIVELY
* OUTPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 16, 9, AND 7, RESPECTIVELY
□ AMPLIFIER BIAS CURRENT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 15, 10, AND 6, RESPECTIVELY

NOTE: A complete schematic diagram of the OTA is shown on Page 6. 92CS-15860RI

Fig.2—Simplified schematic diagram showing bias regulator and one operational transconductance amplifier for each type of the CA3060 family.

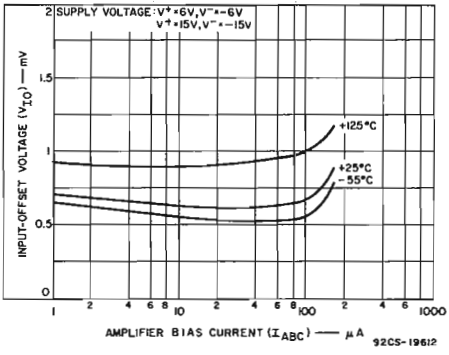


Fig.3—Input offset voltage vs. amplifier bias current.

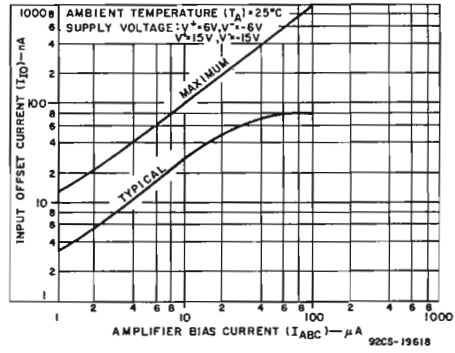


Fig.4—Input offset current vs. amplifier bias current.

ELECTRICAL CHARACTERISTICS (CA3060D)

For each amplifier at T_A = 25°C, V^+ = 6 V, V^- = -6 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVES Fig.	LIMITS									UNITS
			Amplifier Bias Current									
			I_{ABC} = 1 μA			I_{ABC} = 10 μA			I_{ABC} = 100 μA			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a, b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a, b	1.3	2.3	–	15	26	–	150	240	–	μA
Peak Output Voltage: Positive	V_{OM^+}	7	4.6	5	–	4.5	4.8	–	4.5	4.7	–	V
Negative	V_{OM^-}		6.8	5.95	–	5.8	5.95	–	5.7	6.9	–	
Amplifier Supply Current (each amplifier)	I_A	8a, b	–	8.5	14	–	85	120	–	850	1200	μA
Power Consumption (each amplifier)	P	–	–	0.10	0.17	–	1	1.45	–	10	14.5	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	–	–	1.5	120	–	2	120	–	2	120	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	20	120	–	20	120	–	30	120	
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a, b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–	4.4 to -5.1 min. 4.7 to -5.3 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			V
Slew Rate (Test ckt., Fig. 13	SR		–	0.1	–	–	1	–	–	8	–	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	–	20	–	–	45	–	–	110	–	kHz
Input Impedance Components:												
Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Capacitance at 1 MHz	C_I	–	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components:												
Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF

ZENER BIAS REGULATOR CHARACTERISTICS (at T_A = 25°C, I_Z = 0.1 mA)

				MIN.	TYP.	MAX.	
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C	6.2	6.7	7.9	V
Impedance	Z_Z	–			200	300	Ω

* Temperature-Coefficient; -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:

(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test —

V^+ is reduced to 5 volts for V^+ sensitivity

V^- is reduced to -5 volts for V^- sensitivity

(b) V^+ sensitivity in μV/V = $\frac{\text{Voffset - Voffset for +5 V and -6 V supplies}}{\text{1 volt}}$

V^- sensitivity in μV/V = $\frac{\text{Voffset - Voffset for -5 V and +6 V supplies}}{\text{1 volt}}$

ELECTRICAL CHARACTERISTICS (CA3060AD, CA3060BD, CA3060E)

For each amplifier at T_A = 25°C, V^+ = 15 V, V^- = -15 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVE Fig.	LIMITS Amplifier Bias Current I_{ABC} = 1 μA CA3060BD MIN.	TYP.	MAX.	I_{ABC} = 10 μA CA3060BD MIN.	TYP.	MAX.	I_{ABC} = 100 μA CA3060AD CA3060BD CA3060E MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a,b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a,b	1.3	2.3		15	26	–	150	240	–	μA
Peak Output Voltage: Positive	V_{OM^+}	7	12	13.6	–	12	13.6	–	12	13.6	–	V
Negative	V_{OM^-}		12	14.7	–	12	14.7	–	12	14.7	–	
Amplifier Supply Current (each amplifier)	I_A	8a,b	–	8.5	14	–	85	120	–	850	1200	μA
Power Consumption (each amplifier)	P	–	–	0.26	0.42	–	2.6	3.6	–	26	36	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	–	–	1.5	150	–	2	150	–	2	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	20	150	–	20	150	–	30	150	
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a,b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input Voltage Range	V_{ICR}	–	+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			V
Slew Rate (Test ckt., Fig. 13)	SR	–	–	0.1	–	–	1	–	–	8	–	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	–	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Capacitance at 1 MHz	C_I	–	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A=25°C, I_Z = 0.1 mA)						MIN.	TYP.	MAX.				
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z	–					200	300				Ω

* Temperature-Coefficient; -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:

(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test ---

V^+ is reduced to 13 volts for V^+ sensitivity

V^- is reduced to −13 volts for V^- sensitivity

(b) V^+ sensitivity in μV/V = $\frac{\text{Voffset - Voffset for +13 V and −15 V suppl}}{1 \text{ volt}}$

V^- sensitivity in μV/V = $\frac{\text{Voffset - Voffset for −13 V and +15 V suppl}}{1 \text{ volt}}$

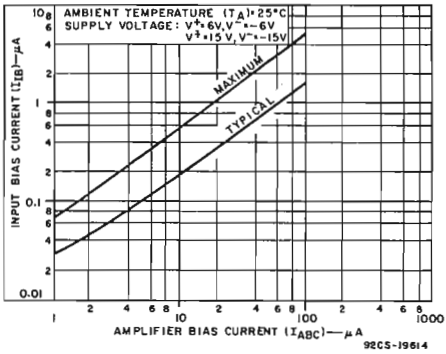


Fig.5a—Input bias current vs. amplifier bias current

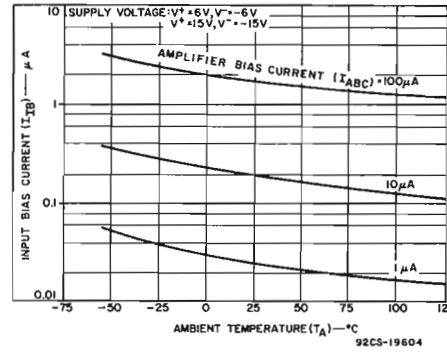


Fig.5b—Input bias current vs. ambient temperature.

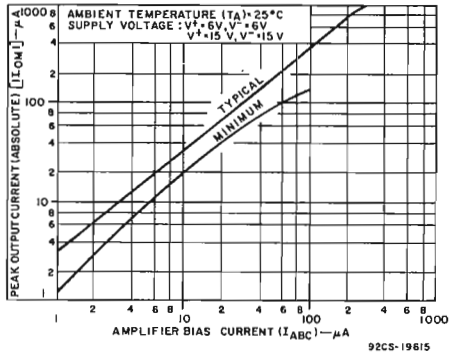


Fig.6a—Peak output current vs. amplifier bias current.

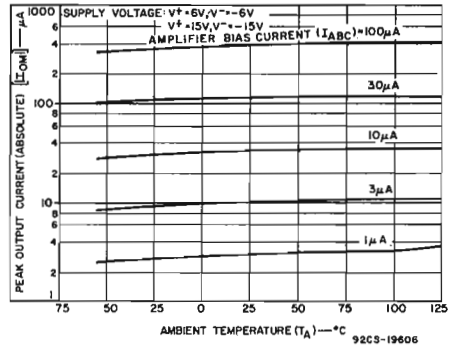


Fig.6b—Peak output current vs. ambient temperature.

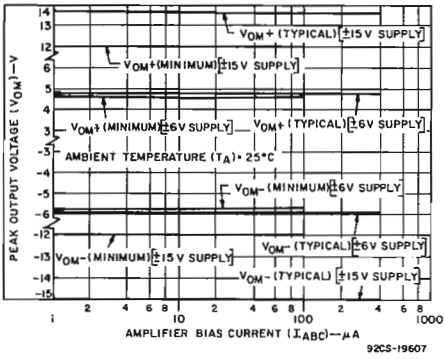


Fig.7—Peak output voltage vs. amplifier bias current.

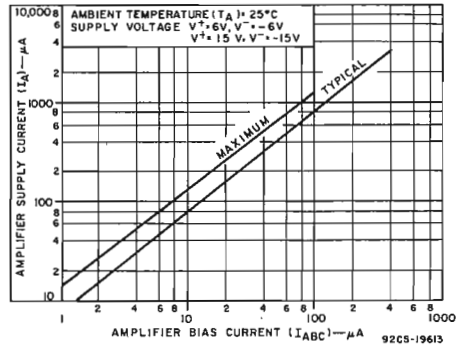


Fig.8a—Amplifier supply current (each amplifier) vs. amplifier bias current.

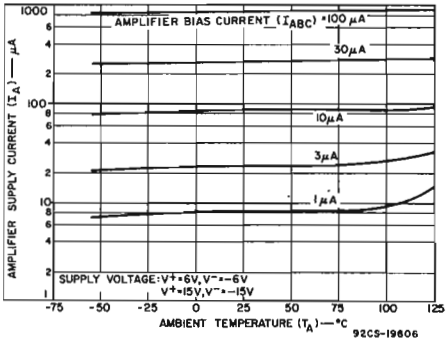


Fig.8b—Amplifier supply current (each amplifier) vs. ambient temperature.

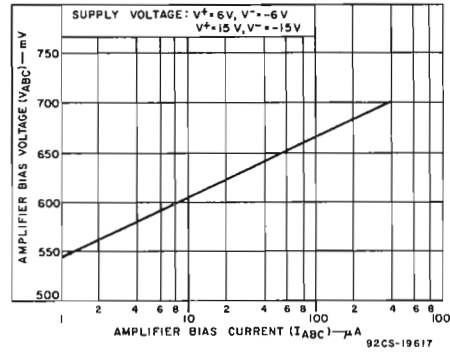


Fig.9—Amplifier bias voltage vs. amplifier bias current.

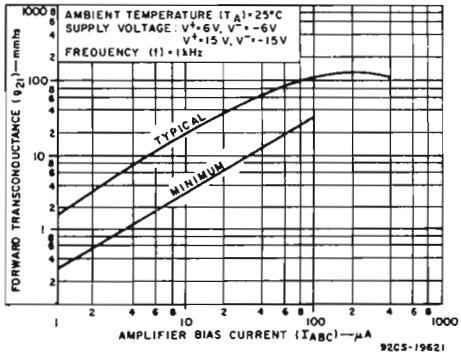


Fig.10a—Forward transconductance vs. amplifier bias current.

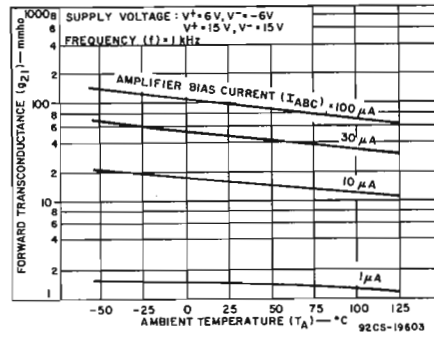


Fig.10b—Forward transconductance vs. ambient temperature.

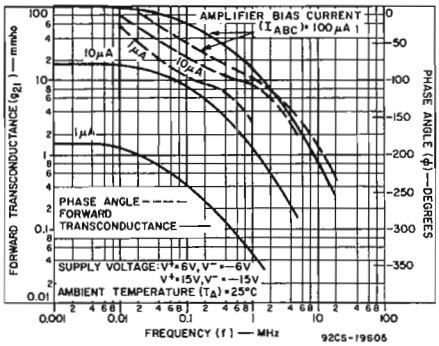


Fig.11—Forward transconductance vs. frequency.

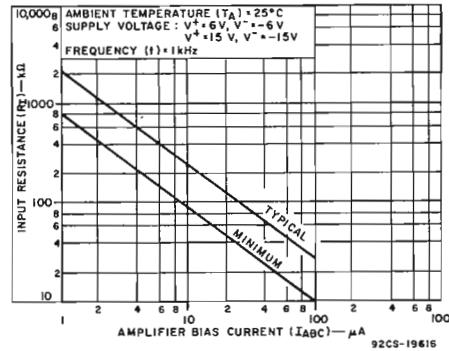
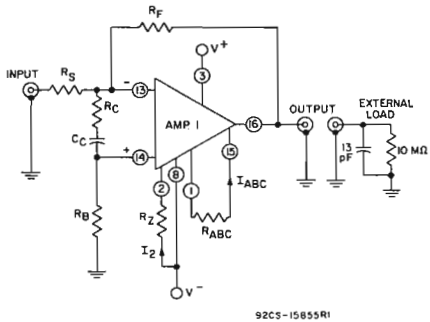


Fig.12—Input resistance vs. amplifier bias current.



V_Z is measured between terminals 1 and 8.

V_{ABC} is measured between terminals 15 and 8.

$$R_Z = \frac{[(V^+)-(V^-)-0.7]}{I_2}, \quad R_{ABC} = \frac{V_Z - V_{ABC}}{I_{ABC}}$$

Supply Voltage: for both ±6 V and ±15 V.

TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS

I_{ABC}	SLEW RATE	I_2	R_{ABC}	R_S	R_F	R_B	R_C	C_C
μA	V/μs	μA	ohms					μF
100	8	200	62 k	100k	100k	51k	100	0.02
10	1	200	620k	1M	1M	510k	1k	0.005
1	0.1	2	6.2M	10M	10M	5.1M	∞	0

Fig.13—Slew rate test circuit for amplifier No. 1 of CA3060.

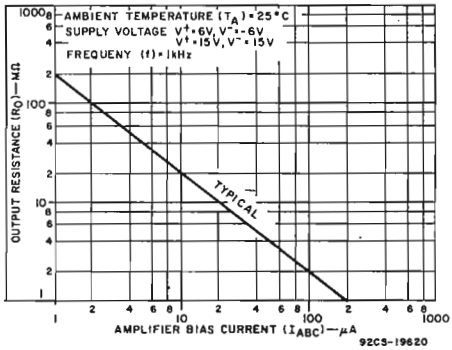


Fig.14—Output resistance vs. amplifier bias current.

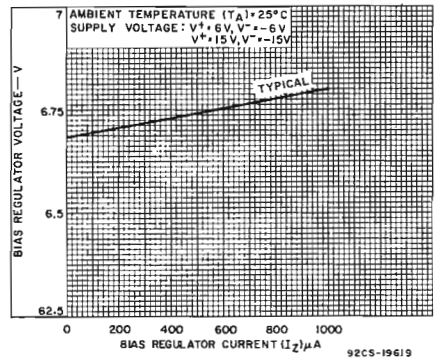


Fig.15—Bias regulator voltage vs. bias regulator current.

OPERATING CONSIDERATIONS

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op-amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op-amp except that the OTA has an extremely high output impedance. Because of this inherent characteristic the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristic is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated on pages 3 and 4 of this data bulletin are similar to those of any typical op-amp.

The OTA circuitry incorporated in the CA3060 (See Fig. 16) provides the equipment designer with a wider variety of circuit arrangements than does the standard op-amp; because as the curves in the data bulletin indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

Bias Considerations for Op-Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the input bias current I_{ABC}. This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

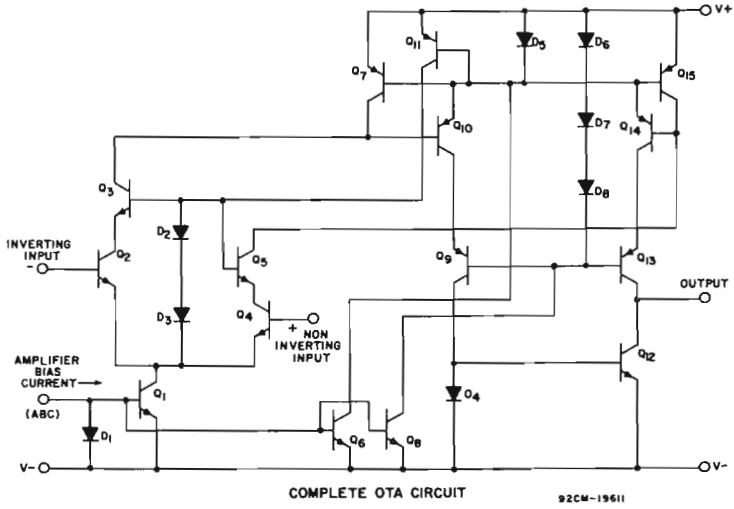


Fig.16 — Complete schematic diagram showing one of the three operational transconductance amplifiers.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operational amplifier circuit (See Fig. 17) would proceed as follows:

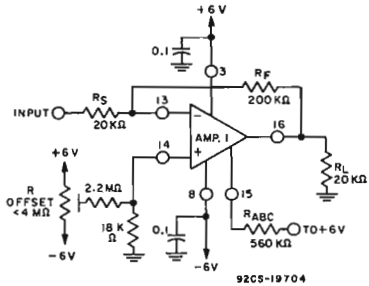


Fig.17—20-dB amplifier using the CA3060.

Circuit Requirements
Closed loop voltage gain = 10 (20 dB)
Offset voltage adjustable to zero
Current drain as low as possible
Supply voltage = ±6 V
Maximum input voltage = ±50 mV
Input resistance = 20 kΩ
Load resistance = 20 kΩ
Device: CA3060

Calculation

1. Required transconductance g_{21}.
   Assume that the open loop gain A_{OL} must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by

$$g_{21} = A_{OL}/R_L$$

$$= 100/18\ k\Omega$$

$$\cong 5.5\ mmho$$

(R_L = 20 kΩ in parallel with 200 kΩ

≅ 18 kΩ)

2. Selection of suitable amplifier bias current.
   The amplifier bias current is selected from the minimum value curve of transconductance (Fig. 10a) to assure that the amplifier will provide sufficient gain. For the required g_{21} of 5.5 mmho an amplifier bias current I_{ABC} of 20 μA is suitable.

3. Determination of Output Swing Capability.
   For a loop gain of 10 the output swing is ±0.5 V and the peak load current 25 μA. However, the amplifier must also supply the necessary current through the feedback resistor and for R_S = 20 kΩ than R_F = 200 kΩ if A_{OL} = 10. Therefore, the feedback loading = 0.5/200 kΩ = 2.5 μA.

   The total amplifier current output requirements are, therefore, ±27.5 μA. Referring to the data given in Fig. 6a we see that for an amplifier bias current of 20 μA the amplifier output current is ±40 μA. This is obviously adequate and it is not necessary to change the amplifier bias current I_{ABC}.

4. Calculation of bias resistance.
   For minimum supply current drain the amplifier bias current I_{ABC} should be fed directly from the supplies and not from the bias regulator. The value of the resistor R_{ABC} may be directly calculated using Ohm's law.

$$R_{ABC} = \frac{V_{SUP} - V_{ABC}}{I_{ABC}}$$

$$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

$$= 568.5\ k\Omega \text{ or } \cong 560\ k\Omega$$

5. Calculation of offset adjustment circuit.
   In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input.

i.e. $$\frac{20 \times 200 \times 10^6 \text{ ohms}}{220 \times 10^3} \cong 18\ k\Omega$$

Because the maximum offset voltage is 5 mV and an additional increment due to the offset current (Fig. 4) flowing through the source resistance

(i.e. $200 \times 10^{-9} \times 18 \times 10^3$ volts), therefore,

the Offset Voltage Range = 5 mV + 3.6 mV = ±8.6 mV

The current necessary to provide this offset is

$$\frac{8.6 \times 10^{-3}}{18 \times 10^3} \text{ or } 0.48\ \mu A$$

With a supply voltage of ±6 V, this current can be provided by a 10 MΩ resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2 MΩ was used in the final circuit.

OTHER CONSIDERATIONS

Capacitance Effects

The CA3060 is designed to operate at such low power levels that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10-kΩ load with a stray capacitance of 15 pF has a time constant of 1 MHz. Fig. 18 illustrates how a 10-kΩ 15-pF load modifies the frequency characteristic.

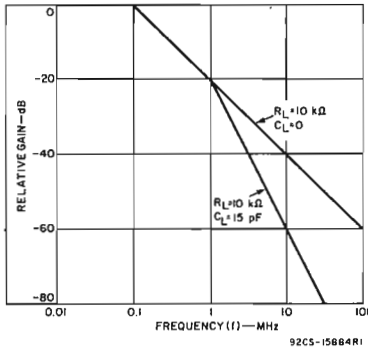


Fig. 18—Effect of capacitive loading on frequency response.

Capacitive loading also has an effect on slew rate; because the peak output current is established by the amplifier bias current, I_{ABC} (see Fig. 6a), the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the I_{OM}. Therefore,

$$SR = dV/dt = I_{OM}/C_L$$

where C_L is the total load capacitance including strays. This relationship is shown graphically in Fig. 19. When measuring slew rate for this data bulletin, care was taken to keep the total capacitive loading to 13 pF.

Phase Compensation

In many applications phase compensation will not be required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier as shown in Fig. 13. The values given in Fig. 13 provide stable operation for the critical unity gain condition, assuming that capacitive loading on the output is 13 pF or less. Input phase compensation is recommended in order to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

APPLICATIONS

Having determined the operating points of the CA3060 amplifiers, they can now function in the same manner as conventional op-amps, and thus, are well suited for most op-amp applications, including inverting and non-inverting amplifiers, integrators, differentiators, summing amplifiers etc.

TRI-LEVEL COMPARATOR

Tri-level comparator circuits are an ideal application for the CA3060 since it contains the requisite three amplifiers. A tri-level comparator has three adjustable limits. If either the upper or lower limit is exceeded, the appropriate output is activated until the input signal returns to a selected intermediate limit. Tri-level comparators are particularly suited to many industrial control applications.

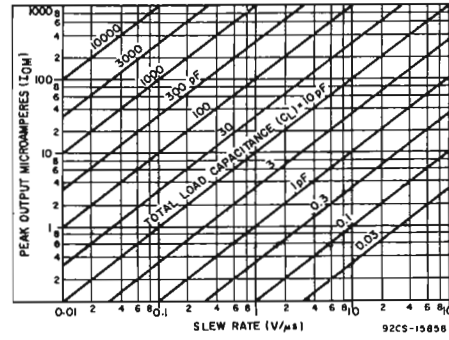


Fig. 19—Effect of load capacitance on slew rate.

Circuit Description

Fig. 20 shows the block diagram of a tri-level comparator using the CA3060. Two of the three amplifiers are used to compare the input signal with the upper-limit and lower-limit reference voltages. The third amplifier is used to compare the input signal with a selected value of intermediate-limit reference voltage. By appropriate selection or resistance ratios this intermediate-limit may be set to any voltage between the upper-limit and lower-limit values. The output of the upper-limit and lower-limit comparator sets the corresponding upper or lower-limit flip-flop. The activated flip-flop retains its state until the third comparator (intermediate-limit) in the CA3060 initiates a reset function, thereby indicating that the signal voltage has returned to the intermediate-limit selected. The flip-flops employ two CA3086 transistor-array IC's, with circuitry to provide separate "SET" and "POSITIVE OUTPUT" terminals.

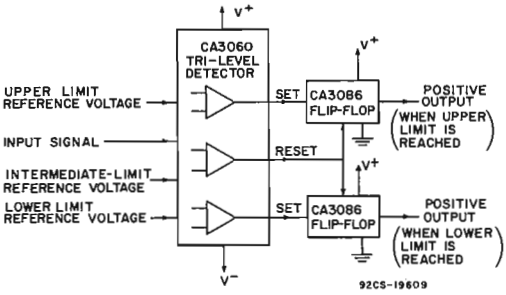


Fig.20—Functional block diagram of a tri-level comparator.

The circuit diagram of a tri-level comparator appears in Fig. 21. Power is provided for the CA3060 via terminals 3 and 8 by ±6-volt supplies and the built-in regulator provides amplifier-bias-current (I_{ABC}) to the three amplifiers via terminal 1. Lower-limit and upper-limit reference voltages are selected by appropriate adjustment of potentiometers R1 and R2, respectively. When resistors R3 and R4 are equal in value (as shown), the intermediate-limit reference voltage is automatically established at a value midway between the lower-limit and upper-limit values. Appropriate variation of resistors R3 and R4 permits selection of other values of intermediate-limit voltages. Input signal (E_S) is applied to the three comparators via terminals 5, 12, and 14. The "SET" output lines trigger the appropriate flip-flop whenever the input signal reaches a limit value. When the input signal returns to an intermediate-value, the common flip-flop "RESET" line is energized. The loads in the circuits, shown in Fig. 21 are 5-V, 25-mA lamps.

Active Filters — Using the CA3060 as a Gyrator

The high output impedance of the OTAs makes the CA3060 ideally suited for use as a gyrator in active filter applications. Fig. 22 shows two OTAs of the CA3060 connected as a gyrator in an active filter circuit. The OTAs in this circuit can make a 3-μF capacitor function as a floating 10-kilohenry inductor across Terminals A and B. The measured Q of 13 (at a frequency of 1 Hz) of this inductor compares favorably with a calculated Q of 16. The 20-kilohm to 2-megohm attenuators in this circuit extend the dynamic range of the OTA by a factor of 100. The 100-kilohm potentiometer, across V+ and V⁻, tunes the inductor by varying the g_{21} of the OTAs, thereby changing the gyration resistance.

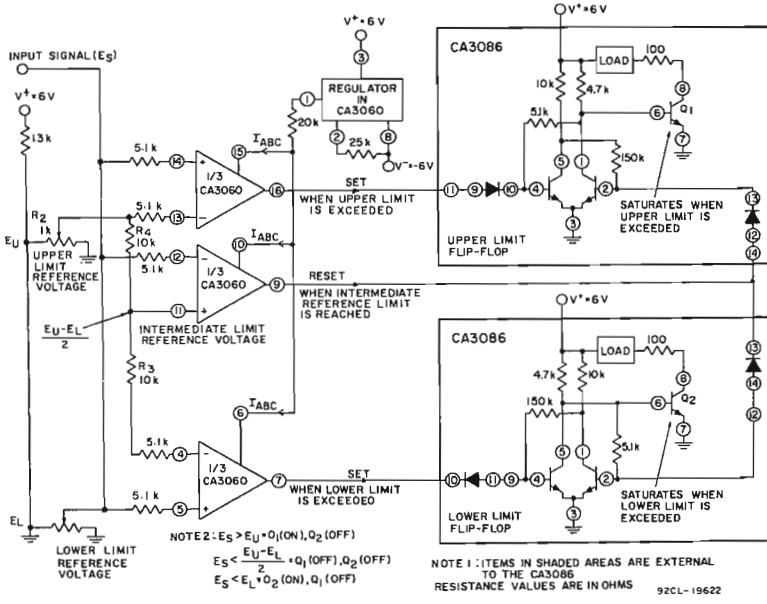


Fig.21—Tri-level comparator circuit.

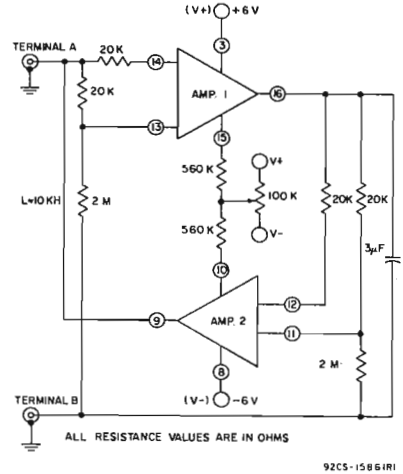


Fig.22—Two operational transconductance amplifiers of the CA3060 connected as a gyrator in an active filter circuit.

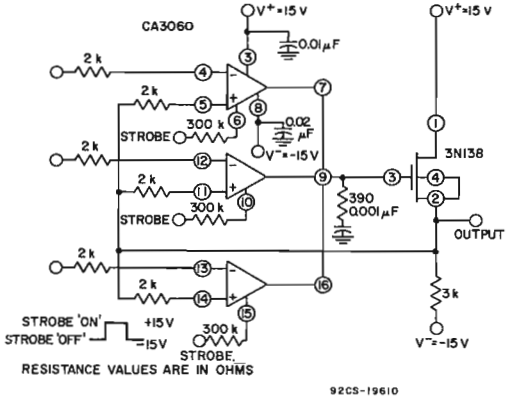


Fig.23—Three-channel multiplexer.

THREE CHANNEL MULTIPLEXER

Fig. 23 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N138 MOS/FET as a buffer and power amplifier.

When the CA3060 is connected as a high-input impedance voltage follower, and strobe "ON," each amplifier is activated and the output swings to the level of the input of that amplifier. The cascade arrangement of each CA3060 amplifier with the MOS/FET provides an open loop voltage gain in excess of 100 dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback.

Operation at ±6 volts is also possible with several minor changes. First, the resistance in series with amplifier bias current (I_{ABC}) terminal of each amplifier should be decreased to maintain 100 μA of strobe—"ON" current at this lower supply voltage. Second, the drain resistance for the MOS/FET should be decreased to maintain the same value of source current. The low cost dual-gate protected MOS/FET, RCA-40841, may be used when operating at the low supply voltage.

The phase compensation network consists of a single 390Ω resistor and a 1000-pF capacitor, located at the interface of the CA3060 output and the MOS/FET gate. The bandwidth of the system is 1.5 MHz and the slew rate is 0.3 volts/μsec. The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

NON LINEAR APPLICATIONS

AM Modulator (Two-Quadrant Multiplier)

Fig. 24 shows Amplifier No. 3 of the CA3060 used in an AM modulator or 2-quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Fig. 24, is obtained. Fig. 24 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to $V_{\bar{}}$.

The two-quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Fig. 24. The polarity of the output must follow that of the differential input; therefore, the output is positive only during, the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or I_{ABC} are zero.

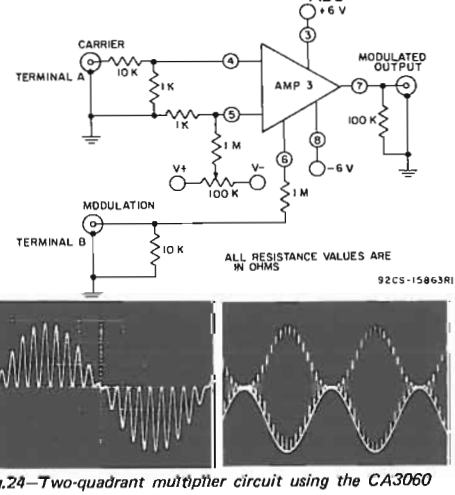


Fig.24—Two-quadrant multiplier circuit using the CA3060 with associated waveforms.

Four-Quadrant Multiplier

The CA3060 is also useful as a four-quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifier Nos. 1, 2, and 3, is shown in Fig. 25 and a typical circuit is shown in Fig. 26. The multiplier consists of a single CA3060 and, as in the two-quadrant multiplier, exhibits no level shift between input and output. In Fig. 25, Amplifier No. 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier No. 1 is calculated as follows:

$$I_{O(1)} = [-V_X]\ [g_{21}(1)] \qquad \text{(Eq.3)}$$

Ampl. No. 2 is a non-inverting amplifier so that

$$I_{O(2)} = [+V_X]\ [g_{21}(2)] \qquad \text{(Eq. 4)}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L\ [g_{21}(2) \cdot g_{21}(1)] \qquad \text{(Eq. 5)}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the g_{21} is also controlled. Amplifier No. 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V\text{-}) + V_Y}{R_1} \qquad \text{(Eq. 6)}$$

Hence,

$$g_{21}(2) \approx k\ [\ (V\text{-}) + V_Y\ ]. \qquad \text{(Eq. 7)}$$

Bias for Amplifier No. 1 is derived from the output of Amplifier No. 3 which is connected as a unity-gain inverting amplifier. $I_{ABC(1)}$, therefore, varies inversely with V_Y. And by the same reasoning as above

$$g_{21}(1) \approx k\ [(V\text{-}) - V_Y]. \qquad \text{(Eq. 8)}$$

Combining equation 5, 7, and 8 yields:

$$V_O \approx V_X \cdot k \cdot R_L \left\{[(V\text{-}) + V_Y] - [(V\text{-}) - V_Y]\right\} \text{ or}$$

$$V_O \approx 2\,k\,R_L\,V_X\,V_Y$$

Fig. 26 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers No. 1 and No. 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier No. 2 and permits adjusting the offset voltage of Amplifier No. 1 to zero by means of the 100-kΩ potentiometer. Next, remove the short between Terminals 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier No. 1 and permits Amplifier No. 2 to be zeroed with the other potentiometer. With AC signals on both the X and Y input, R3 and R11 are adjusted for symmetrical output signals. Fig. 27 shows the output waveform with the multiplier adjusted. The voltage waveform in Fig. 27a shows suppressed carrier modulation of 1-kHz carrier with a triangular wave.

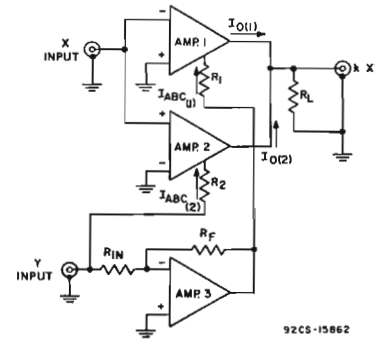


Fig.25—Four-quadrant multiplier using the CA3060.

Figures 27b and 27c, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the outputs are always positive and return to zero after each cycle.

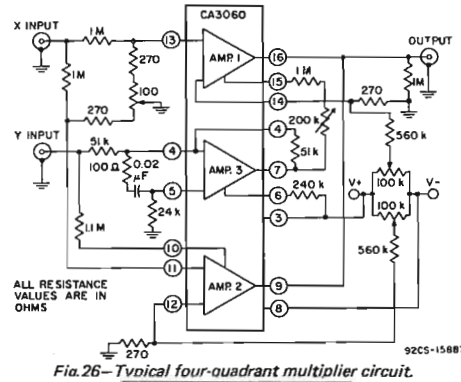


Fig.26—Typical four-quadrant multiplier circuit.

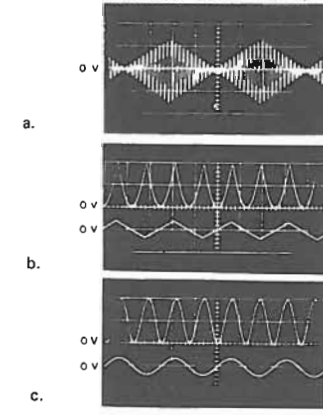


Fig.27—Voltage waveforms of four-quadrant multiplier circuit.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA3062

Approx. 2½ times actual size

Modified 12-lead TO-5 style package

Photo Detector and Power Amplifier

For Photoelectric Control Applications

Features

- 100 mA output-current capability — can drive a relay or thyristor directly
- 5 to 15 volt dc supply voltage
- Compact — complete system in a TO-5 style package

The CA3062* is an integrated circuit consisting of a photosensitive section, an amplifier, and a pair of high-current output transistors on a single monolithic chip.

The photosensitive section consists of Darlington pairs and affords high sensitivity. The power amplifier has a differential configuration which provides complementing outputs in response to a light input — normally "ON" and normally "OFF". The separate photodetector, amplifier, and high-current switch provide flexibility of circuit arrangement. This feature plus the high current capability of the output section, can now provide the user with a complete system particularly useful in photoelectric control applications utilizing IR emitters and visible-light sources.

*Formerly developmental type TA5371B.

Applications

- Counters
- Sorting
- Level controls
- Inspection
- Intrusion alarms
- Position sensor
- Edge monitoring
- Isolators

- See ICAN-6538, "Applications of the RCA-CA3062 IC Photodetector and Power Amplifier in Switching Circuits"

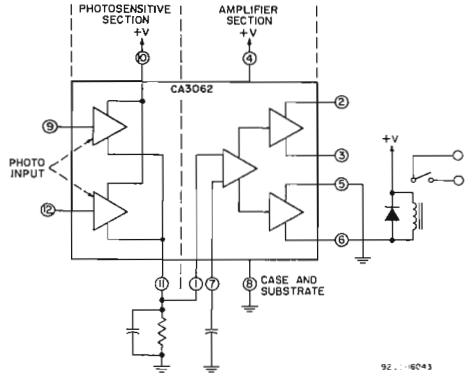


Fig. 1 - Light operated relay using CA3062.

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION:

- Up to T_A = 55°C . . . . . 700 mW
- Above T_A = 55°C . . . . . Derate linearly 5.6 mW/°C
- At Case Temperature (T_C) ≤ 55°C . . . . . 1.5 W
- Above T_C = 55°C . . . . . Derate linearly 16 mW/°C

TEMPERATURE RANGE:

- Operating . . . . . -55°C to +125°C
- Storage . . . . . -65°C to +150°C

LEAD TEMPERATURE (During soldering):

- At distance ≥ 1/32 in (3.17 mm) from seating plane for 10 s max . . . . . +300°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 3 is +15 to 0 volts.

TERMINAL No.	10	11	12	1	2	3	4	5	6	7	8
9	0 -9	+2 -5	*	*	*	*	*	*	*	*	*
10		+9 0	+9 0	*	*	*	*	*	*	*	+15 0
11			+5 -2	*	*	*	*	*	*	*	*
12				*	*	*	*	*	*	*	*
1					*	*	*	*	*	+5 -5	+3 -3
2						+15 0	*	*	*	*	+15 0
3							*	*	*	*	+5 0
4								*	*	*	+9 0
5									0 -15	*	+5 0
6										*	+15 0
7											+3 -3
8	Reference Substrate and Case										

Maximum Current Ratings

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9	1	0.1
10	5	0.1
11	0.1	5
12	1	0.1
1	1	0.1
2	100	0.1
3	0.1	100
4	10	1
5	0.1	100
6	100	0.1
7	1	0.1
8	1	10

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	MEASUREMENT TERMINAL Nos.	TEST CIRCUIT FIG.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC CHARACTERISTICS								
Photo Darlington Section: Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	E = 0 lumens/ft^2, I_C = 1 mA	10–11	–	10	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 0.1 mA, E = 0	9–11, 12–11	–	10	–	–	V
Dark Current	I_{DARK}	V_{CE} = 7.5 V, E = 0	10	3	–	0.1	30	μA
Photo Current	I_P	V_{CE} = 7.5 V, E = 8 lumens/ft^2	10	3	–	60	–	μA
Wavelength of Max. Sensitivity	λ max.			3	–	725	–	Note 2 / nm
Relative Angular Sensitivity				–	–	–	–	–
Area of Each Photo Transistor				–	1.3 x 10^{-4} cm^2			
Amplifier Section Output Transistor: Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO\,6}$ / $V_{(BR)CEO\,7}$	I_C = 1 mA	2-3, 6-5	–	15	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO\,6}$ / $V_{(BR)EBO\,7}$	I_E = 1 mA	3-8, 6-8	–	5	–	–	V
DC Supply Current	I_{SUPPLY}	V_4 = 7.5 V	4	–	–	5.5	10	mA
Sensitivity: Illumination, For Normal "OFF" Output	E_{ON}	Set light input for I_6 = 70 mA	6	7, 15, 17	–	8	70	Notes 1, 3 lumens per ft^2
For Normal "ON" Output	E_{OFF}	Set light input for I_2 = 5 mA	2	17	–	10	–	Notes 1, 3 lumens per ft^2
DYNAMIC CHARACTERISTICS								
Overall Response Time: Turn-On Time	t_{on}	E = 700 μW/cm^2 at λ = 930 nm	——	12	–	38	–	μs
Rise Time	t_r				–	125	–	μs
Turn-Off Time	t_{off}				–	43	–	μs
Fall Time	t_f				–	20	–	μs

NOTES

(1) Tungsten filament light source at a color temperature of 2854K.
(2) One (1) nanometer = 10 Angstrom units.
(3) A radiant flux density of 7.5 μW/cm^2 at 725 nm produces the same photocurrent as 1 lumen/ft^2 from a tungsten filament lamp at a color temperature of 2854K.

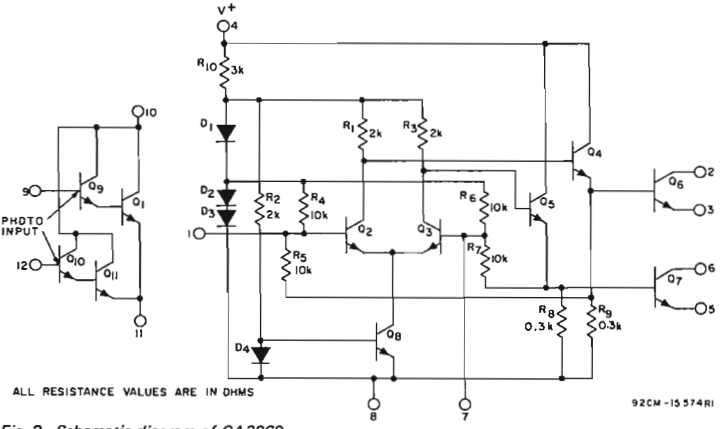


Fig. 2 - Schematic diagram of CA3062.

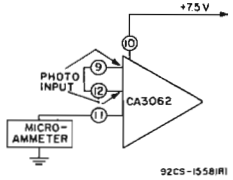


Fig. 3 - Test circuit for photocurrent and typical spectral response of photosensitive Darlington unit.

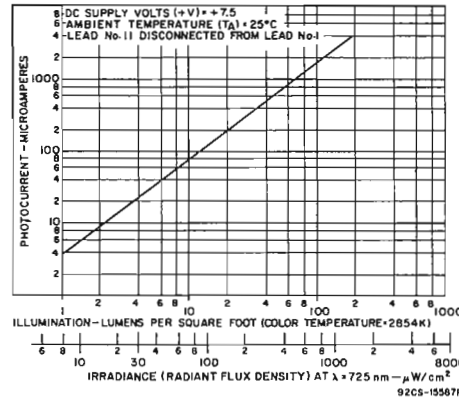


Fig. 4 - Photocurrent as a function of radiant flux.

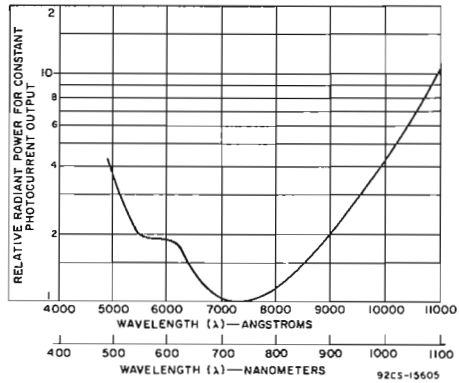


Fig. 5 - Typical spectral response of photosensitive Darlington unit.

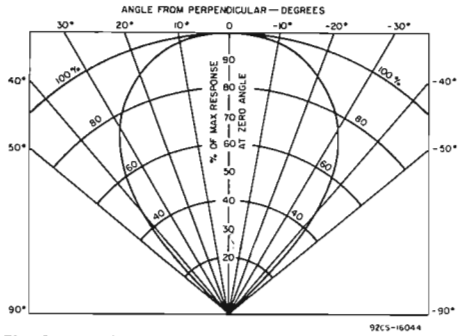


Fig. 6 - Relative angular sensitivity.

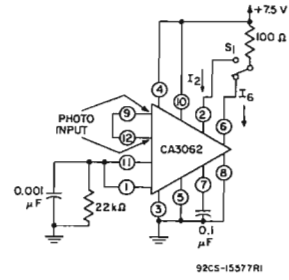


Fig. 7 - Test circuit for sensitivity and dc current measurement.

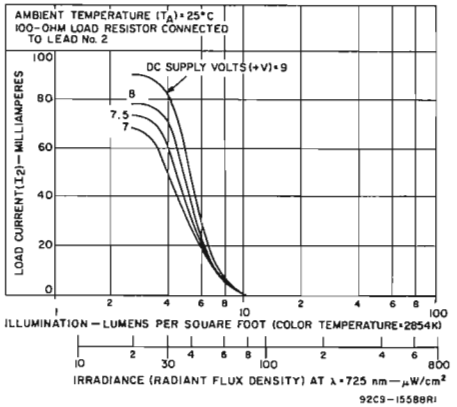


Fig. 8 - Load current (I_2) vs. illumination as a function of supply volts.

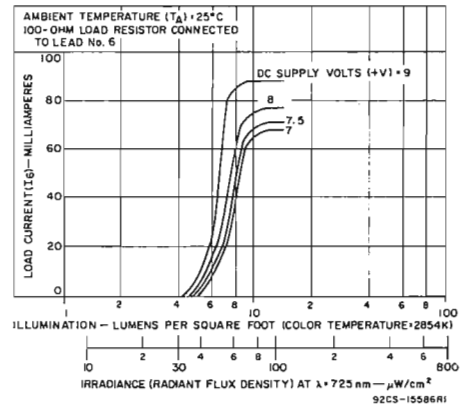


Fig. 9 - Load current (I_6) vs. illumination as a function of supply volts.

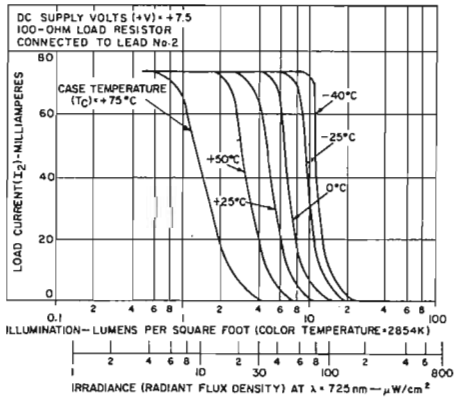


Fig. 10 - Load current (I_2) vs. illumination as a function of case temperature.

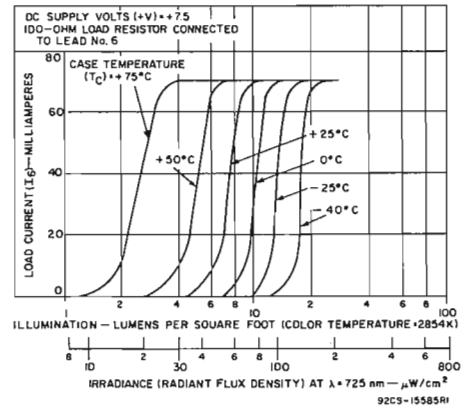


Fig. 11 - Load current (I_6) vs. illumination as a function of case temperature.

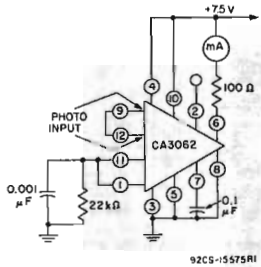


Fig. 12 - Response time test circuit.

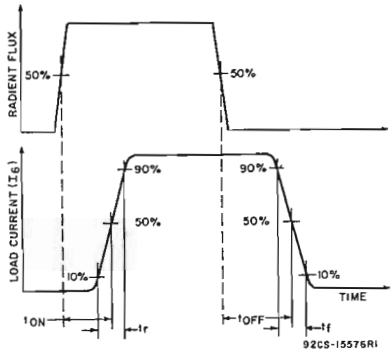


Fig. 13 - Waveforms for measurement of response time.

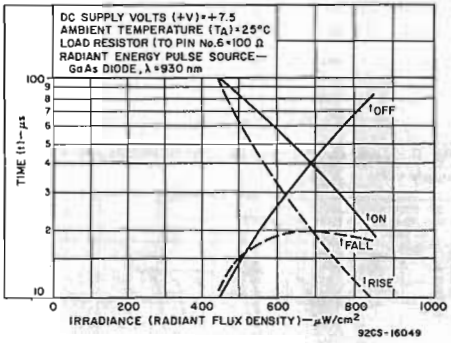


Fig. 14 - Response time as a function of radiant flux density.

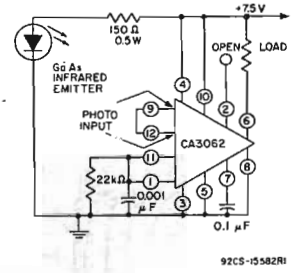


Fig. 15 - Circuit diagram for "ON-OFF" photoelectric control applications.

OPERATING CONSIDERATIONS

Switching Service

The CA3062 is primarily intended to provide "ON-OFF" output in response to a light signal. Optimum performance of this device is achieved when the output transistors are operated at values of load current sufficient to saturate the device in the "ON" state. Operation of the CA3062 at values of load current between the condition of no load current and saturation will cause substantial power to be dissipated in the silicon chip. This condition of operation is therefore not recommended because the heat rise in the silicon chip induced by the increased power dissipation causes the load current to shift in the same direction as though additional illumination were applied to the CA3062, a condition which will substantially alter the switching characteristics of the device.

The signal voltages at the input terminals (terminal No. 1 and No. 7) must not exceed 3 volts, because any increase in the signal voltage beyond the value specified will cause both output transistors to be turned "ON". In the circuit shown in Fig. 7, this condition will occur for values of illumination greater than 60 lumens/ft ^{2}. This adverse operating condition can be avoided by either limiting the maximum illumination or by clamping the input so that the voltage does not exceed 3 volts.

Linear Service

The CA3062 can be connected as shown in Fig. 16 to give a linear output. The value of the load resistor should be greater than 1000 ohms in order to limit the power dissipation and thus minimize the heating effects. Because of the many possible variations in circuit configurations, the CA3062 has not been characterized for linear service applications. A guide-line circuit for this class of service is shown in Fig. 16.

Specific inquiries for use of the CA3062 in this type of service should be addressed to your local RCA Field Technical Representative.

Precautions

Because of the high amplification of the CA3062, care should be taken, when wiring, to keep all lead lengths as short as possible. A recommended breadboard layout is shown in Fig. 17.

If the CA3062 is operated with an inductive load impedance, such as a relay, it is recommended that a diode be connected across the load to absorb the energy of the pulse voltages generated during switching.

Many of the graphs are shown with two sets of abscissa values for light energy input, one expressed in illumination values (lumens/sq. ft.) and the other in irradiance values (μW/sq. cm.)

Correlation between these two sets of abscissa values is accomplished by having the light source operating at the maximum sensitivity wavelength of the CA3062. See Notes on page three.

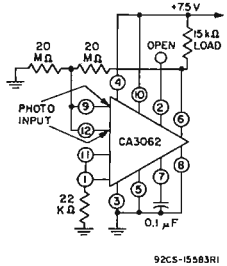


Fig. 16 - Circuit diagram for linear output photoelectric applications.

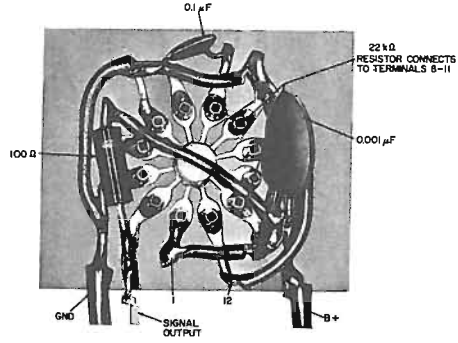


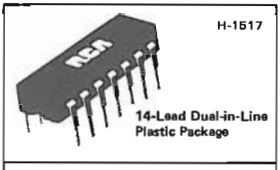
Fig. 17 - Breadboard layout of test circuit, shown in Fig. 7 for the CA3062.

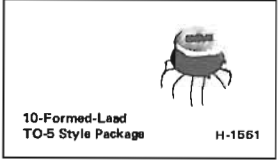
RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3064
CA3064E





TV Automatic Fine Tuning Circuit

Features:

- Cascode type high-gain amplifier (18 mV input for rated output)
- Internal voltage regulator
- Differential detector
- For use with either color or monochrome
- Differential amplifier
- Bipolar outputs
- Wide operating-temperature range; −55 to +125°C

RCA-CA3064 and CA3064E represent the third generation of integrated circuits designed primarily for AFC (Automatic-Frequency-Control) applications. They provide all of the signal-processing components needed (with the exception of the tuned-phase-detector transformer) to derive the AFT correction signals from the output of the video-if amplifier. The CA3064 is supplied in the 10-formed-lead TO-5 style package, and the CA3064E in the 14-lead dual-in-line plastic package. Both types operate over the temperature range of −55 to +125°C.

The CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1 but embody a higher-gain input amplifier which provides a 20-dB improvement in sensitivity. The increased sensitivity extends the application of a proven AFT system to the low-level if-amplifier stages in TV receivers.

Because the CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1, refer to Application Note ICAN-5831, "Application of the RCA CA3044 and CA3044V1 Integrated Circuits in Automatic Fine-Tuning Systems" for general application information.

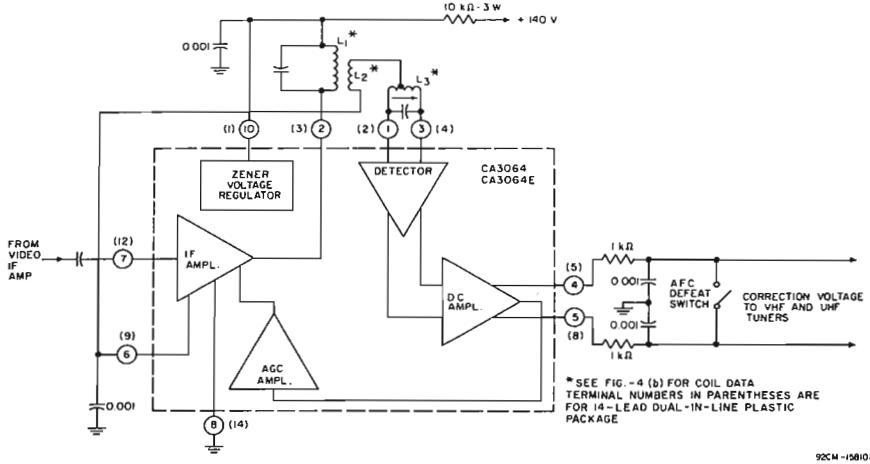


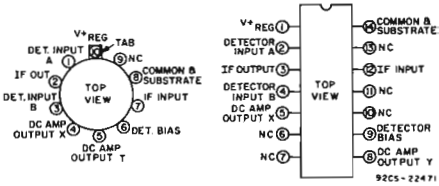
Fig.1 – Block diagram of typical operating circuit utilizing the CA3064 and CA3064E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DEVICE DISSIPATION:
- Up to $T_A = 25^oC$ . . . . . 700 mW
- Above $T_A = 25^oC$ . . . . . derate linearly 5.6 mW/^{o}C

AMBIENT TEMPERATURE RANGE:
- Operating . . . . . −55 to +125^{o}C
- Storage . . . . . −65 to +150^{o}C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max.. . . . . 265^{o}C



(a) CA3064 *(b) CA3064E*

Fig.2 – Terminal assignment diagrams.

MAXIMUM VOLTAGE RATINGS at $T_A = 25^oC$

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 (3) and horizontal terminal 6 (9) is +20 to 0 volts. Terminal nos. in parentheses are for the 14-lead dual-in-line plastic package.

TERMINAL No.	9(6,7, 10,11, 13)	10 (1)	1 (2)	2 (3)	3 (4)	4 (5)	5 (8)	6 (9)	7 (12)	8 (14)
9(8,7,♦ 10,11, 13)	← NO INTERNAL CONNECTION →									
10 (1)			+12 0	+10 -10	+12 0	+12 0	+12 0	+10 0	+20 0	▲
1 (2)				*	+10 - 10	*	*	+5 - 5	*	+5 - 6
2 (3)					*	*	*	+20 0	*	+20 0
3 (4)						*	*	+5 - 6	*	+5 - 6
4 (5)							*	*	*	+12 0
5 (8)								*	*	+12 0
6 (9)									+5 - 2	+2 0
7 (12)										+2 - 10
8 (14)										REF.SUBSTRATE & CASE■

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9(6,7, 10,11, 13)	-	-
10 (1)	50	50
1 (2)	1	0.1
2 (3)	20	20
3 (4)	1	0.1
4 (5)	5	5
5 (8)	5	5
6 (9)	5	5
7 (12)	1	1
8 (14)	50	50

▲ Terminal number 10 (1) may be connected to any positive voltage source greater than the internal zener regulating voltage through a suitable dropping resistor – provided the dissipation rating is not exceeded.

■ This terminal should be connected to the most negative potential of the complete circuit.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

♦ It is recommended that unused terminals 6,7,10,11, and 13 on the 14-lead dual-in-line-plastic package and terminal 9 on the TO-5 package be grounded to act as shields.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS FIG.	TEST CONDITIONS	LIMITS CA3064, CA3064E MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS								
Device Dissipation	P_D	4	V^+ = 30V, R_S = 1.5kΩ; T_A = −25°C	-	135	150	mW	-
			T_A = +25°C	130	140	150		-
			T_A = +85°C	-	145	150		-
Current Drain at 10.5 Volts	I_T	4	$V_{10(1)}$ = 10.5 V	4	6.5	9.5	mA	-
Zener Regulated Voltage — DC Supply Voltage at terminal 10(1)*	$V_{10(1)}$	4	V^+ = 30 V, R_S = 1.5 kΩ	10.9	11.8	12.8	V	-
Quiescent Operating Current into Terminal 2(3)	$I_{2(3)}$	4		1	2	4	mA	-
Quiescent Operating Voltage at Terminal 4(5)	$V_{4(5)}$	-		5	6.9	8	V	-
Quiescent Operating Voltage at Terminal 5(8)	$V_{5(8)}$	-		5	6.9	8	V	-
Output Offset Voltage between Terminals 4 and 5(5 and 8)	V_{4-5} (5-8)	-		-1	0	1	V	-
DYNAMIC CHARACTERISTICS (AS RF AMPLIFIER IN TO-5 STYLE PACKAGE)								
Input Voltage Sensitivity	V_I sensitivity	5	V^+ = +30 V, V_I = 18 mV	Correction Voltage Output as shown in table below.				
Input Admittance	y_{11}	-	f = 45.75 MHz, V^+ = 30 V, R_S = 1.5 kΩ	-	0.41 + j1.0	-	mmho	-
Reverse Transfer Admittance	y_{12}	-		-	0 +j3.4	-	μmho	-
Forward Transfer Admittance	y_{21}	-		-	24.5 - j29	-	mmho	-
Output Admittance	y_{22}	-		-	0.04 + j0.9	-	mmho	-
OUTPUT vs FREQUENCY DEVIATION - AFC								
Correction-Control Voltage at Terminal 4(5)	$V_{corr.\ 4(5)}$	5	V^+ = +30 V, V_I = 18 mV RMS, f_o = MHz as indicated	% of V_{10} (1)		% of V_{10} (1)		
			45.750 - 0.030	85	-	-	V	6,7
			45.750 + 0.030	-	-	25	V	
			45.750 - 0.900	80	-	-	V	7
			45.750 + 0.900	-	-	35	V	
			45.750 - 1.500		-	80	V	
			45.750 + 1.500	35	-		V	
Correction-Control Voltage at Terminal 5(8)	$V_{corr.\ 5(8)}$	5	45.750 - 0.030	-	-	25	V	6,7
			45.750 + 0.030	85	-	-	V	
			45.750 - 0.900	-	-	35	V	7
			45.750 + 0.900	80	-	-	V	
			45.750 - 1.500	35	-	-	V	
			45.750 + 1.500	-	-	80	V	

* Terminal numbers in parentheses are for 14-lead dual-in-line plastic package.

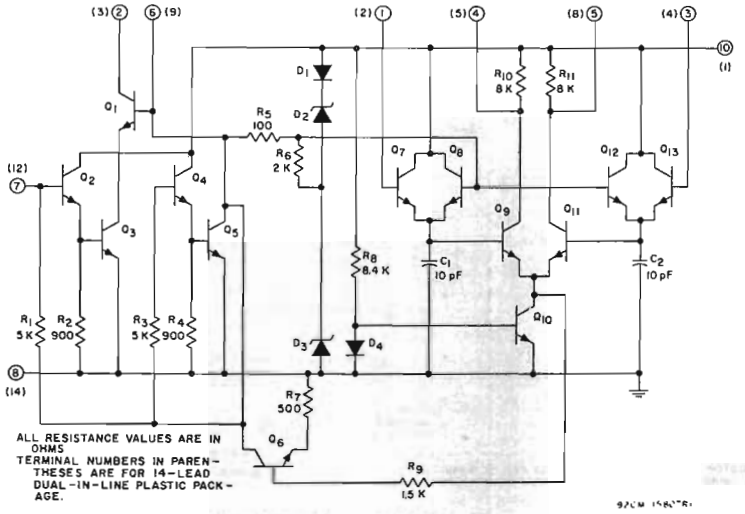


Fig.3 – Schematic diagram for CA3064 and CA3064E.

Circuit Description

The CA3064 and CA3064E integrated circuits can be considered as five functional blocks; an if amplifier-limiter, a balanced detector, a differential dc amplifier, an internally used AGC amplifier, and a zener voltage regulator. The 45-MHz amplifier limiter combination consists of emitter-follower input stage Q2 followed by a cascode-type amplifier Q1, Q3. The emitter-follower input stage Q2 is internally biased, therefore, capacitor coupling must be provided to the input at pin 7 (12) . The external load is connected to pin 2 (3) and should present a load impedance of about 1800 ohms at 45.75 MHz. The detector inputs at pins 1 (2) and 3 (4) from the external transformer are biased through the tertiary winding connected to pin 6 (9), which must be bypassed. The balanced detector is a high-efficiency type consisting of Q7/C1 and Q13/C2, which are internally biased by matching transistors Q8 and Q12. The dc amplifier consists of the differential-amplifier Q9, Q10, Q11, and D4.

The amplifier detector system provides the sharply defined pull-in characteristics shown in figures 5 and 6. The AGC amplifier Q6 senses the detected signals at the collector of A10 and adjusts the gain to compensate for signal changes such as airplane flutter conditions. Diodes D1, D2, and D3 provide the internal voltage regulation.

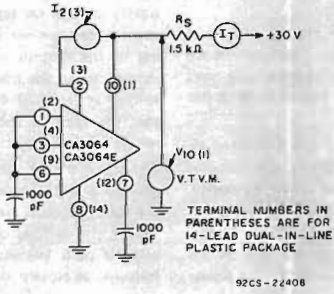
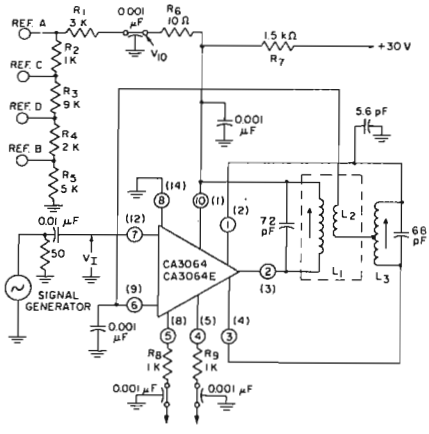


Fig.4 – Test setup: Measurement of total device dissipation, zener regulating voltage, quiescent operating current at terminal 2 (3).



ALL RESISTORS ARE 1% TOLERANCE AND ARE IN OHMS
TERMINAL NUMBERS IN PARENTHESES ARE FOR 14-LEAD DUAL-IN-LINE PLASTIC PACKAGE

92CS-15813R1

L_1 IS ALIGNED FOR SYMMETRICAL BANDWIDTH ON EITHER SIDE OF 45.750 MHz
L_2 TERTIARY WINDING WOUND ON L_1 COIL FORM
L_3 IS ALIGNED FOR ZERO DIFFERENTIAL OUTPUT BETWEEN TERMINALS 4 AND 5 AT f_o = 45.750 MHz
* FOR COIL CONSTRUCTION DATA, SEE FIG.4(b).

REFERENCE VOLTAGE PERCENTAGES	
Ref. A	85% of $V_{10(1)}$
Ref. B	25% of $V_{10(1)}$
Ref. C	80% of $V_{10(1)}$
Ref. D	35% of $V_{10(1)}$

Coil	RCA Distributor Part No.
(L_1, L_2)	122 213
L_3	122 203

Fig.5 (a) – Correction voltage test circuit for CA3064 and CA3064E.

COIL DATA FOR DISCRIMINATOR WINDINGS

L_1 – Discriminator Primary: 3-1/6 turns; #20 Enamel-covered wire – close-wound, at bottom of coil form. Inductance of L_1 = 0.165 μH; Q_o = 120 at f_o = 45.75 MHz.
Start winding at terminal #6; finish at Terminal #1. See Notes below.

L_2 – Tertiary Windings: 2-1/6 turns; #20 Enamel-covered wire – close wound over bottom end of L_1. Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L_3 – Discriminator Secondary: 3-1/2 turns; center-tapped, space wound at bottom of coil form.
Inductance of L_3 = 0.180 μH; Q_o = 150 at f_o = 45.75 MHz.
Start winding at Terminal #2; finish at Terminal #5; connect center tap to Terminal #7. See Notes below.

Notes:
1. Coil Forms; Cylindrical; –0.30" Dia. max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   : Material: Carbinal J or equivalent
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.

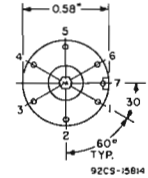


Fig.5 (b) Coil form base terminal diagram.

The CA3064 and CA3064E are specifically intended for use in the AFT system of color television receivers. These devices are tested so that the control voltages generated by the circuit meet the critical requirements of the system. Figure 5 (a) is the schematic diagram of the test circuit.

Figures 5, 6, and 7 show the control voltages generated at terminals 4(5) and 5(8) of the Integrated Circuit as a function of the frequency deviation from the nominal center frequency. Figure 6 shows the region within 30 kHz of the center frequency while Figure 7 covers the entire bandwidth of the system. The horizontal reference lines on the figures are generated by a voltage divider connected between the power supply voltage on terminal 10(1) and ground. The dynamic control voltages are compared with these references according to the Output vs Frequency Deviation Table. For example: when the frequency deviation is –30 kHz the control voltage at terminal 4(5) is greater than the reference A voltage; the control voltage at terminal 5(8) is less than the reference 8 voltage.

The shape of the correction voltage characteristics is dependent to a large degree upon transformer characteristics and the parts layout. In order to closely duplicate the curves shown, the printed circuit boards shown in Figures 8 and 10 and the parts layouts shown in Figures 9 and 11 should be followed as closely as possible.

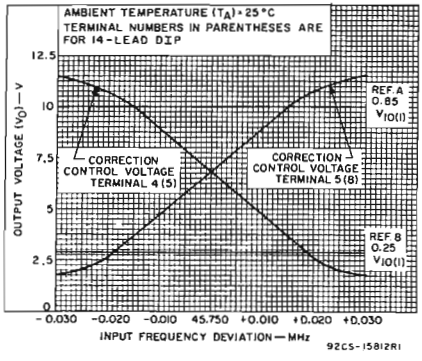


Fig.6 – Typical narrow-band dynamic control voltage characteristics.

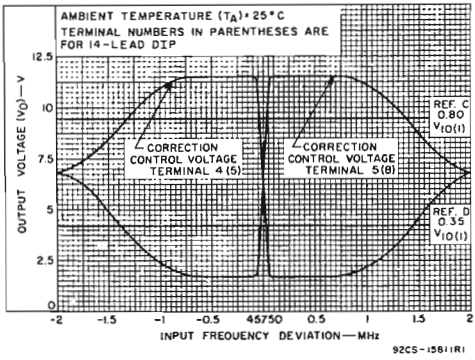


Fig.7 – Typical wide-band dynamic control voltage characteristics.

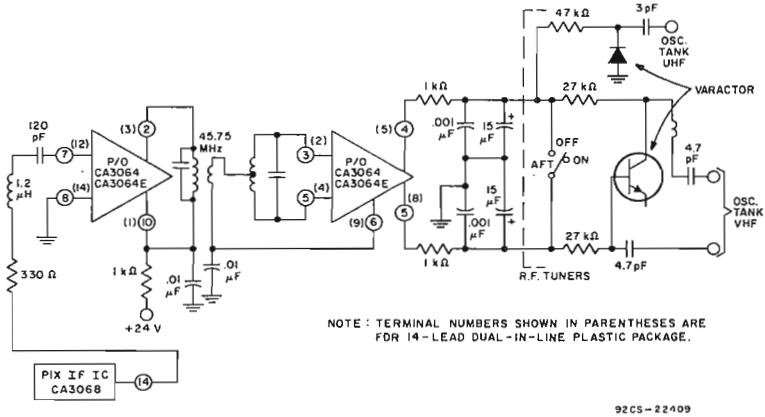
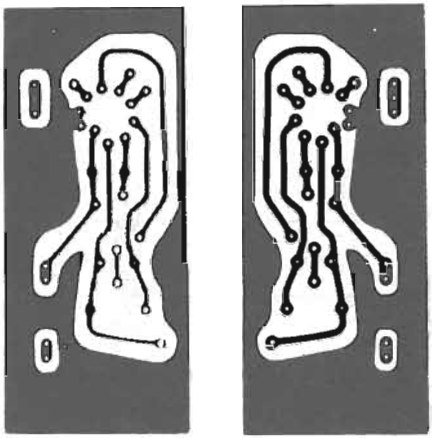


Fig.8 – Typical application of CA3064 and CA3064E AFT IC.



(a) Top view (b) Bottom view

Fig.9 – Printed circuit board for test circuit, (for TO-5 style package).

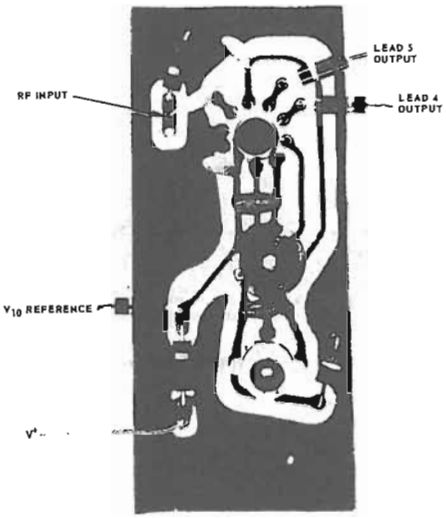
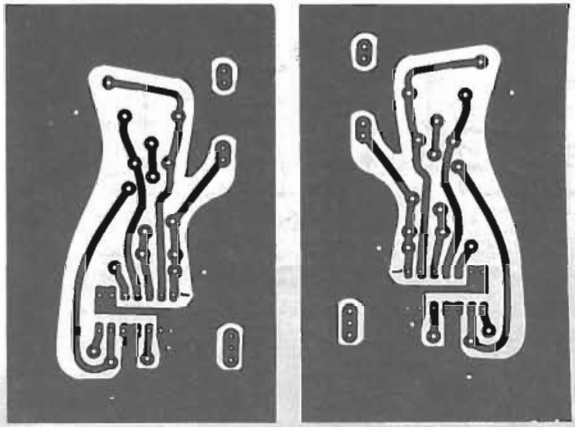


Fig.10 – Top view of wired test board (for TO-5 style package).



(a) Top view (b) Bottom view

Fig.11 – Printed circuit board for test circuit, (for 14-lead dual-in-line plastic package).

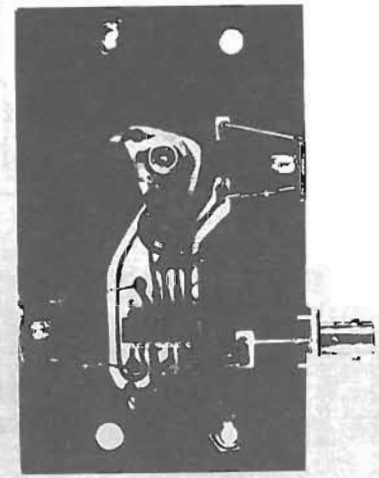


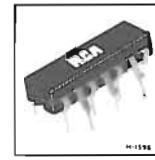
Fig.12 – Top view of wired test board (for 14-lead dual-in-line plastic package)

RCA Solid State Division

Linear Integrated Circuits

CA3065

IF AMPLIFIER-LIMITER, FM DETECTOR, ELECTRONIC ATTENUATOR, AUDIO DRIVER



For Television Sound-System Applications

The RCA CA3065 Television Sound System is a monolithic integrated circuit which combines a multistage IF amplifier limiter, an FM detector, an electronic attenuator, a zener diode regulated power supply, and an audio amplifier-driver that is designed to directly drive an npn power transistor or high-transconductance tube. Because the circuit is so inclusive, a minimum number of external components is required. A block diagram of the integrated circuit television sound system is shown in Fig. 1.

The CA3065 with its advanced circuit design provides a high-performance multistage subsystem for the sound system of a television receiver. A particular feature of the CA3065 is the electronic attenuator which performs the conventional volume control function. Volume control is accomplished when the bias levels in the attenuator are changed by means of a variable resistor connected between Terminal 6 and ground (attenuation in excess of 60 dB is attained). Because no audio signal is present in this control, hum or noise pickup can be bypassed. In most cases, only a single unshielded wire is required between the IF board and the variable resistor (volume control).

The CA3065 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device into suitably punched printed-circuit boards.

FEATURES:

- Electronic attenuator - replaces conventional volume control
- Differential peak detector - requires one single tuned coil
- Internal Zener diode regulated supply
- Inherent high stability
- Excellent AM rejection - 50 dB typ. at 4.5 MHz
- Low harmonic distortion
- High sensitivity - 200 μV limiting (knee) at 4.5 MHz
- Audio drive capability - 6 mA p-p
- Undistorted audio output voltage - 7 V p-p

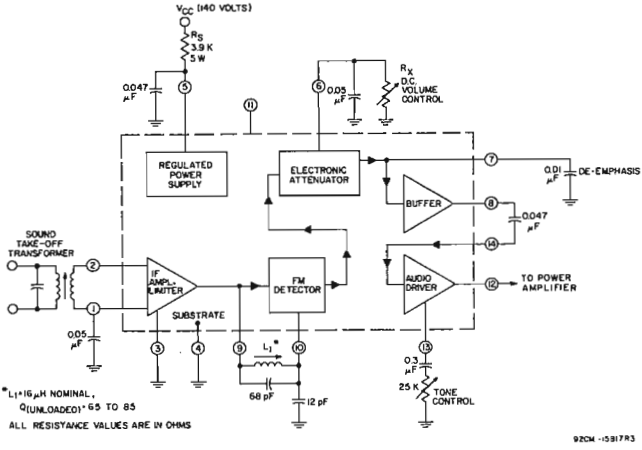


Fig. 1 - Block diagram of CA3065 in a typical circuit application.

MAXIMUM RATINGS, *Absolute Maximum Values*, at T_A = 25°C

Input Signal Voltage (between Terminals 1 and 2) . . .	±3	V
Power Supply Current (Terminal 5)	50	mA
Power Dissipation:		
Up to T_A = 25°C	850	mW
Above T_A = 25°C . . . . . Derate linearly	6.67	mW/°C
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 9 with respect to terminal 3 is 0 to +4 volts.

TERMINAL No.	4	5	6	7	8	9	10	11	12	13	14	1	2	3
4		SUBSTRATE CONNECTION – ALWAYS CONNECT TO TERMINAL 3												
5			+13 0	+13 0	+13 0	*	*	INTERNAL CONNECTION DO NOT USE	+13 0	+13 0	*	*	*	NOTE 1
6				*	*	*	*		*	*	*	*	*	+13 −5
7					+1 −4	*	*		*	*	*	*	*	+13 0
8						*	*		*	*	*	*	*	*
9							*		*	*	*	*	*	+4 0
10									*	*	*	*	*	+4 −5
11									INTERNAL CONNECTION DO NOT USE					
12										+4 −1	*	*	*	*
13											*	*	*	*
14												*	*	+3 −5
1													+5 −5	+5 −5
2														+4 −5
3														

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
4	SUBSTRATE: CONNECT TO TERMINAL 3	
5	50	1
6	1	1
7	1	1
8	0.5	6
9	1	1
10	1	0.1
11	INT. CONN. DO NOT USE	
12	0.5	6
13	1	2
14	1	0.1
1	1	0.1
2	1	0.1
3	0.1	50

Note 1: Terminal No. 5 may be connected to any positive voltage through a suitable resistor provided that the current and dissipation ratings of the CA3065 are not exceeded.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS *at T_A = 25° C, V_{CC} = +140 V applied to Terminal 5 through R_S = 3.9 kΩ, and DC Volume Control (R_x) = 0 unless otherwise indicated.*

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Static Characteristics						
Zener Regulating Voltage Terminal No. 5	V_5		10.3	11.2	12.2	V
Current into Terminal 5	I_5	Connect Terminal 5 to +9 V	10	16	24	mA
Total Device Dissipation	P_T		343	370	400	mW
Terminal Voltages: 1	V_1		–	2	–	V
6	V_6		–	4.8	–	
7	V_7		–	6.1	–	
9	V_9		–	3.7	–	
12	V_{12}		4	5.1	5.8	
Dynamic Characteristics						
IF AMPLIFIER Input Limiting Voltage (at −3 dB point)	$V_{i(lim)}$	f_0 = 4.5 MHz, f_m = 400 Hz, Deviation = ±25 kHz,	–	200	400	μV
AM Rejection	AMR	Amplitude Modulation = 30% f = 4.5 MHz	40	50	–	dB
Transconductance Magnitude	$\|G_m\|$(IF)	f = 4.5 MHz IF Input Terminals: 2, 1 IF Output Terminals: 9, 3	–	500	–	mmho
Phase Angle	θ(IF)		–	46	–	degrees
Feedback Capacitance	C_{fb}	f = 1 MHz; Terminals 2 and 9	–	0.02	–	pF
Input Impedance Components: Parallel Input Resistance	R_i(IF)	Measured between Terminal Nos. 1 and 2	–	17	–	kΩ
Parallel Input Capacitance	C_i(IF)	f = 4.5 MHz	–	4	–	pF
Output Impedance Components: Parallel Output Resistance	R_o(IF)	Measured between Terminal No. 9 and gnd	–	3.25	–	kΩ
Parallel Output Capacitance	C_o(IF)	f = 4.5 MHz	–	7.5	–	pF
DETECTOR Recovered AF Voltage	V_o(af)	f = 4.5 MHz; V_i = 100 mV Δf = ±25 kHz fm = 400 Hz	0.5	0.75	–	V(rms)
Total Harmonic Distortion	THD		–	0.9	2	%
Output Resistance: Terminal 7	R_o		–	7.5	–	kΩ
Terminal 8			–	300	–	Ω
ATTENUATOR		See Fig. 7				
Max. Attenuation	–	R_X = ∞	60	80	–	dB
Max. "Play-through" Voltage*	–	R_X = ∞	–	0.075	1	mV
AUDIO AMPLIFIER						
Voltage Gain	A(af)	V_I = 0.1 V(rms), f = 400 Hz	17.5	20	–	dB
Total Harmonic Distortion	THD	V_O = 2 V(rms), f = 400 Hz	–	1.5	–	%
Undistorted Output Voltage	–	THD = 5%, f = 400 Hz	2	2.5	–	V(rms)
Input Resistance	R_i(af)	f = 400 Hz	–	70	–	kΩ
Output Resistance	R_o(af)	f = 400 Hz	–	270	–	Ω

*"Playthrough" voltage is the unwanted signal, measured at Terminal 8, when the volume control is set for minimum output.

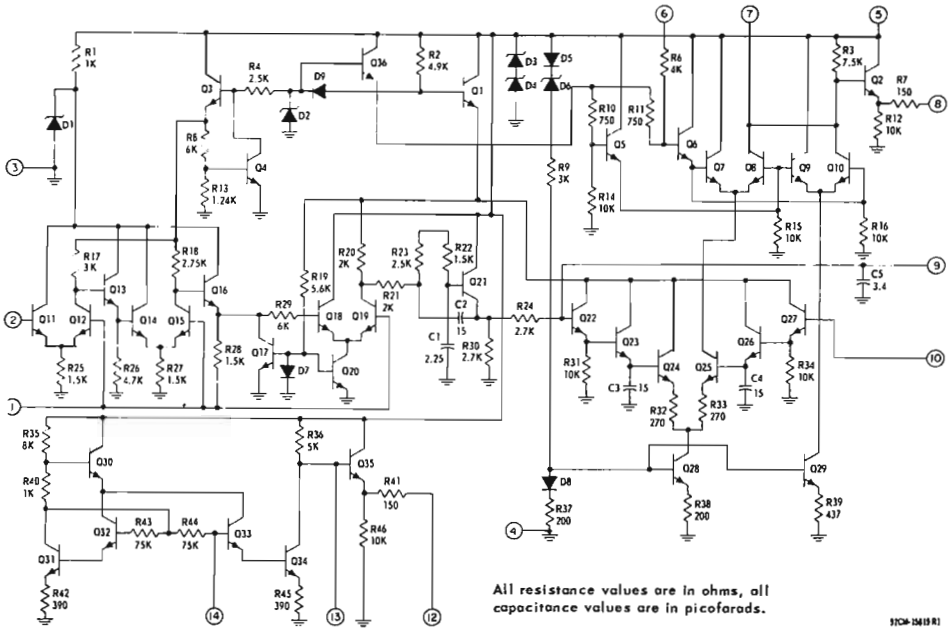


Fig. 2 - Schematic diagram of CA3065

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

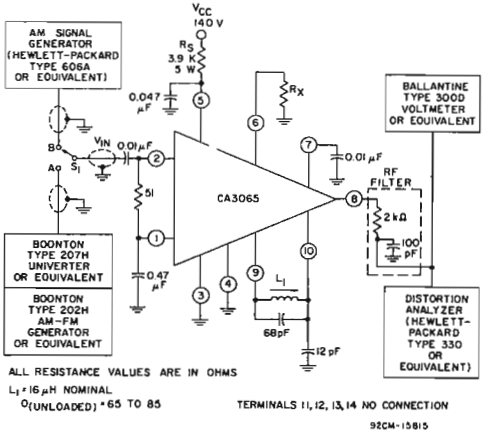


Fig. 3 - Input limiting voltage, AM rejection, recovered audio, total harmonic distortion, maximum attenuation, maximum "play-through" test circuit.

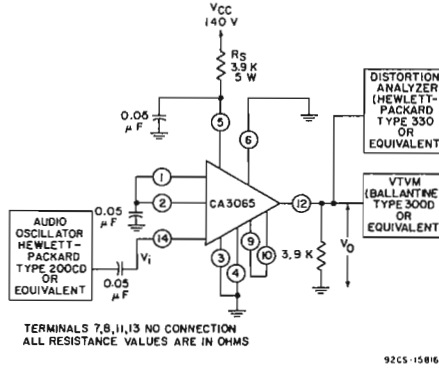
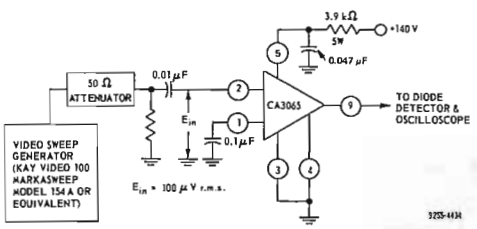
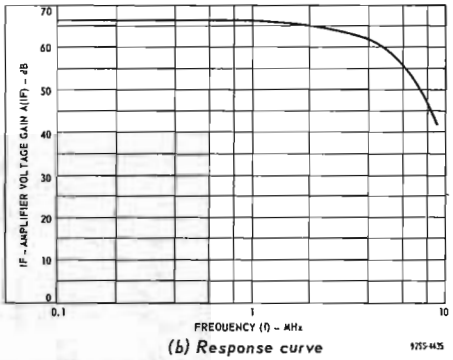


Fig. 4 - Audio voltage gain (undistorted output) test circuit.

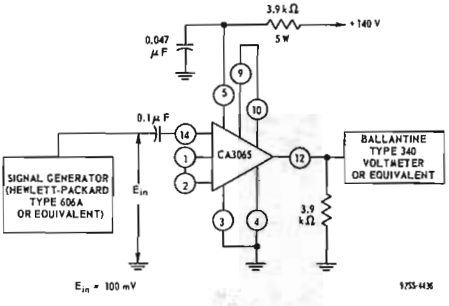


(a) Test circuit

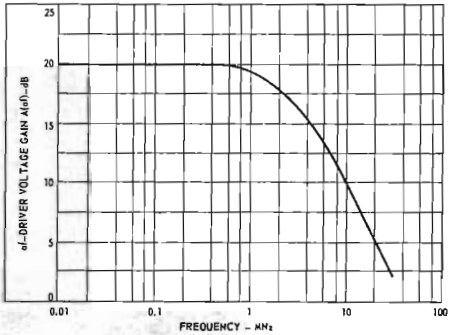


(b) Response curve

Fig. 5 - Frequency response of IF-amplifier section of CA3065



(a) Test circuit



(b) Response curve

Fig. 6 - Frequency response of af-amplifier section of CA3065

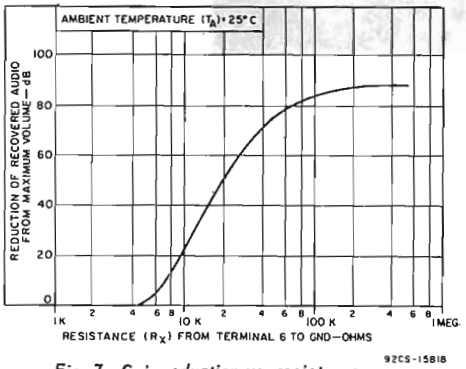


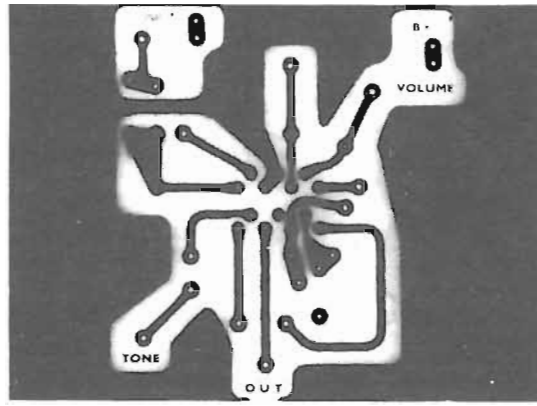
Fig. 7 - Gain reduction vs. resistance (terminal 6 to gnd)

OPERATING CONSIDERATIONS

The CA3065 may be used to drive a video output transistor or a high-transconductance output tube.

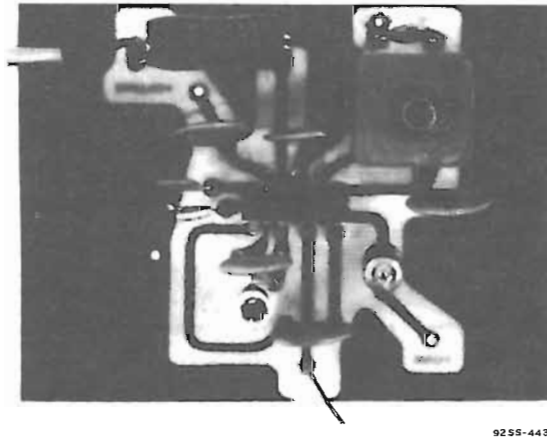
As in all TV receivers, precaution should be taken to prevent destruction of the CA3065 in the event of cascade arcs originating in the picture tube or in the output tube. In the case of arcing in the output tube a resistor of 150k in series with terminal No. 12 and the grid of the tube is usually sufficient protection.

To prevent damage from picture tube arcs, a careful analysis of board layout and coupling modes (electrostatic or magnetic) may be necessary to suggest alternate layouts or appropriate locations for the placement of spark gaps to absorb the high energy discharge.



92SS-4438

*(a) Printed circuit board – bottom view**



92SS-4439

*(b) Parts layout – top view**

Fig. 8 - Recommended parts layout for TV receiver sound strip using CA3065.

* A 200 mil square grid was used in the layout of passive components on the printed circuit board. The Quad-in-line formed leads conform to a standard grid spacing of 100 mil centers.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA3066
CA3067

16-lead Quad-in-line plastic package

CA3066 – CA3067

H-1706

Television Chroma System

The RCA CA3066 and CA3067 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3066 provides subcarrier regeneration and total chroma signal processing prior to demodulation; the CA3067 performs the demodulation and tint control functions. Each device utilizes a 16-lead quad-in-line plastic package.

System Features

CA3066
CHROMA SIGNAL PROCESSOR

- Complete Color Sync Circuit
- Blanked Chroma Amplifier
- Chroma Band-Pass Amplifier
- Low Output Impedance Chroma Driver
- ACC Detector-Amplifier
- Killer Detector-Amplifier
- DC Chroma Gain Control
- Zener Diode for Regulated Voltage Reference
- Short-Circuit Protection on All Terminals

CA3067
CHROMA DEMODULATOR

- Balanced Chroma Demodulators
- Color Difference Matrix
- DC Tint Control
- Three Low Output Impedance Drivers for Direct Coupling
- Reference Subcarrier Limiter
- Zener Diode for Regulated Voltage Reference
- Internal RF Filtering

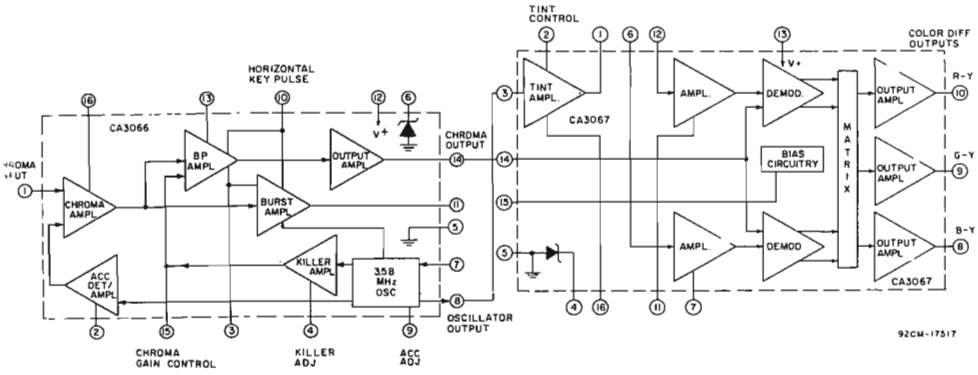


Fig. 1 - TV chroma system functional block diagram.

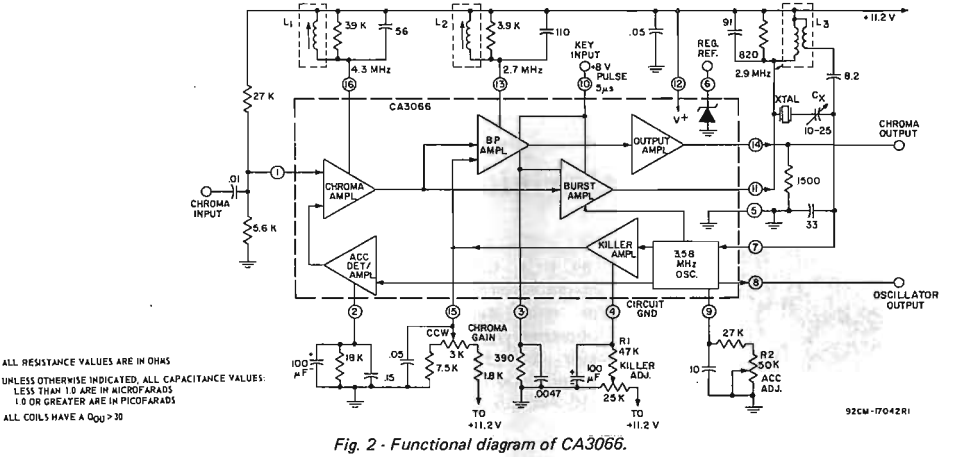


Fig. 2 - Functional diagram of CA3066.

The CA3066 contains substantially all the color processing circuitry exclusive of the tint control and demodulating circuits. The chroma amplifier sections of the CA3066 consist of the chroma and bandpass amplifiers. The chroma amplifier receives the chroma input signal at terminal No. 1. This amplifier is gain controlled by the automatic chroma control (ACC) detector-amplifier. The chroma signal is internally coupled from the output of the chroma amplifier to the input of the chroma bandpass amplifier and burst separator amplifier. The horizontal keying pulse (+8V) is used to gate the burst portion of the chroma signal from the input of the bandpass amplifier to the input of the burst separator amplifier. The bandpass amplifier is gain controlled by the dc chroma gain control and can also be controlled by the killer detector-amplifier. The bandpass amplifier output is internally coupled to the chroma output amplifier stage of the CA3066. The coils of the chroma amplifier and the bandpass amplifier are stagger-tuned to provide a combined typical bandpass of 3.08 to 4.08 MHz. The burst separator amplifier injects the burst signal into the 3.58 MHz oscillator. The oscillator amplitude is dependent on the terminal No. 9 impedance to ground and is also responsive to the burst signal amplitude at terminal No. 11. The ACC detector and killer detector sense the burst level or absence of burst, respectively, by monitoring the oscillators response to the burst injection level. The thresholds for the ACC and killer are independently adjusted by resistors R2 and R1 at terminals No. 9 and No. 4, respectively. The chroma output is at terminal No. 14 and the oscillator output is at terminal No. 8. Terminal No. 6 is a zener diode for use as a regulated voltage reference at 11.9 volts. When the zener reference element is not used, the power supply voltage should be maintained at 11.2 ± 0.5 volts.

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$

Supply Voltages and Currents (see charts below)

Device Dissipation:

Up to $T_A = 70^oC$ . . . . . 600 mW

Above $T_A = 70^oC$ . . . . derate linearly 7.7 mW/^oC

Ambient Temperature Range:

Operating . . . . . –40 to +85 ^oC

Storage . . . . . –65 to +150 ^oC

Lead Temperature (During soldering for 10s max. at not less than 1/32" from package) . . . +265 ^oC

Voltage with respect to Terminal No. 5.

Terminal No.	$V_{min.}$ (volts)	$V_{max.}$ (volts)
6	See Note N1	
7	–	–
8	–	–
9	—	–
10	–5.0	N2
11	0.0	18.0
12	0.0	12.0
13	0.0	15.0
14	–	–
15	0.0	N2
16	0.0	15.0
1	–5.0	5.0
2	–	–
3	–	–
4	–	–

Current

Terminal No.	I_I mA	I_O mA
6	20	0.1
7	5	0.1
8	1	2
9	0.1	2
10	1	0.1
11	10	1
12	50	1
13	10	1
14	0.1	6
15	3	1
16	6	1
1	1	0.1
2	0.1	2
3	0.1	20
4	1	1

N1 Terminal No. 6 is connected to a zener reference element, that, if used, should be biased by a positive voltage through a resistor that limits the current to a value which is less than the maximum current rating of terminal No. 6.

N2 The upper voltage limit cannot exceed the power supply input voltage at terminal 12.

ELECTRICAL CHARACTERISTICS at T_A = 25°C and V^+ = 11.2 V

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST FIG. AND CURVES
Static Characteristics							
Voltages:							
ACC Reference	V_2		–	0.5	–		
Burst-Chroma Ampl. Bias Current Term.	V_3		–	2.9	–		
Killer Reference	V_4		–	1.0	–		
Zener Reg. Reference	V_6		10.6	11.9	12.6	V	4
Oscillator Input	V_7		–	1.4	–		
Oscillator Output	V_8		–	2.35	–		
Balance (ACC Control)	V_9		–	1.65	–		
Chroma Output	V_{14}		–	4.6	–		
Currents:							
Total Supply	I_5		14	24	33		
Burst Separator Output	I_{11}	S_1 Closed	–	6.5	–	mA	
Band-Pass Ampl. Output	I_{13}		–	4.8	–		
Chroma Ampl. Output	I_{16}		–	1.27	–		
Dynamic Characteristics							
Oscillator Output	v_8	v_1 = 0 $v_{p\text{-}p}$ v_1 = 1.25 $v_{p\text{-}p}$	0.8 –	1.2 2.5	– 3.5	$v_{p\text{-}p}$	6
Chroma Output:							
100%	v_{14}	v_1 = 1.25 $v_{p\text{-}p}$	0.5	1.0	–	$v_{p\text{-}p}$	6,5
Killed		v_1 = 0.025 $v_{p\text{-}p}$	–	–	12		
ACC Detector Output	v_2	v_1 = 1.25 $v_{p\text{-}p}$	–	0.9	–	V	6
Small-Signal Input Resistance (Term. No.1)	r_i		–	50	–	kΩ	–
Small-Signal Input Capacitance (Term. No.1)	c_i		–	2.4	–	pF	
Small-Signal Output Impedance (Term. No.14)	r_o		–	250	–	Ω	

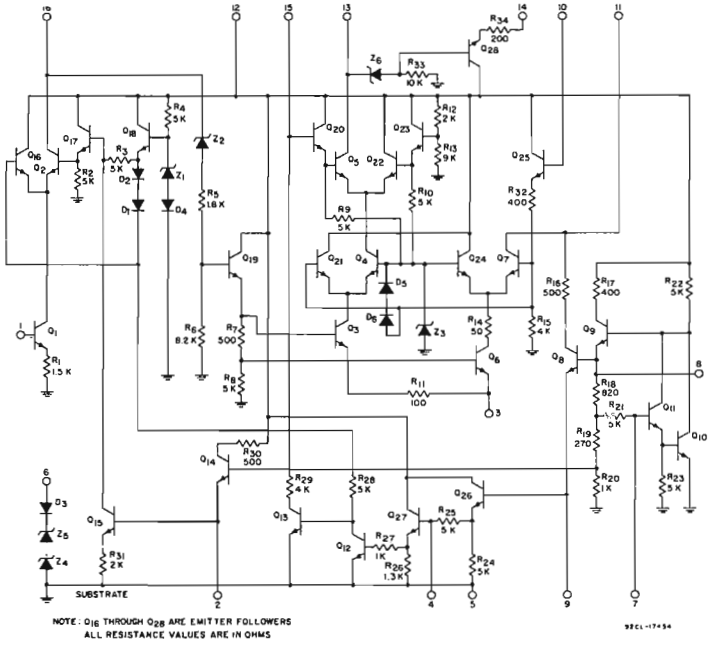


Fig. 3 - CA3066 schematic diagram.

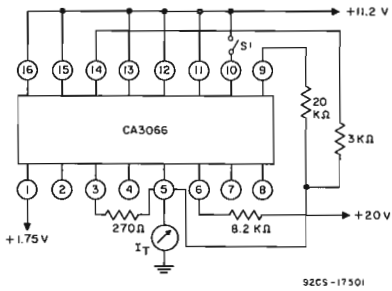


Fig. 4 - Static characteristics test circuit.

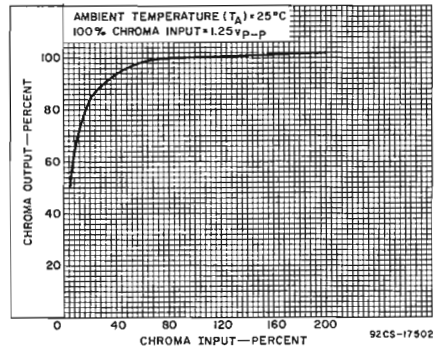


Fig. 5 - Typical ACC characteristic of chroma output vs chroma input.

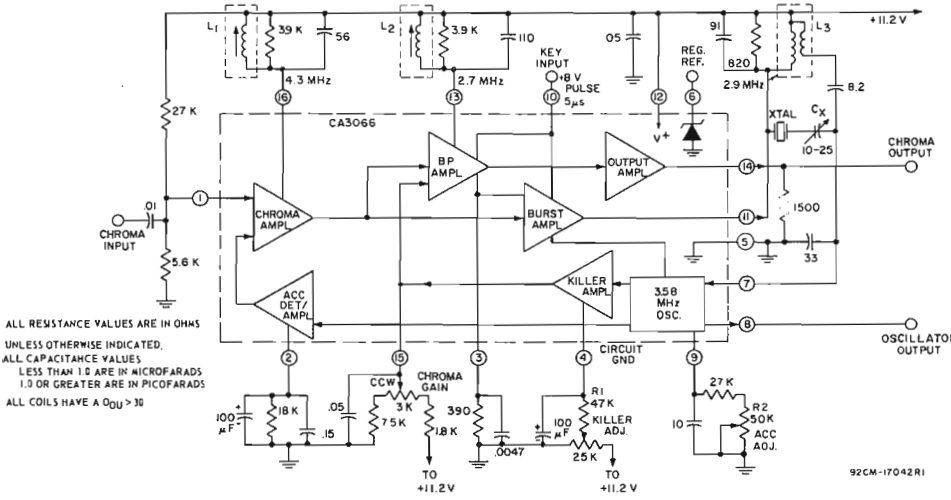


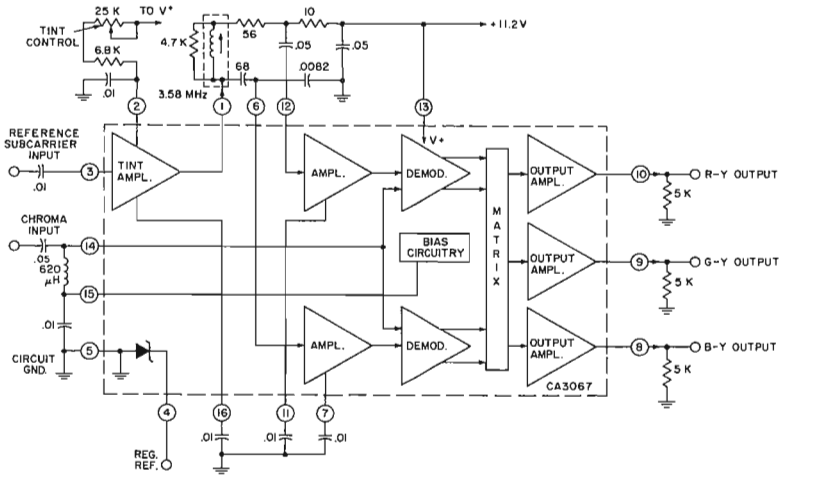
Fig. 6 - Dynamic characteristics test circuit.

DYNAMIC CHARACTERISTICS TEST PROCEDURE

Steps 1, 2, and 3 are performed with no Chroma input ($v_1 = 0$)

1. Adjust ACC potentiometer for $V_2 = +0.65V$.
2. Adjust Killer potentiometer for $V_4 = +1.2V$.
3. Adjust capacitor C_X (crystal trimmer) so that frequency of oscillator is 3.579545 MHz.
4. Unless otherwise noted, the chroma gain control is at maximum gain (fully clockwise).
5. The chroma input test signal is a 52.5 μs "line" at subcarrier frequency, and 10 cycles of burst at 46.5% of the "line" amplitude. The chroma input (v_1) is in peak-to-peak volts of "line" amplitude.
6. The chroma output (v_{14}) is the same as the chroma input (v_1) except that the burst is removed and keying overshoot occurs in the retrace period. The chroma output is in peak-to-peak volts of "line" amplitude.
7. The oscillator output (v_8) is the CW output at terminal No. 8 and is in peak-to-peak volts. Some modulation of oscillation dampening between burst injection is visible.

CA3067 Chroma Demodulator



ALL RESISTANCE VALUES ARE IN OHMS

UNLESS OTHERWISE INDICATED, ALL CAPACITANCE VALUES LESS THAN 1.0 ARE IN MICROFARADS 1.0 OR GREATER ARE IN PICOFARADS

Fig. 7 - Functional diagram of CA3067.

The CA3067 contains the separate functional systems of a dc tint control and a demodulator. The phase shift of the tint amplifier system is accomplished by functional control of the fixed phase signal from the CA3066 oscillator output. This regenerated reference subcarrier is applied to terminal No. 3 and driven differentially into phase shift circuits. The tint adjustment controls the vector addition of phase shifted signals after which a limiting amplifier removes any remaining amplitude modulation. The output of the tint amplifier at terminal No. 1 is phase separated for the required reference subcarrier phase at terminal No. 6 and No. 12 (terminal No. 12 lags terminal No. 6 by approximately 76°). These terminals are inputs to the demodulator drive amplifiers. The demodulators consist of two sets of balanced detectors which receive their reference subcarrier from the demodulator drive amplifiers. The chroma signal input from the CA3066 is applied to terminal No. 14. The chroma signal differentially drives the demodulators. The demodulation components are matrixed and dc-shifted in voltage to give R–Y, G–Y, and B–Y color difference components with close dc balance and proper amplitude ratios. The output amplifiers of the CA3067 are specially designed to meet the low-impedance driving source requirements of the high-level color output amplifiers. A special feature of the CA3067 is R–C filtering of high frequency demodulation components. Terminal No. 4 is a zener diode for use as a regulated voltage reference at 11.9V. When the zener reference element is not used, the power supply should be maintained at +11.2 ±0.5 volts.

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$

Supply Voltages and Currents (see charts below)

Device Dissipation:

Up to $T_A = 70^oC$ . . . . . 600 mW

Above $T_A = 70^oC$ . . . . derate linearly 7.7 mW/°C

Ambient Temperature Range:

Operating . . . . . −40 to +85 °C

Storage . . . . . −65 to +150 °C

Lead Temperature (During soldering for 10s max. at not less than 1/32" from package) . . . +265 °C

Voltage with respect to Terminal No. 5

Terminal No.	$V_{min.}$ (volts)	$V_{max.}$ (volts)
6	0	N2
7	0	N2
8	0	N2
9	0	N2
10	0	N2
11	0	N2
12	0	N2
13	0	12
14	−3	N2
15	0	N2
16	N3	N3
1	0	15
2	0	N2
3	0	5
4	N1	

Current

Terminal No.	I_i (mA)	I_o (mA)
6	3	3
7	3	3
8	20	20
9	20	20
10	20	20
11	3	3
12	3	3
13	50	1
14	1	0.1
15	6	2
16	N3	N3
1	3	3
2	3	0.1
3	3	3
4	20	0.1

N1 Terminal No. 4 is connected to a zener reference element, that, if used, should be biased by a positive voltage through a resistor that limits the current to a value which is less than the maximum current rating of terminal No. 4.

N2 The upper voltage limit cannot exceed the power supply input voltage at terminal 13.

N3 Terminal No. 16 should be bypassed for normal operation.

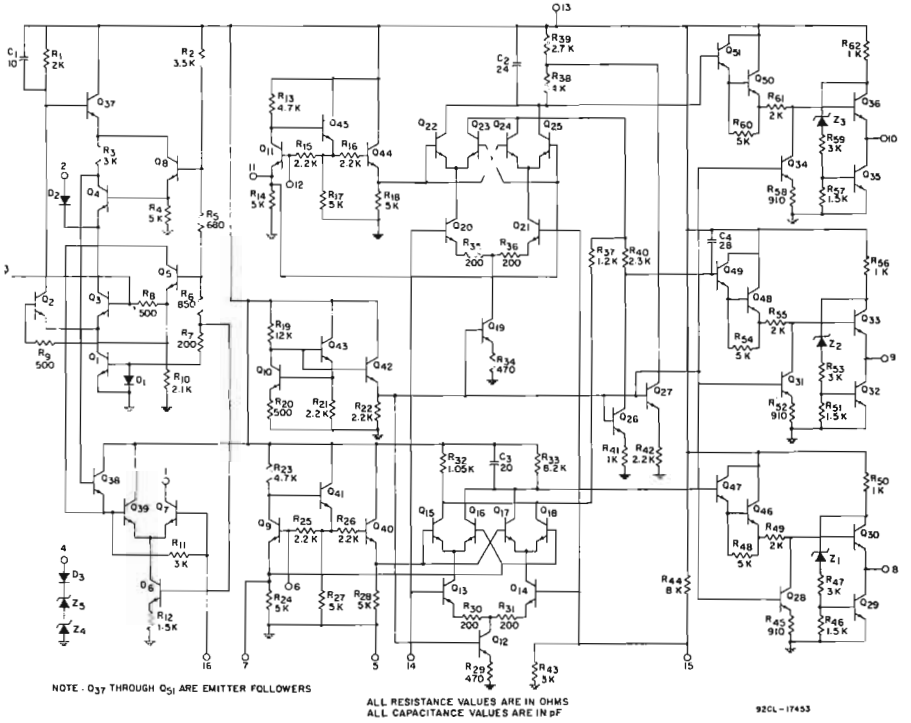


Fig. 8 - CA3067 schematic diagram.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$ and $V^+ = 11.2$ V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST FIG. AND CURVES
Static Characteristics							
Voltages:							
Tint Control Input	V_2	$I_2 = 0.25$ mA	–	3.5	–		
Reference Subcarrier	V_3		–	2.1	–		
Zener Regulator Ref.	V_4		10.6	11.9	12.6	V	9
B–Y, R–Y Oscillator Ref. Inputs	V_6, V_{12}		–	5.7	–		
Balance (B–Y, R–Y)	V_7, V_{11}		–	5.0	–		
B–Y, G–Y, R–Y Outputs	$V_{8, 9, 10}$		4.2	5.0	5.8		9, 11, 12
Difference Outputs*	$\Delta V_8, \Delta V_9, \Delta V_{10}$		–0.3	–	0.3		
Chroma Inputs	V_{14}, V_{15}		–	3.0	–		9
Tint Ampl. Balance	V_{16}		–	4.7	–		
Currents:							
Tint Ampl. Output (min.)	I_1(min.)	$V_{16} = 8$ V	0.16	0.37	–	mA	
Total Supply	$I_1 + I_{13}$		15	24	33		
Dynamic Characteristics							
Tint Amplifier Output							
Sensitivity	V_1	$V_3 = 7$ mV (RMS)	160	250	–	mV (RMS)	
Limiting Knee		$V_3 = 35$mV (RMS)	–	300	–		
Limiting		$V_3 = 350$mV (RMS)	–	–	380		
Tint Ampl. Phase Ref.▲	ϕ_6	$V_3 = 70$mV (RMS)	185	220	235	deg.	
Tint Ampl. Phase Shift‡	$\Delta\phi_6$	$V_3 = 70$mV (RMS)	90	105	–	deg.	
Demodulated Chroma Output:							
R–Y	V_{10}	$V_3 = 70$mV (RMS) $V_{14} = 35$mV (RMS)	150	250	–	V(RMS)	
Ratio of G–Y to R–Y	V_9/V_{10}		0.28	0.36	0.44		
Ratio of B–Y to R–Y	V_8/V_{10}		1.0	1.2	1.4		
Color Difference Output BW at 3.3 dB	$BW_{Diff.}$		450	550	–	kHz	10
Color Difference Outputs (max. input signals):							
R–Y	v_{10}	$V_3 = 70$mV (RMS) $V_{14} = 212$mV (RMS)	–	3.0	–	V_{p-p}	
G–Y	v_9		–	1.1	–		
B–Y	v_8		–	3.6	–		
Small Signal Input Resistance							
Terminal No. 3	r_i		–	550	–	Ω	
Terminal Nos. 6 & 12			–	22	–		
Small Signal Output Resistance Terminal Nos. 8, 9, & 10	r_o		–	5	–		

*$\Delta V_8 = V_8 - \left(\frac{V_8 + V_9 + V_{10}}{3}\right)$, $\Delta V_9 = V_9 - \left(\frac{V_8 + V_9 + V_{10}}{3}\right)$, $\Delta V_{10} = V_{10} - \left(\frac{V_8 + V_9 + V_{10}}{3}\right)$

▲ Terminal No. 3 is phase reference

‡ read phase shift as tint control is varied

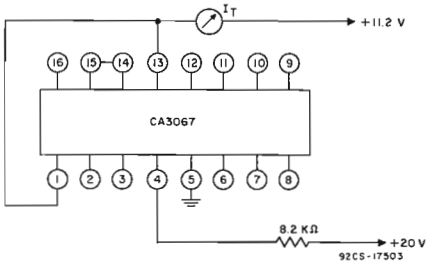


Fig. 9 - Static characteristics test circuit.

DYNAMIC CHARACTERISTICS TEST PROCEDURE

1. The reference subcarrier input (v_3) is a 3.58 MHz CW signal from a 50Ω source.
2. The chroma input (v_{14}) is a 3.53 MHz CW signal from a 50Ω source.
3. Phase and amplitude at terminal Nos. 1, 3, 6 and 12 are measured with a vector voltmeter (HP8405A or equivalent).
4. Signals at terminal Nos. 8, 9, and 10 are measured with an ac voltmeter (HP400E or equivalent) or an oscilloscope.
5. Unless otherwise noted the Tint control is at maximum resistance.

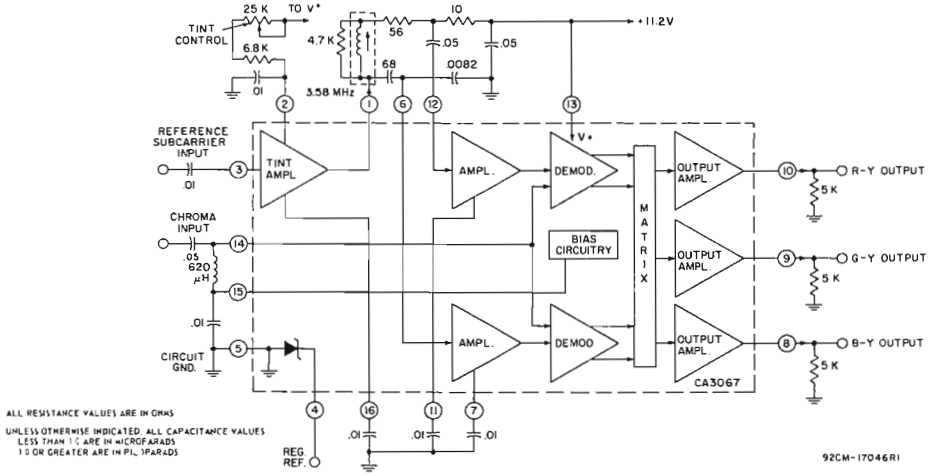


Fig. 10 - Dynamic characteristics test circuit.

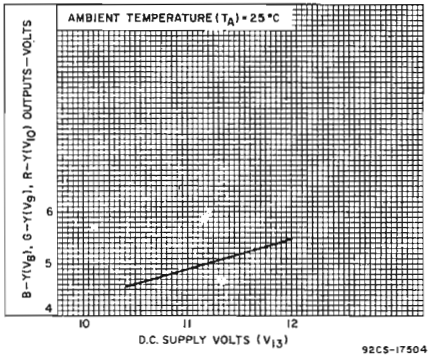


Fig. 11 - DC voltage at color-difference outputs vs supply voltage.

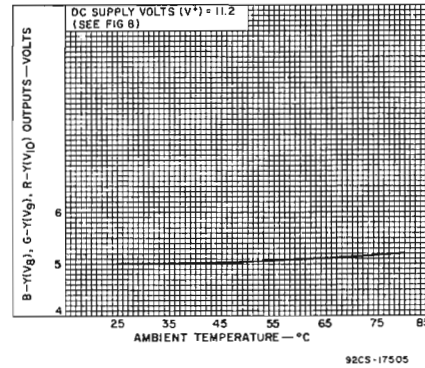


Fig. 12 - Temperature drift of DC voltage at color-difference outputs.

Application Information

TYPICAL CHROMA SYSTEM UTILIZING THE CA3066 AND THE CA3067

CA3066

A typical circuit using the CA3066 is shown in Fig. 13. This circuit is designed for a peak-to-peak chroma input level (v_1) of 1.25 volts, a horizontal keying pulse amplitude (V_{10}) of +8 peak volts, and a regulated supply voltage (V_{12}) of +11.2 volts. The chroma signal should be derived from the 1st or 2nd video amplifier and the luminance should be filtered out before the signal is applied to the CA3066 chroma input at terminal No. 1. For proper switching, the horizontal keying pulse (V_{10}) should be at least +7.5 peak volts but must not exceed the dc supply voltage level (V_{12}) which should be maintained at the recommended value of +11.2V. The dc supply can be externally regulated or the regulation circuit shown in Fig. 13 may be used. An RCA 2N3053 (or equivalent) transistor in an emitter follower configuration is used as a basic regulator in the circuits shown in Figs. 13 or 17. The zener diodes (connected to terminal No. 6 in the CA3066 or terminal No. 4 in the CA3067) are intended as reference-voltage sources for this circuit and may be used separately.

If either the CA3066 or CA3067 can be separately removed from the operating circuit, paralleling the zeners (to establish a regulator reference) is recommended to avoid excessive voltage on the remaining unit. For best voltage tracking and bias stability the zener diode reference element of the CA3066 should be used for the CA3066 supply voltage regulator circuit. The setup adjustments for the circuit of Fig. 13 are the killer (R_1), automatic chroma control (R_2), and oscillator frequency (c_x). The chroma gain control is a dc adjustment that controls the color drive level to the demodulator circuit and is normally a front panel adjustment. The killer and ACC adjustments are initial setup controls to optimize performance. The killer control (R_1) setting adjusts the threshold level at which the chroma bandpass amplifier will be cutoff. This threshold level is normally set at +1.2 V at terminal No. 4. The ACC adjustment (R_2) controls the oscillator loop gain and sets the ACC threshold level at which the chroma output signal ceases to increase linearly with increases in the chroma-input-signal level. When R_2 is properly adjusted, the voltage at terminal No. 2 is +0.6 to +0.7 volts (normally set at +0.65 volts).

The L_1 coil in Fig. 13 has two slugs, one for setting the frequency and another which serves as a Q "spoiler." In this way it is possible to control the tilt of the chroma bandpass frequency response and to compensate for overall-system phase errors. Coils L_1 and L_2 are single-tuned; the transformer T_1 is fix-tuned. The secondary of T_1 provides the reverse phase signal to neutralize the 3.58 MHz crystal and, with the series 12 pF capacitor, provides the correct compensation to terminal No. 7. An adjustable trimmer capacitor in series with the crystal is set for a free-running frequency of 3.579545 MHz ±10 Hz and will, for the typical circuit shown, stay within a nominal drift variation of 30 Hz during warm up.

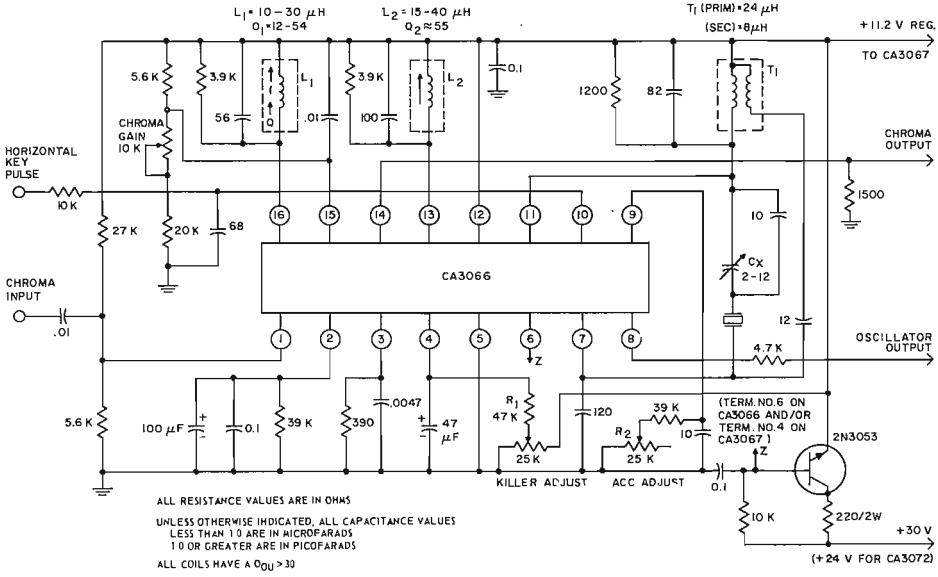


Fig. 13 - CA3066 chroma amplifier-oscillator circuit.

92CM-17506

System performance curves for the CA3066 are shown in Fig. 14. The chroma and oscillator outputs and the killer and ACC reference voltage are plotted as a function of the input chroma signal. Because the killer threshold is a function of the killer reference voltage, a typical curve for the threshold variation is shown in Fig. 15. This curve was generated for various settings of R_1 (killer reference points) with no signal applied to terminal No. 1. At each setting a signal was applied and reduced in magnitude until the bandpass amplifier was cutoff by the killer amplifier. Oscilloscope photographs of the terminal voltage signals and frequency response curves are shown in Fig. 16.

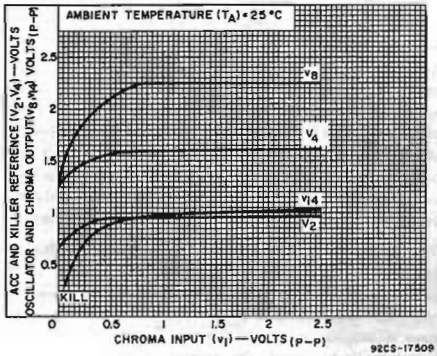


Fig. 14 - Typical chroma system parameters vs NTSC chroma input signal for CA3066.

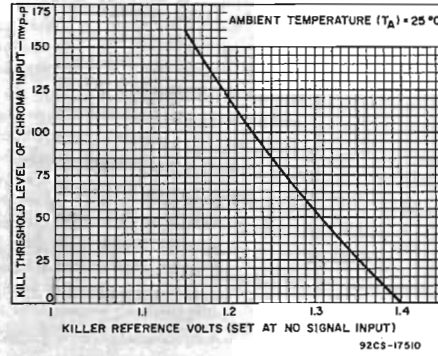
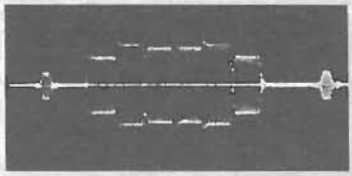


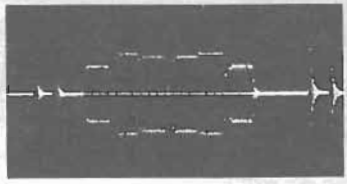
Fig. 15 - Typical killer threshold of chroma input vs killer reference voltage (V_4) using NTSC signal.

Fig. 16 a thru 16 k

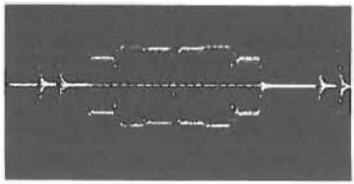
(a) Terminal No. 1.
One horizontal line
1.25 v_{p-p} of NTSC signal at chroma input (v_1 = 1.25 v_{p-p}).



(b) Terminal No. 16.
One horizontal line
0.2 v_{p-p} of chroma amplifier output (v_1 = 1.25 v_{p-p}).

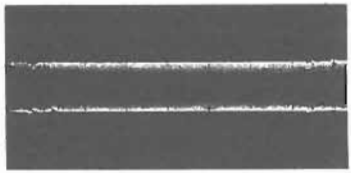


(c) Terminal No 13.
One horizontal line
1.0 v_{p-p} bandpass amplifier output (v_1 = 1.25 v_{p-p}).

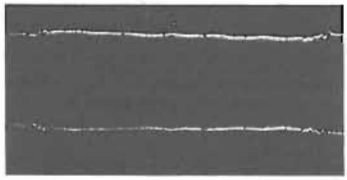


(d) Terminal No. 14.
One horizontal line
1.0 $v_{p\text{-}p}$ of chroma output (v_1 = 1.25 $v_{p\text{-}p}$).

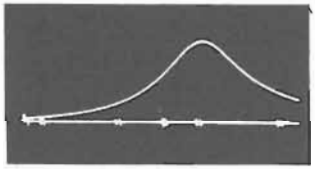
(e) Terminal No. 11.
One horizontal line
2.3 $v_{p\text{-}p}$ of separated burst (v_1 = 1.25 $v_{p\text{-}p}$).



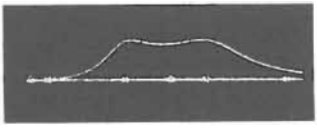
(f) Terminal No. 8.
One horizontal line
1.2 $v_{p\text{-}p}$ of oscillator output with no input signal (v_1 = 0).



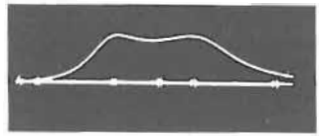
(g) Terminal No. 8.
One horizontal line
2.5 $v_{p\text{-}p}$ of oscillator output (v_1 = 1.25 $v_{p\text{-}p}$).



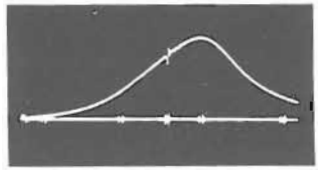
(h) Terminal No. 16.
Frequency response sweep 0.5 MHz/horizontal division peak response at 4.08 MHz (Terminal No. 4 connected through 24 k Ω to +11.2V).



(i) Terminal No. 13.
Frequency response sweep 0.5 MHz/horizontal division (terminal No. 4 connected through 24 k Ω to +11.2V).



(j) Terminal No. 14.
Frequency response sweep 0.5 MHz/horizontal division (terminal No. 4 connected through 24 kΩ to +11.2V).



(k) Terminal No. 11.
Frequency response sweep 0.5 MHz/horizontal division
Terminal No. 4 connected through 24 kΩ to +11.2V
Terminal No. 7 connected through 4.7 kΩ to +11.2V
Terminal No. 10 connected through 10 kΩ to +11.2V

CA3067

The Tint Amplifier-Demodulator, CA3067 is shown in Fig. 17. The oscillator output from Terminal No. 8 of the CA3066 is buffer-connected through a 4.7 KΩ resistor to the reference subcarrier input, Terminal No. 3. The chroma output from the CA3066, available on Terminal No. 14, is connected through a series tuned circuit consisting of a 150 pF capacitor, a 560Ω resistor, and a 47 μH coil to terminal Nos. 14 and 15. Terminal Nos. 14 and 15 are biased through an interconnected choke network to provide a balanced bias to the chroma demodulator drivers Q13 and Q14. If desired, the phase polarity of the output of the CA3067 circuit can be reversed by reversing the input connections at terminal Nos. 14 and 15. The regulated 11.2 V dc supply voltage for the CA3067 is obtained from Terminal No. 12 of the CA3066.

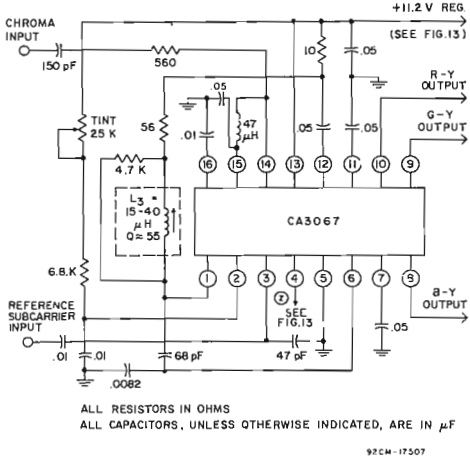


Fig. 17 - CA3067 tint control-chroma demodulator circuit.

In Table I the amplitude and phase values are given with the 0° phase reference at terminal No. 3 and the tint amplifier adjusted to a B–Y signal reference which can be recognized by the waveform on terminal No. 8. Typical terminal voltage values are given for the CA3066 and CA3067 in Table II.

TABLE I – Typical Voltage and Phase Relationships for the CA3067 Tint-Control Amplifier.

TERMINAL NO.	AC VOLTAGE-mv	PHASE ANGLE
3	70	0°
1	200	– 93°
6	1.5	– 67°
12	2.5	–143°

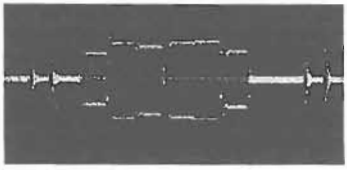
Reference Condition: Tint control centered on B–Y phase at terminal No. 8.

TABLE II – Typical DC Terminal Voltages with no Input Signals for CA3066 and CA3067.

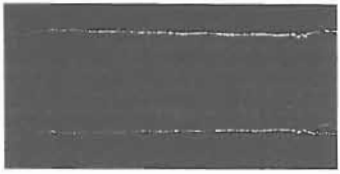
TERMINAL NO.	DC VOLTS	
	CA3066	CA3067
1	1.75	11.2
2	0.68	3.5
3	2.8	2.1
4	1.25	11.9
5	0	0
6	11.9	5.7
7	1.4	5.0
8	2.2	5.0
9	1.9	5.0
10	0	5.0
11	11.2	5.0
12	11.2	5.7
13	11.2	11.2
14	4.6	3.0
15	4.4	3.0
16	11.2	4.8

The demodulation angles are determined by the phase of the reference subcarrier signals at terminal Nos. 6 and 12. These signals are amplified and applied to the demodulators such that their respective demodulated signals are present at terminal Nos. 8 and 10. The phase shift network from terminal No. 1 resolves the signal into two components that are phase separated by 76°. Relative to the terminal No. 6 phase, which is directly represented by the B–Y phase, the terminal No. 12 phase is shifted 180° and the demodulation angle at terminal No. 10 is 180° minus 76° or typically 104°. While the output signals at terminals Nos. 8, 9, and 10 are given as B–Y, G–Y, and R–Y respectively, it is obvious that the phase angles as recognized by the waveforms in the oscilloscope photographs of Fig. 18 are not precisely the NTSC standard representation of color difference signals. The latest developments in color TV picture tubes, such as the 18VANP22, require some phase shift for color correction.

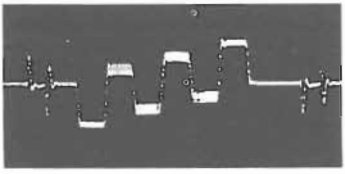
Fig. 18 a thru 18 e.



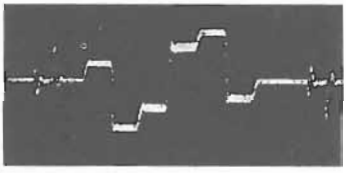
(a) Terminal No. 14.
One horizontal line
0.2 $v_{p\text{-}p}$ chroma input to demodulator.



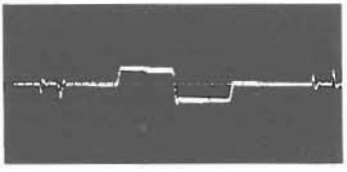
(b) Terminal No. 3.
One horizontal line
0.25 $v_{p\text{-}p}$ oscillator injection input to tint control amplifier.



(c) Terminal No. 8.
One horizontal line
1.0 $v_{p\text{-}p}$ at B–Y output.



(d) Terminal No. 10.
One horizontal line
1.2 $v_{p\text{-}p}$ at R–Y ouyput.



(e) Terminal No. 9.
One horizontal line
0.4 $v_{p\text{-}p}$ at G–Y output.

The tint amplifier of the CA3067 is unique in that all phase shift requirements are satisfied by dc bias control to terminal No. 2. Resistor R1 and capacitor C1 of Fig. 8 provide the basic requirements for a phase shifting of the tint-controlled signal. The reference subcarrier signal at terminal No. 3 is separated 180° by the differential amplifier Q2 and Q3. The output of Q2 is shifted in phase by the R1, C1 time constant. The output of Q3 is directed to a recombination adder junction at the collector of Q4. The tint control determines the Q4 output signal by directing more or less signal to ac ground through diode, D2. The tint-controlled signal is then passed through an amplifier-limiter circuit to terminal No. 1.

The output amplifiers of the CA3067 are very-low-impedance followers that allow for direct coupling to high-level amplifiers. As shown in Figs. 11 and 12, the difference outputs vary linearly with voltage and temperature. Typically, the red and blue difference outputs have a 3-volt peak-to-peak maximum voltage-swing capability with a 5 $k\Omega$ load.

CA3072 Alternate Demodulator Circuit

The circuit shown in Fig. 19 represents an alternate tint amplifier-chroma demodulator. This circuit provides greater color-difference output levels than the CA3067. When the CA3072-2N3933 demodulator and tint amplifier circuit is used in conjunction with the CA3066, +24 volts should be used to provide the proper V^+ for the CA3072. Both the 2N3053 and 2N3933 are typical of the type of transistors that may be used with the CA3066, CA3067, and CA3072 integrated circuits. For complete data information on the RCA types 2N3053, 2N3933, and CA3072, refer to their respective Technical Bulletins.

Construction Information

Fig. 20 is a photograph and template of a circuit board layout for the CA3066 and CA3067 combination. Particular information for most of the components is given in Figs. 13 and 17. Special attention must be given to bypassing at terminal Nos. 2 and 15 in the CA3066. Terminal No. 2 requires a high-Q capacitor (0.1 µF) in parallel with the 100 µF electrolytic bypass. Terminal No. 15 requires bypassing to the power supply lines for best results. To assure complete cutoff at the minimum chroma-gain-control setting, the power supply side of L2 must be well bypassed to ground, and preferably to a common ground point that also includes the 1500-ohm resistor at terminal No. 14 and the CA3067 terminal No. 15 bypass.

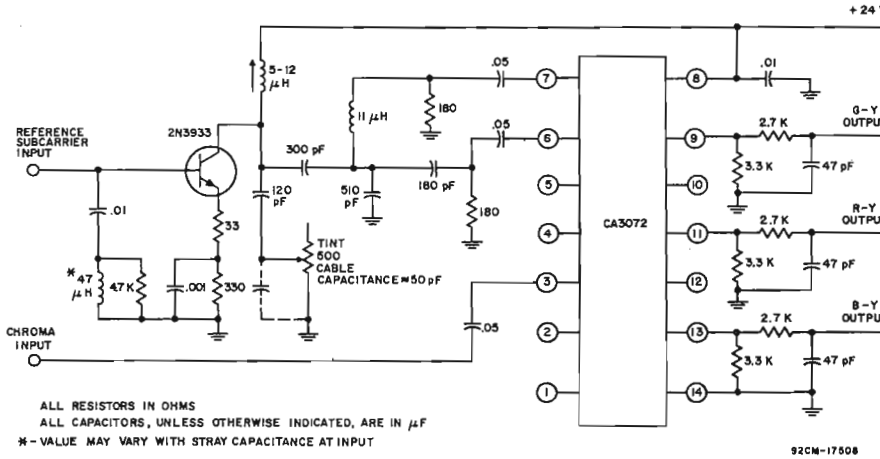


Fig. 19 - CA3072 chroma demodulator with 2N3933 tint control amplifier circuit.

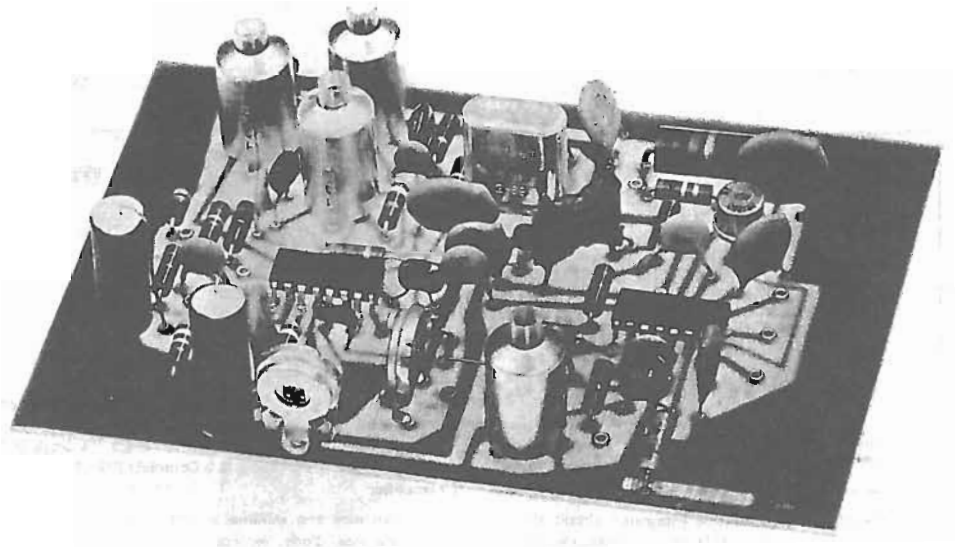
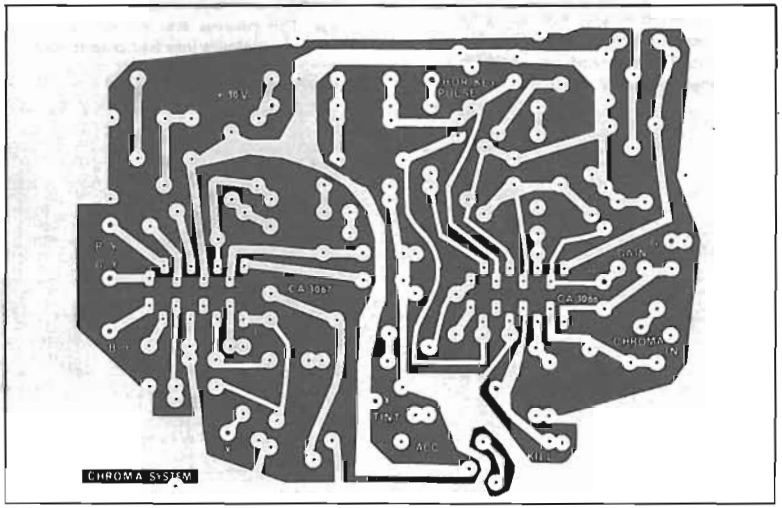


Fig. 20 a - Circuit board layout.



FULL SIZE

Fig. 20 b - Template for circuit board layout

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3068

20-lead quad-in-line plastic package

H-1704

Television Video IF System

FEATURES:

- High-gain wide-band IF amplifier: 75 dB typ. at 45 MHz
- Gain reduction with excellent stability: 50 dB typ. at 45 MHz
- Video detector with linear characteristics
- Video amplifier: 12 dB gain
- Impulse noise limiter
- Keyed AGC with noise immunity circuits
- Delayed AGC for tuner
- Buffered AFT output
- Separate sound IF intercarrier amplification
- Sound carrier detector
- 4.5 MHz sound carrier amplifier
- Isolated zener reference diode for regulated voltage supply
- See ICAN-6303, "A Single IC for the Complete PIX-IF System in TV Receivers"

RCA-CA3068* is a monolithic integrated circuit that incorporates an entire video TV-IF subsystem on a single chip. Innovations in integrated circuit design, in addition to the many active devices and closely matched components utilized in the circuit, make the CA3068 ideally suited for use in color and black-and-white TV receivers.

The primary functions performed by the IF subsystem are video IF amplification, linear detection, video output amplification, AGC from a keyed supply, AGC delay for tuner, sound carrier detection, sound carrier amplification, and a buffered AFT output. The advanced circuit design of the CA3068 also includes secondary functions for improved noise immunity and minimal airplane flutter. An isolated zener reference diode, incorporated in the IC, provides a convenient and economical means for controlling the regulated voltage supply. The inherent wide bandwidth capability (10-70 MHz) and high overall gain (87 dB) make the CA3068 suitable for other AM IF applications whose frequencies range within this bandwidth.

The CA3068 utilizes a unique 20-lead quad-in-line plastic package. This package also includes a wrap-around shield that serves to minimize interlead capacitances.

* Formerly Developmental No. TA5914

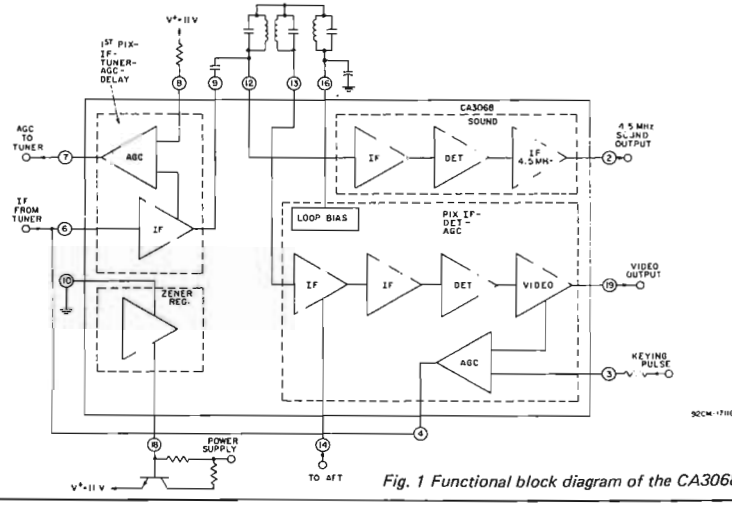


Fig. 1 Functional block diagram of the CA3068.

MAXIMUM RATINGS, *Absolute Maximum Values, at $T_A = 25°C$*

DC Supply Voltage:		
Between Terminals 15 and 5*	11.3	V
Terminal 7 (Collector to ground)	20	V
Terminal 9 (Collector to ground)	20	V
DC Current (into Terminal 18)	2	mA
Device Dissipation:		
Up to $T_A = 60°C$	600	mW
Above $T_A = 60°C$	derate linearly 6.7	mW/°C
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	− 65 to +150	°C
Lead Temperature (During soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

* This rating does not apply when using the internal zener reference in conjunction with the pass transistor.

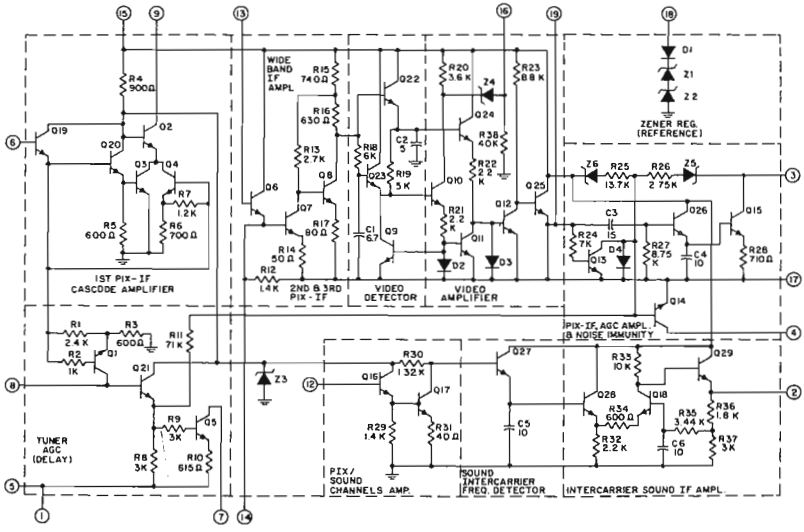


Fig. 2 - CA3068 — Simplified schematic diagram.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	CIRCUIT Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
Static (DC) Characteristics							
Quiescent Circuit Current	I_{15}	–	3	15	–	45	mA
DC Voltages:							
Terminal 2 (Sound)	V_2	–	5	–	6	–	V
Terminal 3 (Keying Input)	V_3	–	3	6.4	–	10	V
Terminal 7 (1) (AGC)	V_7	–	3	16	–	21	V
Terminal 7 (2) (AGC)	V_7	–	4	–	1	–	V
Terminal 8 (AGC Delay)	V_8	–	4	–	4	–	V
Terminal 9 (Cascode Collector)	V_9	–	3	–	8.5	–	V
Terminal 16 (Bias)	V_{16}	–	3	1.1	–	2.3	V
Terminal 18 (Zener)	V_{18}	$V_5 = V_{17} = 0$ V, $I_{18} = 1$ mA	–	10.6	11.9	13.2	V
Terminal 19 (White Level)	V_{19}	–	5	6	–	10	V
Dynamic Characteristics							
Video Sensitivity	e_I	$f_O = 45.75$ MHz, Mod. (AM) = 85% at 400 Hz; Adjust e_I for 4 V_{p-p} at Term. 19	6	40	100	200	μV
Sync. Tip Level Voltage	V_{19}	$f_O = 45.75$ MHz, e_I(CW) = 10 mV	6	0.4	0.8	1.6	V
Automatic Fine Tuning (AFT) Drive Level Voltage	V_{14}		6	–	15	–	mV
Delay Bias Voltage:	V_7						
At e_I = 10 mV		$f_O = 45.75$ MHz, e_I(CW) = 20 mV;	6	16	–	–	V
At e_I = 30 mV		Adjust R_1 for V_7 = 14 V		0.5	–	2	V
3.58 MHz Chroma Output Voltage	V_{19}	$f_O = 45.75$ MHz, e_I(step mod.) = 10 mV; $f_1 = 42.17$ MHz, e_I(step mod.) = 3.33 mV	6	0.5	0.8	—	V
4.5 MHz Sound Output Voltage	V_2	$f_O = 45.75$ MHz, e_I(step mod.) = 10 mV; $f_2 = 41.25$ MHz, e_I(step mod.) = 2.5 mV	6	50	200	—	mV
Parallel Input Impedance:							
Resistance at Term. 6	R_{I-6}	$f_O = 45.75$ MHz Impedance and Admittance measured at bias conditions as developed by circuit shown in Fig. 7	7	4	–	–	kΩ
Capacitance at Term. 6	C_{I-6}			–	2	–	pF
Resistance at Term. 12	R_{I-12}		7	–	4.5	–	kΩ
Capacitance at Term. 12	C_{I-12}			–	4	–	pF
Resistance at Term. 13	R_{I-13}		7	–	5	–	kΩ
Capacitance at Term. 13	C_{I-13}			–	4	–	pF
Parallel Output Impedance:							
Resistance at Term. 9	R_{O-9}		7	30	–	–	kΩ
Capacitance at Term. 9	C_{O-9}			–	3	–	pF
Cascode Transfer Characteristics: Magnitude of Forward Transadmittance	$\|y_f\|$		7	–	50	—	mmho
Reverse Transfer Capacitance	C_r		7	–	0.001	–	pF

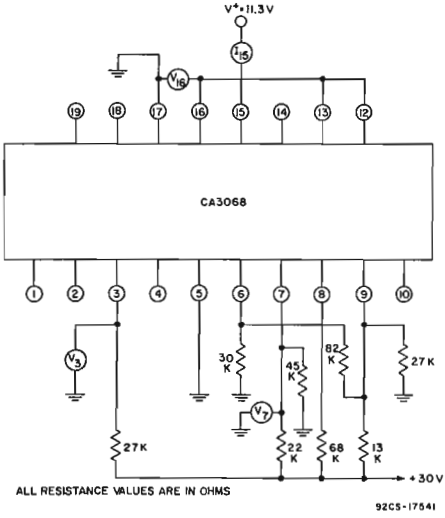


Fig. 3 — Test circuit for measurement of quiescent current (I_{15}), keying terminal voltage (V_3), bias voltage (V_{16}), AGC terminal voltage 1 (V_7), and cascode collector voltage (V_9)

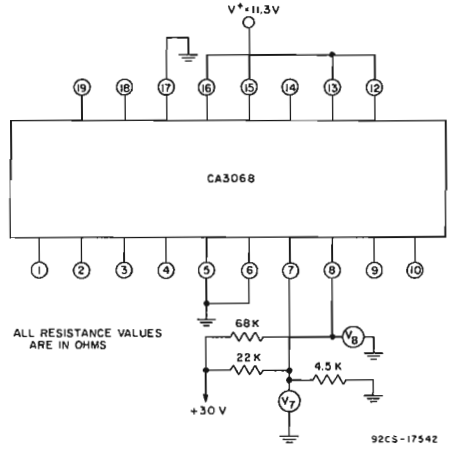


Fig. 4 — Test circuit for measurement of AGC terminal voltage 2 (V_7) and terminal 8 voltage (V_8).

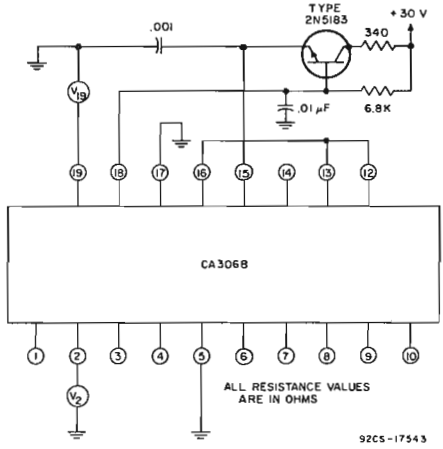
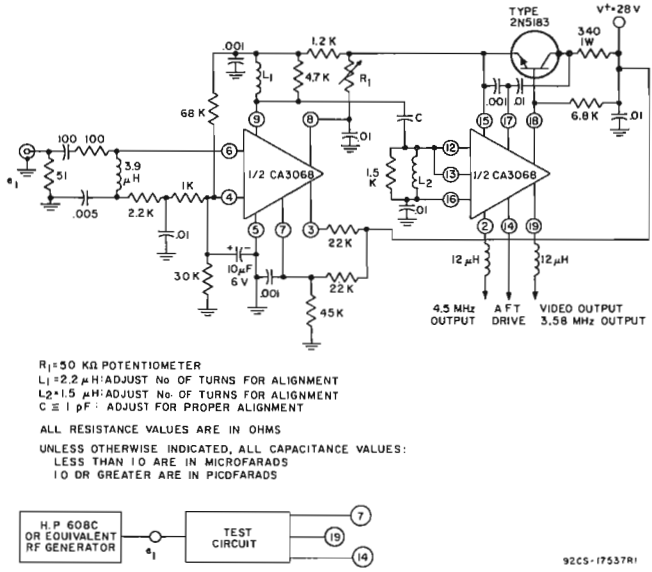
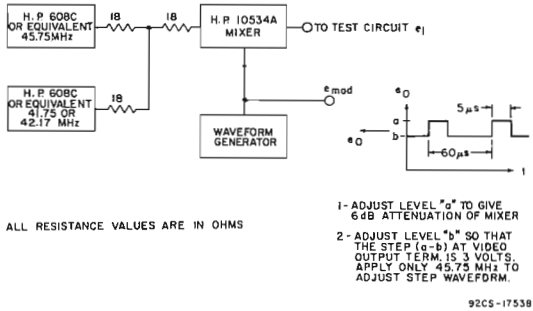


Fig. 5 — Test circuit for measurement of white level (V_{19}) and terminal 2 voltage (V_2).



(a) Test setup for measurement of video sensitivity, sync. tip level, delay bias, AFT drive voltage.



(b) Test setup for measurement of sound and chroma outputs.

Fig. 6 — Typical dynamic test circuit diagrams.

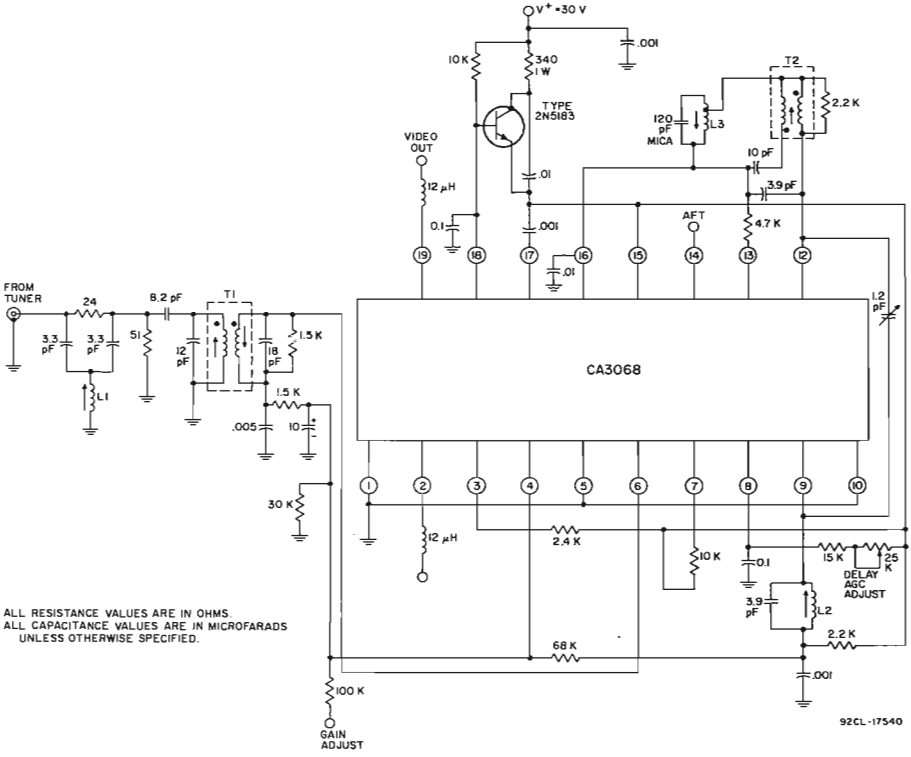


Fig. 7a — Color TV-IF amplifier test circuit.

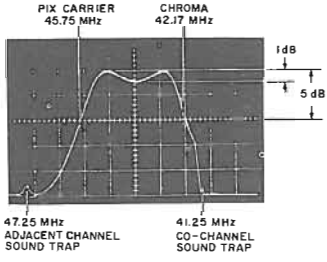


Fig. 7b — Color TV-IF amplifier with associated waveform and test circuit.

Alignment of the IF Amplifier

1. Apply a 2 to 4 mV signal from a sweep generator, Telonic SV13 or equivalent to the input of the IF amplifier.
2. Apply a negative DC supply voltage, to the Gain Adjust Terminal.
3. Set the gain supply voltage to provide a peak-to-peak output of 6 volts.
4. The overall response curve should conform to the waveform shown in Fig. 7b.

A TYPICAL COLOR–TV VIDEO SYSTEM

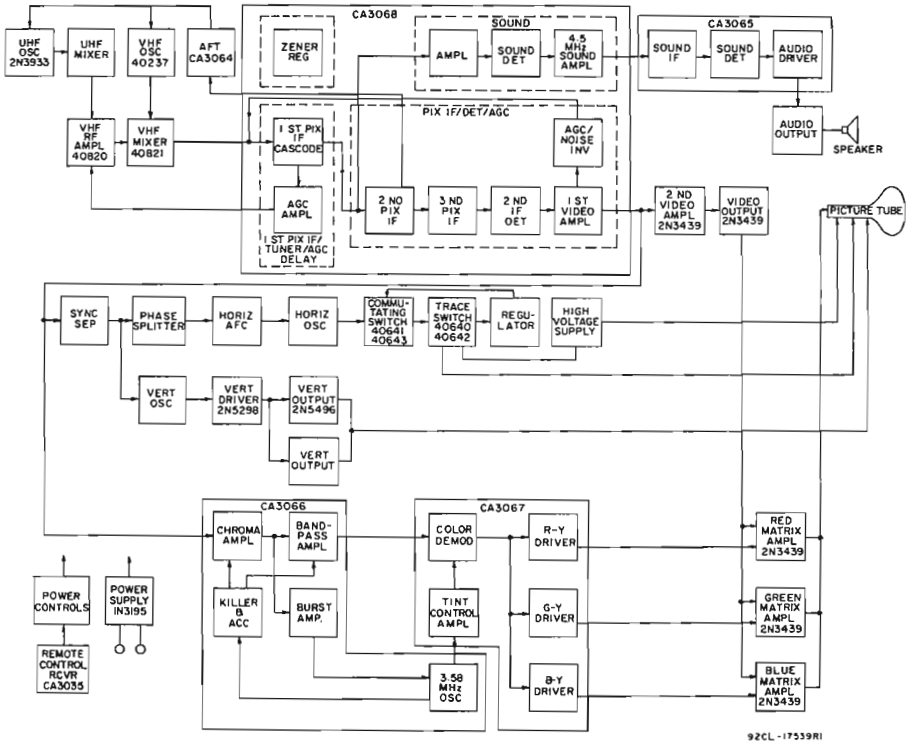


Fig. 8 – Block diagram of a typical color TV receiver utilizing the CA3068.

Application Information

A block diagram of a typical color TV application of the CA3068 is shown in Fig. 8. The input from the TV tuner is applied to the IF cascode amplifier of the IC. The cascode amplifier has a gain reduction of 50 dB typ. and a gain of 35 dB typ. The cascode output is coupled to succeeding stages via the IC lead interconnections. Associated with the cascode amplifier is an AGC delay network that provides gain control for the RF amplifier. This arrangement enables the circuit designer to introduce the desired bandpass-shaping circuitry between the cascode input stages and the remaining IF stages. These IF stages provide an additional gain of 40 dB typ. The output, taken from the emitter of the second IF stage, also provides a buffered AFT signal that is designed to drive the RCA-CA3064 TV Automatic Fine-Tuning IC.

The IF detector circuit provides an extremely linear output signal that is DC coupled to the first video amplifier. The first video amplifier has a voltage gain of 12 dB typ. The detector and video amplifier circuits provide a signal which has in addition to its linear output an extremely sharp limiting characteristic. The maximum video output level is approximately 7 volts peak-to-peak. The sharp limiting action of this circuit clips any signal (e.g. impulse noise) that exceeds this 7-volt value.

The video amplifier also provides a signal which drives a keyed AGC signal. The unique keyed AGC circuits utilize active devices that virtually eliminate noise from interfering with the action of the AGC. A separate sound section provides amplification at intercarrier frequencies, sound carrier detection, and sound carrier amplification. This sound section is designed to drive the RCA-CA3065 TV Sound System IC.

A color IF circuit with associated performance data is shown in Fig. 7. For a more detailed description of the CA3068 and related performance and IF printed circuit construction information, refer to the RCA Application Note ICAN-6544.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA3070, CA3071
CA3072

CA3070
16-Lead Dual-In-Line
Plastic Package
H-1622

CA3071
CA3072
14-Lead Dual-In-Line
Plastic Package
H-1517

Television Chroma System

SYSTEM FEATURES

CA3070

- Voltage Controlled Oscillator
- Keyed APC & ACC Detectors
- DC Hue Control
- Shunt Regulator

CA3071

- ACC Controlled Chroma Amplifier
- DC Chroma Gain Control
- Color Killer
- Amplifier Short-Circuit Protection

CA3072

- Synchronous Detector with Color Difference Matrix
- Emitter-Follower Output Amplifiers with Short-Circuit Protection

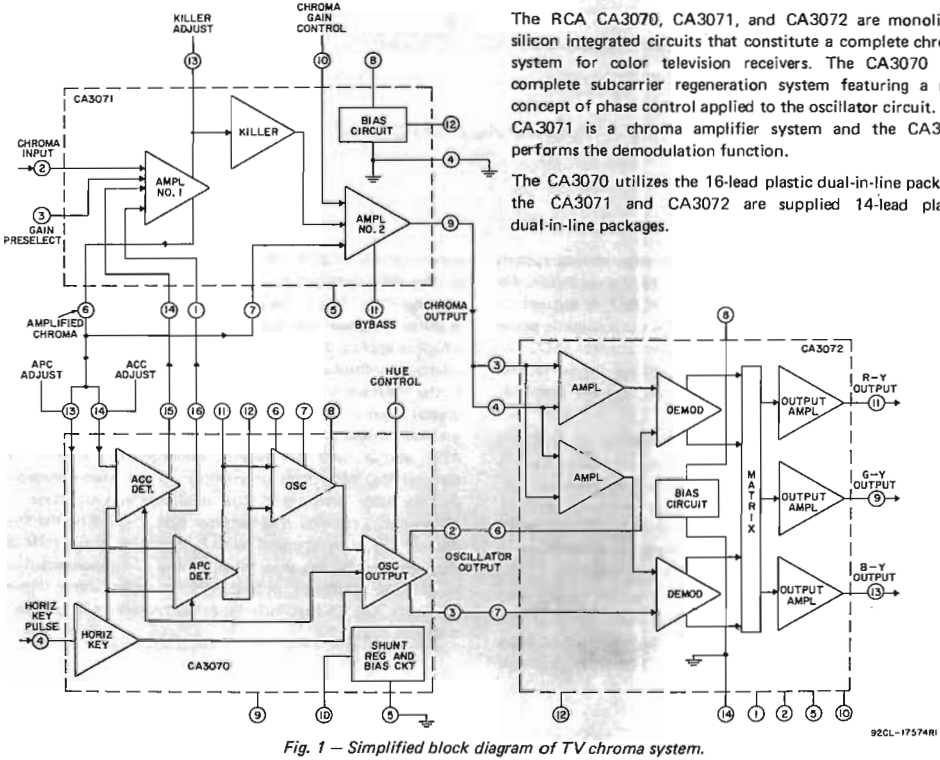


Fig. 1 – Simplified block diagram of TV chroma system.

The RCA CA3070, CA3071, and CA3072 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3070 is a complete subcarrier regeneration system featuring a new concept of phase control applied to the oscillator circuit. The CA3071 is a chroma amplifier system and the CA3072 performs the demodulation function.

The CA3070 utilizes the 16-lead plastic dual-in-line package; the CA3071 and CA3072 are supplied 14-lead plastic dual-in-line packages.

CA3070 Chroma Signal Processor

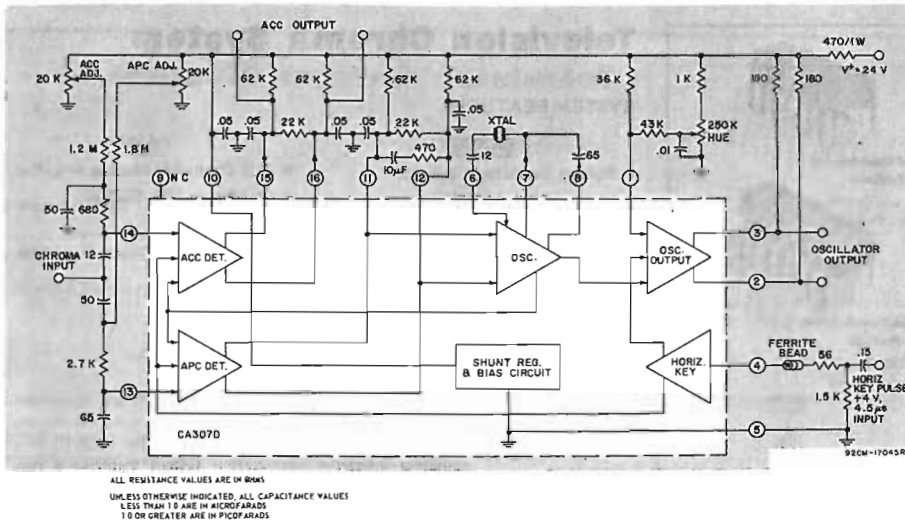


Fig. 2 – Functional diagram of RCA-CA3070.

The CA3070 is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplified chroma signal from the CA3071 is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval.

The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 & 16. This control signal is applied to the input terminal Nos. 1 & 14 of the CA3071. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator.

To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback loop, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The CA3070 includes a shunt regulator to establish a 12-volt dc supply.

MAXIMUM RATINGS, *Absolute Maximum-Values at $T_A = 25°C$*

DC Supply Voltage and Current .....See Charts Below
Device Dissipation:
Up to $T_A = +70°C$ ..... 530 mW
Above $T_A = +70°C$ ... Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:
Operating ..... −40 to +85 °C
Storage ..... −65 to +150 °C
Lead Temperature (During Soldering):
At distance 1/32 in. (3.17 mm) from seating plane for 10 s max. ..... +265 °C

▲ With respect to terminal No.5 and with terminal No. 10 connected through 470Ω to +24 V.
N1 Regulated voltage at terminal No. 10.
N2 Controlled by max. input current.
N3 Limited by dissipation.

Maximum Voltage and Current Ratings at $T_A = +25°C$

Terminal No.	Voltage▲ Min. Volts	Voltage▲ Max. Volts	Current Terminal No.	Current I_I mA	Current I_O mA
1	0	*	1	20	1
2	0	+16	2	—	—
3	0	+16	3	—	—
4	−5	N2	4	20	1
6	—	—	10	N3	1
7	—	—	11	—	—
8	—	—	12	—	—
10	0	N3	13	20	1
11	0	N1	14	20	1
12	0	N1			
13	0	N1			
14	0	N1			
15	0	+16			
16	0	+16			

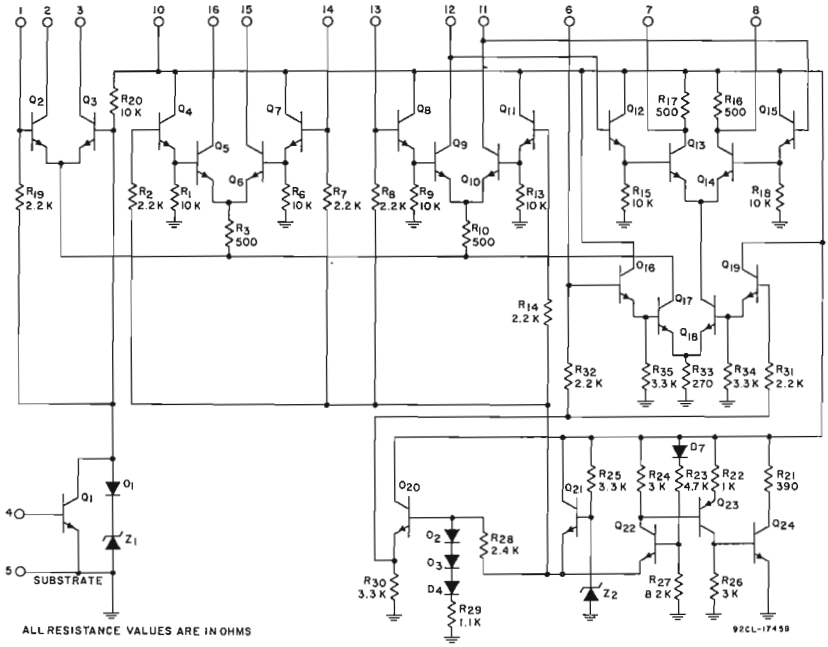


Fig. 3 – Schematic diagram CA3070.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3070 MIN.	LIMITS CA3070 TYP.	LIMITS CA3070 MAX.	UNITS	TEST CIRCUITS FIG.
Static Characteristics							
Voltage:							
Hue Control	V_1	Switch in position 2	6.9	7.7	8.6	V	4c
Oscillator Input	V_6		–	2.8	–	V	4a
APC Input	V_{13}		–	6.5	–	V	4a
Regulator	V_{10}	V^+ = 21 V	11	12.3	13.5	V	4a
Regulator Change	V_{10}	V^+ = 27 V	−0.2	–	+0.2	V	4a
Horizontal Key Input	V_4	I_4 = −10 μA	5	—	—	V	4a
Currents:							
Oscillator Output	I_2		–	5.8	–	mA	4c
APC Output	I_{11}, I_{12}		–	1.45	—	mA	4b
ACC Output	I_{15}, I_{16}		–	1.45	–	mA	4b
Dynamic Characteristics							
Oscillator Outputs:							
Terminal No. 2	V_2	S_1 in position 1	0.75	1.0	–	V_{p-p}	5
Terminal No. 3	V_3	S_1 in position 2	0.75	1.0	–	V_{p-p}	5
ACC Detected Output	V_{16}−V_{15}	S_1 in position 1	115	150	–	mV	5
Oscillator Pull-In Range	–		–	±400	–	Hz	5

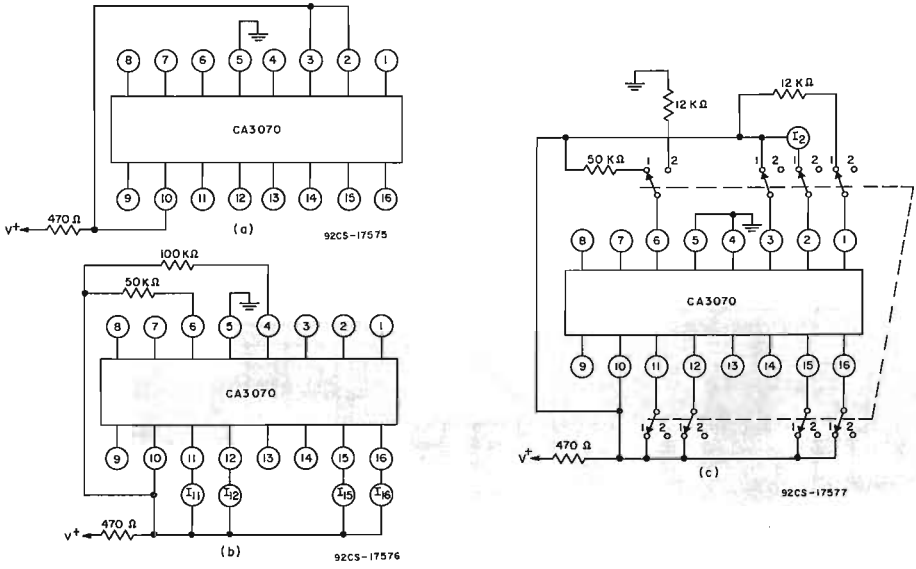


Fig. 4 — Static characteristics test circuits.

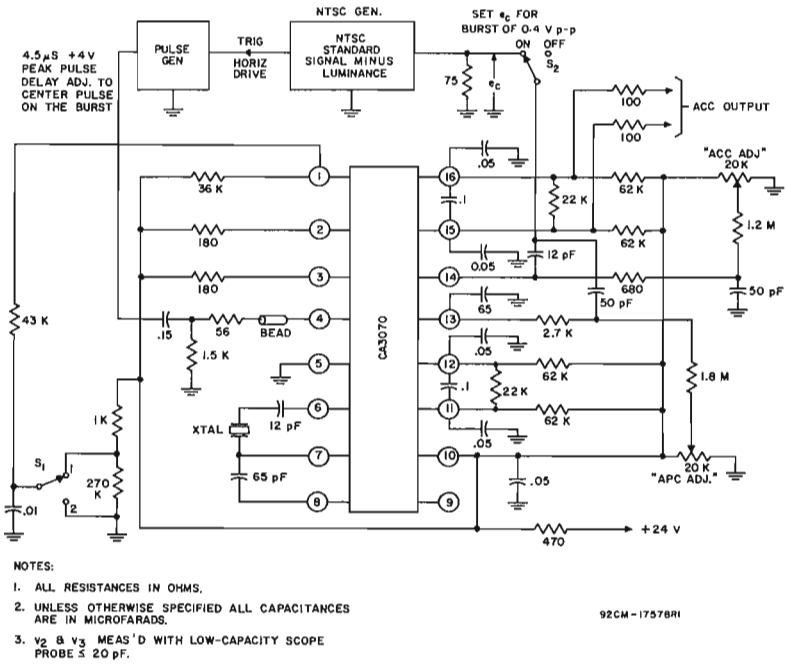


Fig. 5 — CA3070 Dynamic test circuit.

Dynamic Test Initial Adjustments

1. APC ADJUST: With S2 in "OFF" position adjust the "APC ADJ" potentiometer to set oscillator frequency at 3.579545 MHz ±25 Hz. With S1 in position 1 measure frequency at terminal No. 2 output, using crystal probe shown in Fig. 6.
2. ACC ADJUST: With S2 in "OFF" position adjust "ACC ADJ" potentiometer to give an ACC output reading of 0 ±2 mV.

Procedure to Pull-in Range Measurement

1. Set S1 in position 1 and connect the crystal probe to terminal No. 2.
2. Turn S2 to "OFF" and set "APC ADJ." arm to ground.
3. Turn S2 to "ON" and gradually adjust "APC ADJ" until oscillator "locks" as witnessed by a sharp increase in ACC output voltage between terminal Nos. 15 and 16.
4. Turn S2 to "OFF" and adjust capacitor Cp of crystal probe for maximum deflection on Ballantine Meter.
5. Switch Ballantine meter to "Amplifier" position and read oscillator frequency on counter.
6. Repeat steps 2 — 5 with "APC ADJ" arm set to terminal No. 10 instead of to ground.

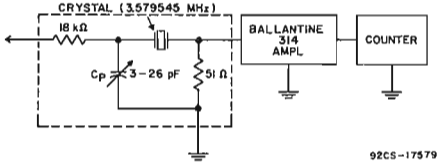


Fig. 6 — Crystal probe for frequency measurements.

CA3071 Chroma Amplifier

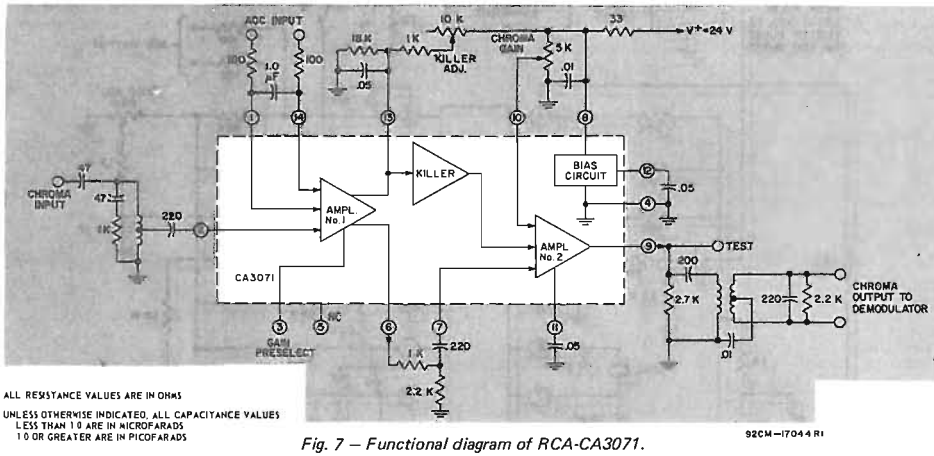


Fig. 7 – Functional diagram of RCA-CA3071.

The CA3071 is a combined two-stage chroma amplifier and functional control circuit. The input signal is received from the video amplifier and applied to terminal No. 2 of the input amplifier stage. The first amplifier stage is part of the ACC system and is controlled by differential adjustment from the ACC input terminal Nos. 1 and 14. The output of the 1st amplifier is directed to terminal No. 6 from where the signal may be applied to the ACC detection system of the CA3070 or an equivalent circuit. The output at terminal No. 6 is also applied to terminal No. 7 which is the input to the 2nd amplifier stage. Another output of the 1st amplifier at terminal No. 13 is directed to the killer adjustment circuit.

The dc voltage level at terminal No. 13 rises as the ACC differential voltage decreases with a reduction in the burst amplitude. At a pre-set condition determined by the killer adjustment resistor the killer circuit is activated and causes the 2nd chroma amplifier stage to be cut off. The 2nd chroma amplifier stage is also gain controlled by the adjustment of dc voltage at terminal No. 10. The output of the 2nd chroma amplifier stage is available at terminal No. 9. The typical output termination circuit that is shown, provides differential chroma drive signal to the demodulator circuit. Both amplifier outputs utilize emitter-followers with short-circuit protection.

MAXIMUM RATINGS, *Absolute Maximum-Values at* $T_A = 25°C$

DC Supply Voltage (Terminal 8 to Terminal 4) ..... 30 VDC

Device Dissipation:

Up to $T_A = +70°C$ ..... 530 mW

Above $T_A = +70°C$ .... Derate Linearly at 6.7 mW/°C

Ambient Temperature Range:

Operating ..... –40 to +85 °C

Storage ..... –65 to +150 °C

Lead Temperature (During Soldering):

At distance 1/32 in (3.17 mm) from seating plane for 10 s max. ..... +265 °C

Maximum Voltage and Current Ratings @ $T_A = +25°C$

Current

Terminal No.	I_I mA	I_O mA
1	5	1.0
2	5	1.0
3	10	10
6	1.0	20
7	5	1.0
9	1.0	20
12	1.0	5
14	5	1.0

Voltage*

Terminal No.	MIN VOLTS	MAX VOLTS
1	–5	+15
2	–5	+5
3	0	+2
6	0	+24
7	–5	+5
8	0	+30
9	0	+24
10	0	+24
11	0	+24
12	0	+20
13	0	+20
14	–5	+15

* With reference to terminal No. 4 and with +24 V on terminal No. 8 except for the rating given for terminal No. 8.

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

CHARACTERISTICS	SYMBOLS (Measure)	SPECIAL TEST CONDITIONS	LIMITS CA3071 MIN.	LIMITS CA3071 TYP.	LIMITS CA3071 MAX.	UNITS	CURVES & TEST CIRCUITS FIG.
Static Characteristics							
Voltages:							
Bias Reference Terminal	V_{12}	S_1 Open, S_2 Open	–	17.3	–	V	8
Ampl. No. 1 Chroma Input	V_2	S_1 Open, S_2 Open	–	1.75	–		
Ampl. No. 1 Chroma Output Balanced	V_6	S_1 Open, S_2 Open	–	20	–		
Unbalanced	V_6	S_1 Open, S_2 Closed	–	13.5	–		
Ampl. No. 2 Chroma Input	V_7	S_1 Open, S_2 Open	–	1.5	–		
Ampl. No. 2 Chroma Output	V_9	S_1 Closed, S_2 Open	–	20.6	–		
Supply Current	I_T	S_1 Open, S_2 Open	17	24.5	31	mA	
Dynamic Characteristics							
Amplifier No. 1 Voltage Gain	A_{V1}	E_g = 30 mV_{RMS} Measure v_6	14	–	–	dB	9
Amplifier No. 2 Voltage Gain	A_{V2}	V_g = 1.0 V (RMS) Measure v_7	–	14	–	dB	
Max. Chroma Output Voltage	v_9		–	2	–	V_{RMS}	13
10% Chroma Gain Control Reference Voltage	$V_8 - V_{10}$	E_g = 50 mV_{RMS}, adjust Chroma Gain Control to Change v_9 to 10% of Maximum Chroma Output	2.1	3.8	6.8	V	9
Output Voltage, Killer Off	v_9	S_1 in Position 2 E_g = 50 mV_{RMS}, adjust "Killer Adjust" for an abrupt decrease in V_g	–	–	12	mV RMS	
Output Voltage, Chroma Off	v_9	E_g = 50 mV_{RMS}, adjust Chroma control to min. Chroma Output	–	–	12	mV RMS	
Bandwidth: Amplifier No. 1	BW		–	12	–	MHz	11, 12
Amplifier No. 2			–	30	–		
Ampl. No. 1 Input Impedance	r_{i1}		–	2	–	kΩ	9
	c_{i1}		–	4	–	pF	
Ampl. No. 1 Output Impedance	r_{o1}		–	85	–	Ω	
Ampl. No. 2 Input Impedance	r_{i2}		–	2.1	–	kΩ	
	c_{i2}		–	3.5	–	pF	
Ampl. No. 2 Output Impedance	r_{o2}		–	85	–	Ω	

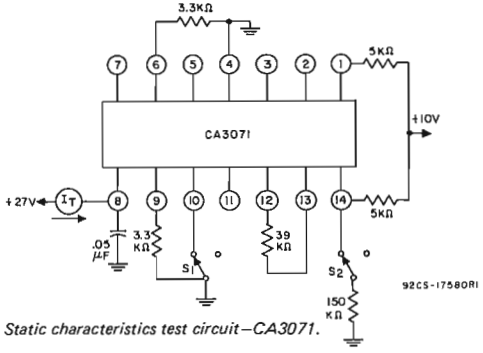


Fig. 8 – Static characteristics test circuit–CA3071.

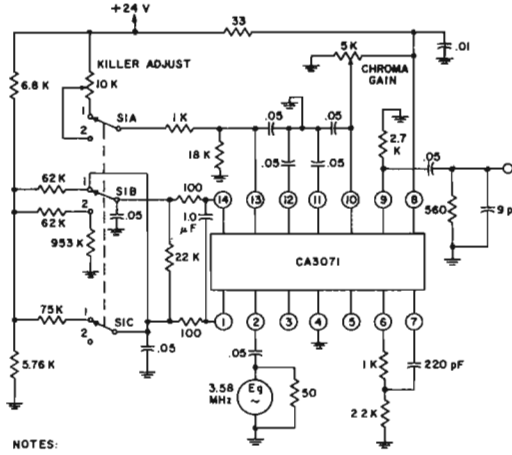


Fig. 9 – Dynamic characteristics circuit-CA3071.

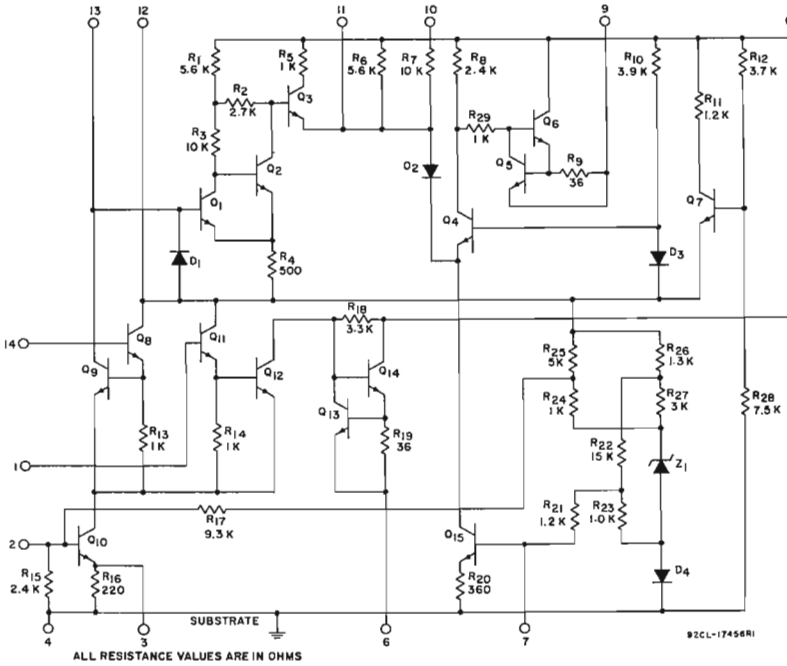


Fig.10—Schematic diagram for CA3071.

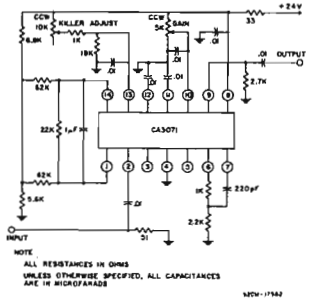


Fig. 11 – CA3071 Wideband amplifier circuit.

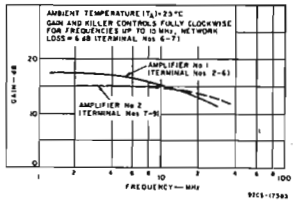


Fig. 12 – Frequency response for wideband amplifier CA3071.

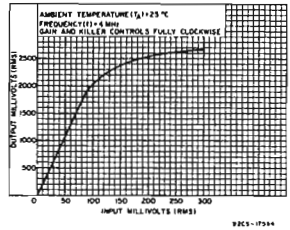


Fig. 13 – Typical CA3071 wideband amplifier linearity

CA3072 Chroma Demodulator

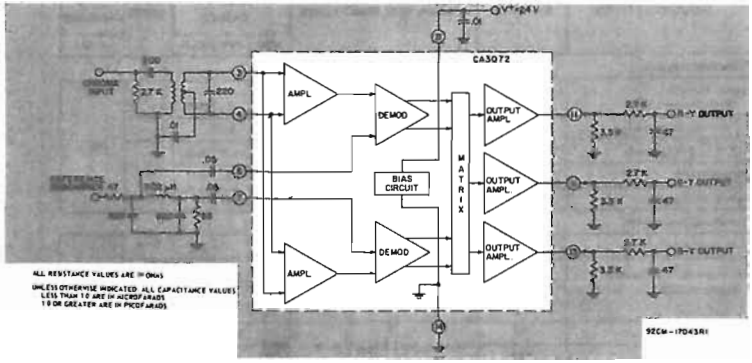


Fig. 14 – Functional diagram of RCA-CA3072.

The CA3072 has two sets of synchronous detectors with matrix circuits to achieve the R-Y, G-Y, and B-Y color difference output signals. The chroma input signal is applied to terminal Nos. 3 and 4 while the oscillator injection signal is applied to terminal Nos. 6 and 7. The color difference signals, after matrix, have a fixed relationship of amplitude and phase nominally equal dc voltage levels. The outputs of the CA3072 are suitable for driving high level color difference or R, G, B output amplifiers. Emitter-follower output stages used to drive the high level color amplifiers have short-circuit protection.

ELECTRICAL CHARACTERISTICS, at T_A = 25° C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3072			UNITS	TEST CIRCUITS
			MIN.	TYP.	MAX.		FIG.
Static Characteristics							
Supply Current With Output Loads	I_T	S_1 Closed	16.5	–	26.5	mA	15
With No Output Loads		S_1 Open	–	9			
G-Y, R-Y, B-Y Outputs	V_9, V_{11}, V_{13}	S_1 Closed	13.2	14.7	15.8	V	
Chroma Inputs	V_3, V_4	S_1 Open	–	3.3	–		
Reference Subcarrier	V_6, V_7	S_1 Open	–	6.2	–		
Dynamic Characteristics							
Demodulator Unbalance	v_9, v_{11}, v_{13}	$V_3 = V_4 = 0$	–	–	0.8	v_{p-p}	16
Maximum Color Difference Output Voltage	v_{13}	$V_3 = V_4 = 0.6\ V_{P-P}$	8.0	–	–	v_{p-p}	
	v_{11}		5.5	–	–		
	v_9		1.2	–	–		
Chroma Input Sensitivity	v_3	Adjust e_c for 5.0 v_{p-p} @ term No. 13 (B-Y)	–	0.2	0.35		
Relative R-Y Output	v_{11}		3.5	–	4.2		
Relative G-Y Output	v_9		0.75	–	1.25		
V_{DC} Difference Between any two Output Terminals	$\lvert V_9 \rvert - \lvert V_{11} \rvert$ $\lvert V_9 \rvert - \lvert V_{13} \rvert$ $\lvert V_{11} \rvert - \lvert V_{13} \rvert$	$e_c = 0$	–	–	0.6	V	
Input Impedance Reference Subcarrier Inputs	r_i6, 7		–	1.7	–	kΩ	
	c_i6, 7		–	6	–	pF	
Input Impedance at Chroma Inputs	r_i3, 4		–	0.95	–	kΩ	
	c_i3, 4		–	6	–	pF	
Output Resistance	r_o9, r_o11, r_o13		–	180	–	Ω	

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25° C*

DC Supply Voltage (Terminal 8 to Terminal 14) ..... 27 V
Reference Input Voltage ..... 5 v_{p-p}
Chroma Input Voltage ..... 5 v_{p-p}
Device Dissipation:
Up to T_A = +70°C ..... 530 mW
Above T_A = +70°C ..... Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:
Operating ..... -40 to +85°C
Storage ..... -65 to +150°C
Lead Temperature (During Soldering):
At distance 1/32 in (3.17 mm) from seating plane for 10 s max ..... +265°C

*With reference to terminal No. 14 and with the voltage between terminal No. 8 and terminal No. 14 at +24 V except as given in rating for terminal No. 8.

Maximum Voltage and Current Ratings at T_A = +25°C

Voltage*

Terminal No.	MIN VOLTS	MAX VOLTS
3	0	+5
4	0	+5
6	0	+12
7	0	+12
8	0	+27
9	0	+20
11	0	+20
13	0	+20

Current

Terminal No.	I_I mA	I_O mA
3	–	–
4	–	–
6	–	–
7	–	–
8	–	–
9	1.0	20
11	1.0	20
13	1.0	20

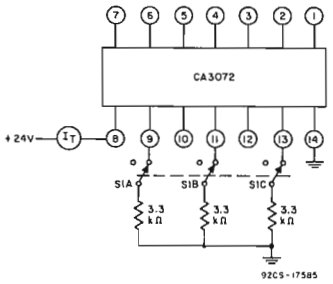


Fig. 15 – Static characteristics test circuit–CA3072.

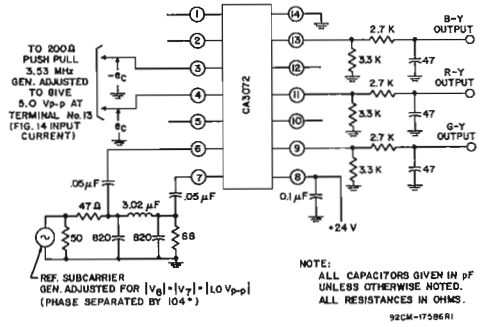


Fig. 16 – Dynamic characteristics test circuit for CA3072.

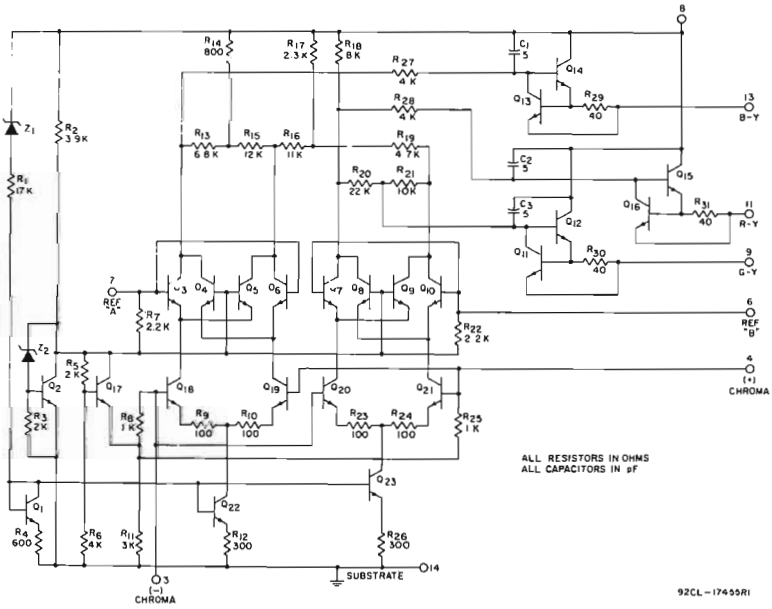


Fig. 17–Schematic diagram for CA3072.

Application Information

TYPICAL APPLICATION CIRCUIT FOR THE CHROMA SYSTEM

The circuit of Fig. 18 is a complete signal processing system for color TV. The RCA types CA3070, CA3071 and CA3072 monolithic integrated circuits are respectively used as the subcarrier regenerator, chroma amplifier, and chroma demodulator.

The input to the system is the chroma signal which may be taken from the first or second video stage and is coupled into the CA3071 chroma amplifier through a bandpass filter. The outputs from the system are the color difference signals which are intended to drive high level amplifiers. Luminance mixing may be external to the picture tube or, the difference signals may be amplified and applied to the picture tube grid or cathode, where they are internally mixed with the luminance signal.

Other input requirements to the system are the power supply voltage of +24 volts and the horizontal keying pulse. The power supply voltage should be maintained within ±3 volts of the recommended value of +24 volts. The total current for the system is approximately 70 milliamperes. The horizontal keying pulse input to the subcarrier regenerator is approximately +4 volts peak and centered on the burst as seen at terminal Nos. 13 and 14 of the CA3070. The pulse width should be maintained as close as possible to the recommended value of 4.5 microseconds.

CA3070 Circuit Operation

The CA3070 circuit as shown in Fig. 3, consists of an oscillator, automatic phase control (APC) detector, automatic chroma control (ACC) detector, gated oscillator output amplifier and a shunt regulator. The shunt regulator provides the necessary bias stability for the 3.579545 MHz oscillator, as well as the bias to all functions of the CA3070 circuit. The regulation voltage is nominally +12 volts as measured at terminal No. 10.

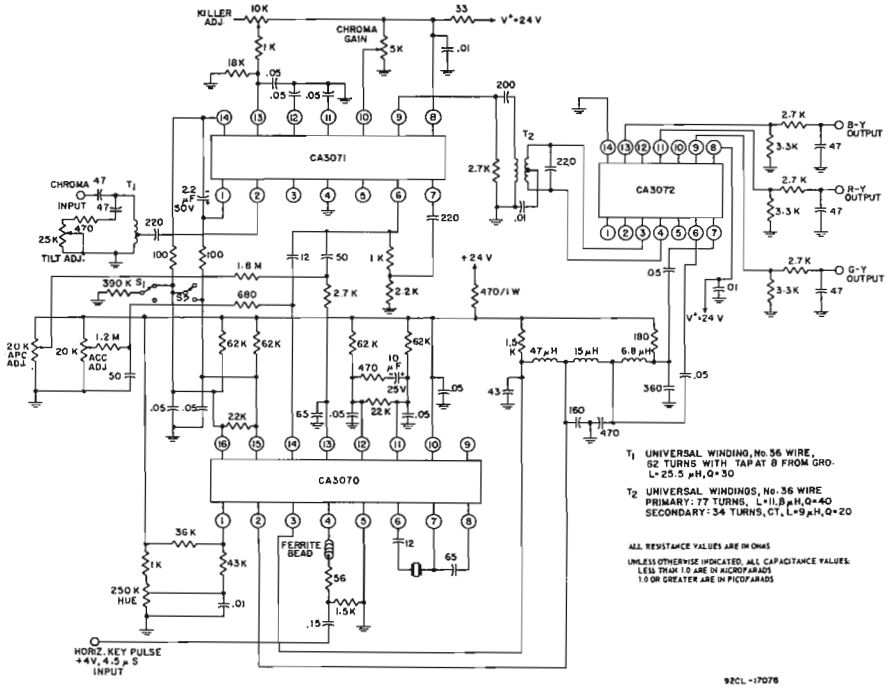


Fig. 18 — Typical chroma system for color-TV receivers utilizing RCA-CA3070, CA3071, and CA3072.

The APC and ACC detectors are synchronous detectors which are keyed by the horizontal input pulse. This form of detection eliminates the need for a burst separator as an individual amplifier stage. When a positive pulse is present at terminal No. 4, the oscillator output is cutoff and the oscillator drive signal is diverted to the APC and ACC detectors. Referring to Fig. 3, the APC detector (Q_9 & Q_{10}) and the ACC detector (Q_5 & Q_6) are emitter driven from the oscillator transistor (Q_{17}), when the oscillator output amplifier transistors (Q_2 & Q_3) are cutoff. The chroma signal is applied to terminal Nos. 13 and 14. There is oscillator current drive to the APC and ACC detectors during the keying interval; burst separation is effectively accomplished by the gating action of the detectors. A further advantage of the keying action is the high gain made possible as a result of the low average current flow of the APC and ACC detectors. High resistor values of 62 kilohms at the detector output terminals provide proper detector bias consistent with the duty factor of the keying pulse. For a wider keying pulse, it is necessary that smaller values of detector load resistors be used.

In the absence of the keying pulse (line period), the resistor, R_{20}, biases the oscillator's output amplifier transistors (Q_2 & Q_3) on by keeping their emitters at a higher potential than the base bias voltages of Q_5, Q_6, Q_9, and Q_{10}. The 3.58 MHz signal is now present at terminal Nos. 2 & 3. Photographs of oscilloscope traces for one line period at the terminal Nos. 1, 2, and 3 are shown in Fig. 19 The effect of the keying pulse is shown in Fig. 19a, and the cutoff of the oscillator output amplifier is shown in Fig. 19b and 19c.

The oscillator section of the CA3070 consists of the loop formed by Q_{18} and the emitter driven differential pair, Q_{13} & Q_{14}. The signal output from terminal Nos. 7 & 8 is coupled through the series tuned crystal circuit back through terminal No. 6 to Q_{16} & Q_{17}. The collector of Q_{17} drives the oscillator output amplifier and the APC & ACC detectors. Q_{17} is emitter coupled to transistor Q_{18}. The oscillator frequency and phase control is accomplished by the differential drive from the APC detector to transistors Q_{12} & Q_{15} which control the balance of Q_{13} & Q_{14}. The resulting phase of the feedback loop is determined by the relative amplitudes of the oscillator output signal at terminal Nos. 7 and 8. The 65 pF capacitor between terminal No. 7 and 8 provides the phase shifting component as the balance of Q_{13} and Q_{14} is varied. In this way the APC detector controls the crystal frequency at which the phase shift is cancelled in the feedback loop.

The controls for the CA3070 subcarrier regenerator circuit are the APC balance, the ACC balance, and the hue control. The hue control is a dc balance adjustment of the oscillator output amplifier transistors Q_2 & Q_3. A phase delay network between the output terminals Nos. 2 & 3 determines the range of the hue control, which for the value shown in Fig. 18, is approximately 90°.

The ACC adjustment sets the initial balance of the ACC drive to the input of the CA3071 in Fig. 18 (terminal Nos. 1 and 14 of the CA3071). The APC is a frequency adjustment of the oscillator through the balance control of the APC detector.

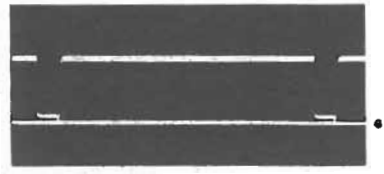


Fig. 19(a) - CA3070 terminal No. 1 7.5 V oscillator "gate off" pulse.

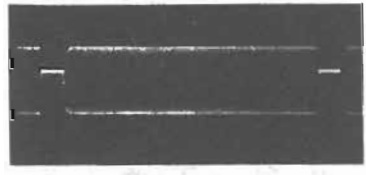


Fig. 19(b) - CA3070 terminal No. 2, 3.5 V_{p-p} oscillator output; one horizontal line, (gated off during burst).

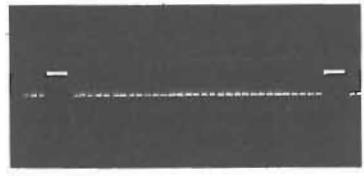


Fig. 19(c) - CA3070 terminal No. 3, 2.0 V_{p-p} oscillator output; one horizontal line, (gated off during burst).

As a setup adjustment, for both the ACC and APC, switch S1 is opened and S2 is closed. The chroma input to the system is removed and the dc voltage at terminal No. 6 of the CA3071 is noted. The switch S2 is then opened and the ACC adjusted to set the voltage at terminal No. 6 to that previously noted. Alternatively, the differential dc voltage at terminal Nos. 15 & 16 of the CA3070 may be set to 0 mV (±2 mV) when S1 and S2 are open, and the CA3071 is removed from the circuit.

With the chroma signal still removed, the APC adjustment sets the frequency of the oscillator to 3.579545 MHz. Due to the gated off interval, a counter will not accurately record the frequency at the oscillator output amplifier terminals. Two simple and accurate methods are as follows: (1) a buffered crystal filter circuit, connected to the oscillator output amplifier terminals will continue to ring and fill the gated off window providing the proper interface to a counter; (2) the other method involves monitoring the demodulated output at the color difference output terminals

of the CA3072. A zero beat signal, at the color difference outputs may be seen on an oscilloscope.

When these adjustments are made, similar oscilloscope traces should be seen as shown in Fig. 20.

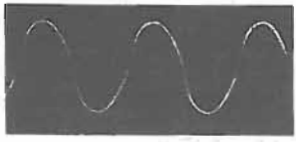


Fig. 20(a) - CA3070 terminal No. 6, oscillator waveform 1.1 $V_{p\text{-}p}$ 3.58 MHz.

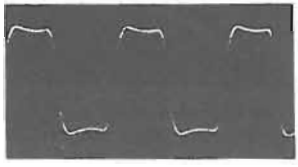


Fig. 20(b) - CA3070 terminal No. 7, oscillator waveform 1.4 $V_{p\text{-}p}$ 3.58 MHz.

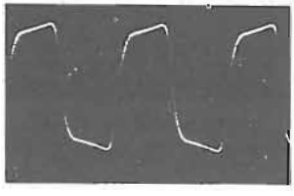


Fig. 20(c) - CA3070 terminal No. 8, oscillator waveform 1.6 $V_{p\text{-}p}$ 3.58 MHz.

CA3071 CIRCUIT OPERATION

The CA3071 is the basic amplifier and control circuit of the chroma system. It contains the gain control functions of the ACC loop, the color killer, and the dc chroma gain control. The CA3071 is a wide band amplifier having two stages of voltage gain. Curves of frequency-response and linearity are shown in Figs. 12 & 13 for the wideband circuits shown in Fig. 11. This is the same basic amplifier as the one in the system shown in Fig. 18 except for the omission of the tuned circuits and the ACC loop connection. The amplifiers have bandwidths of greater than 10 MHz. and are usable well beyond 30 MHz. The signal swing of the wide band amplifier is in excess of 5 $V_{p\text{-}p}$, even with the typical load coupling as shown in Fig. 18. Fig. 21 (a, b and c) show the oscilloscope traces for an NTSC signal at the chroma input. The overall frequency-response curves are shown in Fig. 22.

CA3071 operation is as follows (Refer to Figs. 10 & 18). The input chroma signal is applied to terminal No. 2. This signal is amplified in a cascode differential circuit from Q_{10} to Q_{12}

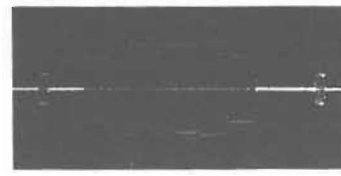


Fig. 21(a) - CA3071 chroma input 1.25 $V_{p\text{-}p}$; one horizontal line of NTSC input signal.

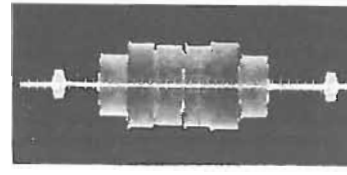


Fig. 21(b) - CA3071 terminal No. 6, amplifier No. 1 chroma output 2.3 $V_{p\text{-}p}$; one horizontal line for 1.25 $V_{p\text{-}p}$ chroma input

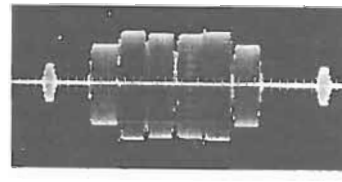


Fig. 21(c) - CA3071 terminal No. 9, amplifier No. 2 chroma output 5.5 $V_{p\text{-}p}$; one horizontal line for 1.25 $V_{p\text{-}p}$ chroma input

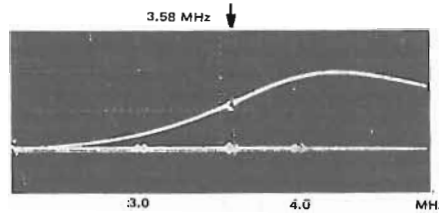


Fig. 22(a) - Frequency response sweep curve between terminal Nos. 2 & 6 for CA3071. f = 250 KHz/div.

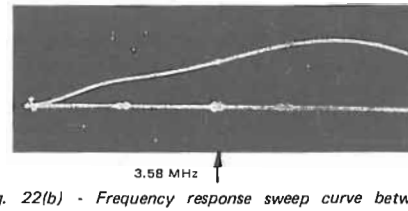


Fig. 22(b) - Frequency response sweep curve between terminal No. 2 of CA3071 and terminal No. 3 of CA3072. f = 250 KHz/div.

and the output is an emitter follower, Q_{14} (Terminal No. 6.) The signal is divided in the Q_9 & Q_{12} differential amplifier, depending on the applied ACC error signal amplitude at terminal Nos. 1 & 14. The ACC error signal is derived from terminal Nos. 15 & 16 of the CA3070 and after filtering, is applied to terminal Nos. 1 & 14 of the CA3071.

At low signal drive, the 390 kilohm resistor at switch S1 (normally closed) unbalances the differential amplifier for high signal gain through Q_{12}. As the burst level at the chroma input increases, the ACC drive changes differentially in a positive direction at terminal No. 14 and a negative direction at terminal No. 14 and a negative direction at terminal No. 1. At strong signal levels the gain is reduced by diverting the balance of ac current in the differential amplifier from Q_{12} to Q_9, which is shunted to ac ground at terminal Nos. 12 and 13. The ACC loop is completed through the chroma signal at terminal No. 6 of the CA3071 to terminal No. 14 (input) of the CA3070. A typical ACC characteristic is shown in Fig. 23.

The chroma signal is buffer connected from terminal No. 6 to terminal No. 7 of the CA3071 and is amplified in the 2nd

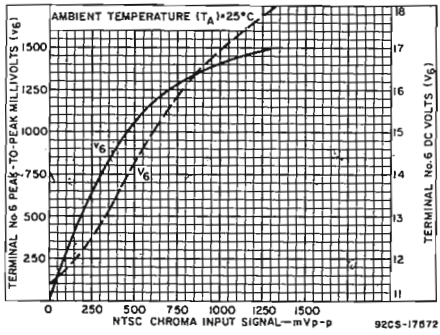


Fig. 23 - Typical ACC characteristics for chroma system of Fig. 18

stage of voltage gain. Both the color killer adjustment and the dc chroma gain control are applied to the 2nd stage to control the chroma output at terminal No. 9. The color killer section of the CA3071 is a Schmitt trigger & amplifier circuit consisting of transistors Q_1, Q_2 and Q_3. Under maximum chroma output conditions, the diode D_2 is reversed biased, and the signal path is through Q_{15}, Q_4 and Q_5 to terminal No. 9. When the color killer circuit is actuated, or the chroma gain control is adjusted to a higher positive voltage at terminal No. 10, the anode voltage of diode D_2 is increased to draw current from the signal path at the emitter of Q_4. This decreases the chroma gain as the potential at terminal No. 10 is increased. When the potential at terminal No. 10 is the same as terminal No. 8, the chroma output at terminal 9 is cutoff.

The color killer circuit provides an abrupt voltage swing at the anode of D_2 to cutoff the chroma output when the Schmitt trigger circuit is forward biased at terminal No. 13. In the circuit of Fig. 18, the color killer adjustment is a resistance divider circuit which establishes the threshold of burst level at which the killer operates the chroma amplifier.

CA3072 CIRCUIT OPERATION

The CA3072 is a chroma demodulator having full color difference signal demodulation capability. The chroma signal is applied to terminal Nos. 3 & 4 and the reference subcarrier signal is applied to terminals Nos. 6 & 7 of the CA3072. The output color difference signals are B-Y at terminal No. 13, R-Y at terminal No. 11, and G-Y at terminal No. 9. The typical level of differential chroma drive required at terminal Nos. 3 & 4 is 400 mV_{p-p}. The amplitude of chroma at terminal No. 6 & 7 is approximately 1.0 volt at 104° relative phase difference which results in a B-Y output amplitude of $5V_{p-p}$. The voltages of the R-Y & G-Y outputs are at 3.8 and 1.0 V_{p-p} respectively, when there is $5V_{p-p}$ output at B-Y. These comparative signals are based upon a complete phase rotation of the chroma relative to the subcarrier signal reference. The relative demodulation phase and amplitude ratios of the Fig. 18 circuit are shown in the oscilloscope trace photographs of Fig. 24. Using the hue control setting for B-Y phase at the B-Y output, the G-Y color-difference signal is approximately −104° and the R-Y color-difference signal is approximately +106°. Since the amplitude ratios are a function of the applied signal phase relationship, the NTSC color difference output signals are shown here primarily for phase reference conditions.

Fig. 24(a) - CA3072 - terminal No. 3 or 4, chroma input signal, 220 mV_{p-p}, one horizontal line

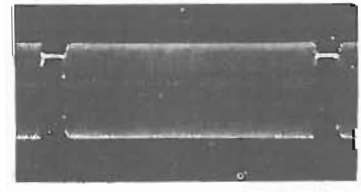


Fig. 24(b) - CA3072 - terminal No. 6 or 7, reference subcarrier 1.2 V_{p-p}, one horizontal line

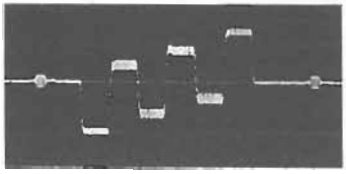


Fig. 24(c) - CA3072 terminal No. 13, 4.8 v_{p-p} B-Y output, one horizontal line

Fig. 24(d) - CA3072 - terminal No. 9, 1.2 v_{p-p} G-Y output, one horizontal line

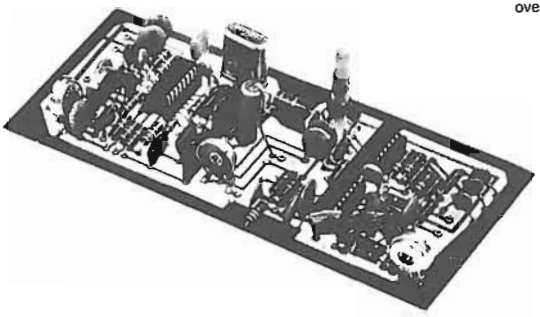


Fig. 25 (a) - Circuit layout and template (printed circuit board) for TV chroma system CA3070, CA3071, and CA3072.

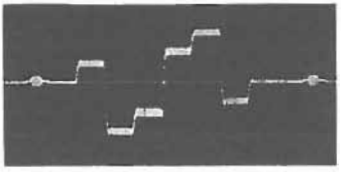


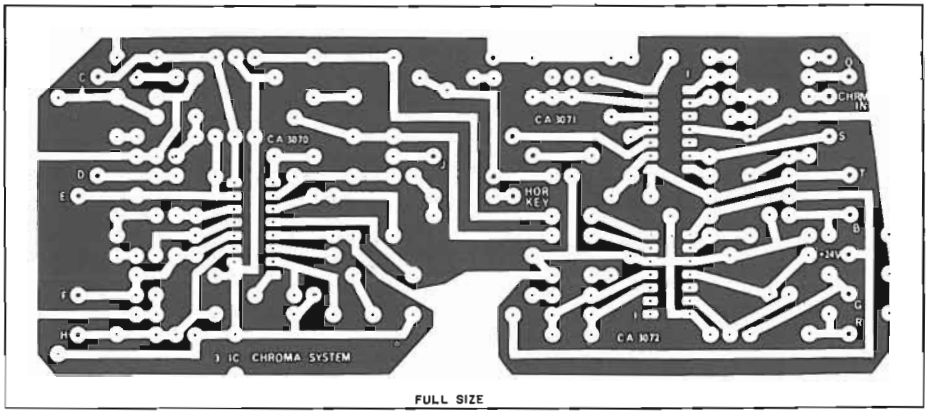
Fig. 24(e) - CA3072 - terminal No. 11, 5.2 v_{p-p} R-Y output, one horizontal line

CHROMA SYSTEM CONSTRUCTION

Fig. 25 shows the complete CA3070, CA3071 and CA3072 chroma system in the Fig. 18 circuit. Table I lists the dc terminal voltages for the system. The chroma gain and hue controls, as well as the switches S1 and S2 are removed. The template circuit board layout is also shown for duplication purposes. It should be noted that a few component values are modified in Fig. 18 from the dynamic circuit values of the data sheet. These are necessary for system matching and overall filter requirements.

TABLE 1 TYPICAL CHROMA SYSTEM TERMINAL DC VOLTAGES (NO SIGNAL INPUT)

TERMINAL No.	DC VOLTS		
	CA3070	CA3071	CA3072
1	7.6	7.3	–
2	11.5	1.7	–
3	11.5	–	3.3
4	−1.7	0	3.3
5	0	–	–
6	2.8	11.4	5.9
7	11.2	1.4	5.9
8	11.2	23.0	24.0
9	–	VARIABLE	14.7
10	12.0	VARIABLE	–
11	7.8	VARIABLE	14.7
12	7.8	15.0	–
13	6.7	VARIABLE	14.7
14	6.7	7.1	0
15	7.3	–	–
16	7.1	–	–



FULL SIZE

(b) – Printed circuit board template.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3075

14-lead dual-in-line plastic package, leads in quad-formed arrangement.

H-1596

FM IF Amplifier - Limiter, Detector, and Audio Preamplifier

For FM IF Amplifier Applications Up To 20 MHz In Communications Receivers And High-Fidelity Receivers

Features:

- Good sensitivity: Input limiting voltage (knee) = 250 μV typ. at 10.7 MHz
- Excellent AM rejection: 55 dB typ. at 10.7 MHz
- Internal Zener diode regulation for the IF amplifier section
- Low harmonic distortion
- Differential peak detection: Permits simplified single-coil tuning
- Audio preamplifier voltage gain: 21 dB typ.
- Minimum number of external parts required

RCA CA3075 is an integrated circuit which provides, in a single monolithic chip, an FM IF subsystem for Communications and High-Fidelity Receivers. This device, shown in the schematic diagram (Fig. 2), consists of a multistage IF amplifier-limiter section with a Zener regulated power supply, an FM detector stage, and an AF preamplifier section. A typical application of the CA3075, in FM receiver circuits, is shown in the block diagram (Fig. 1).

The three-stage, emitter-follower-coupled IF amplifier section provides a 60-dB typ. voltage gain at an operating frequency of 10.7 MHz and features, because of its transistor constant-current sink, an output stage with exceptionally good limiting characteristics.

The FM detector section, which utilizes a differential-peak-detection circuit, requires only a single coil in the associated outboard detector circuit; hence, tuning the detector circuit is a simple procedure.

The audio preamplifier circuit provides a 21-dB voltage gain with low impedance output for driving subsequent audio amplifier stages.

The CA3075 utilizes a 14-lead dual-in-line plastic package with leads in a special quad-formed arrangement.

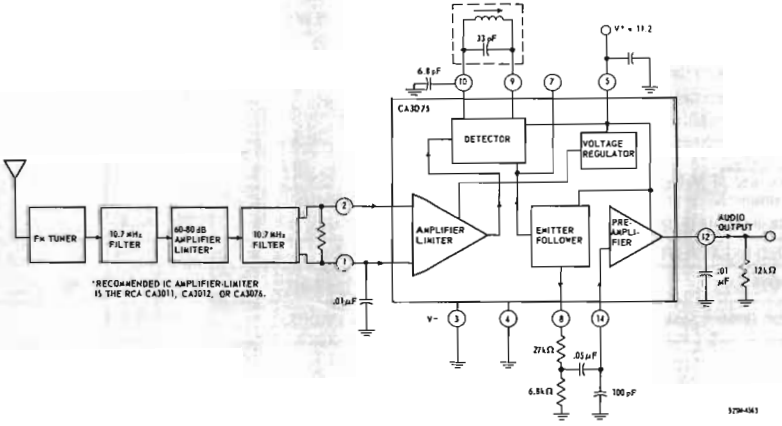


Fig. 1 - Block diagram of typical FM receiver utilizing the CA3075

MAXIMUM RATINGS, *Absolute-Maximum Values at* T_A = 25°C

DC Supply Voltage [between Terminals 5 (V^+) and 3 (V^-)]	12.5	V
DC Current (into Terminal 5)	30	mA
Device Dissipation:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During soldering for 10 s max.)	+265	°C

ELECTRICAL CHARACTERISTICS at T_A = 25° C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CIRCUIT FIG. NO.
Static Characteristics							
DC Voltage:							
At Terminal 7	V_7	V^+ = 11.2 V	–	6.1	–	V	6
At Terminal 8	V_8		–	5.4	–	V	
At Terminal 12	V_{12}		–	5.2	–	V	
DC Current (into Terminal 5):							
At V^+ = 8.5 V	I_5	–	8.5	15	–	mA	6
At V^+ = 11.2 V			–	17.5	–	mA	
At V^+ = 12.5 V			–	19	29	mA	
Dynamic Characteristics at V^+ = 11.2							
IF AMPLIFIER Input Limiting Voltage (knee, − 3 dB point)	V_I(lim)	f_0 = 10.7 MHz f(Modulation) = 400 Hz Deviation = ±75 kHz	–	250	600	μV	3
AM Rejection	AMR	f_0 = 10.7 MHz f(Modulation) = 400 Hz FM: Deviation = ±75 kHz AM: Modulation = 30%	–	55	–	dB	5
Input Impedance Components:							
Parallel Resistance	R_I	f_0 = 10.7 MHz	–	4.5	–	kΩ	–
Parallel Capacitance	C_I	V_{IN} = 10 mV RMS	–	4.5	–	pF	
DETECTOR Recovered AF Voltage (at Terminal 12)	V_O(AF)	f_0 = 10.7 MHz f(Modulation) = 400 Hz	–	1.5	–	V	3
Total Harmonic Distortion	THD	Deviation = ± 75 kHz	–	1	2	%	
AUDIO PREAMPLIFIER Voltage Gain	A(AF)	V_{IN} = 100 mV, f_0 = 400 Hz	–	21	–	dB	4
Total Harmonic Distortion	THD	V_{OUT} = 2 V, f_0 = 400 Hz	–	1.5	5	%	4

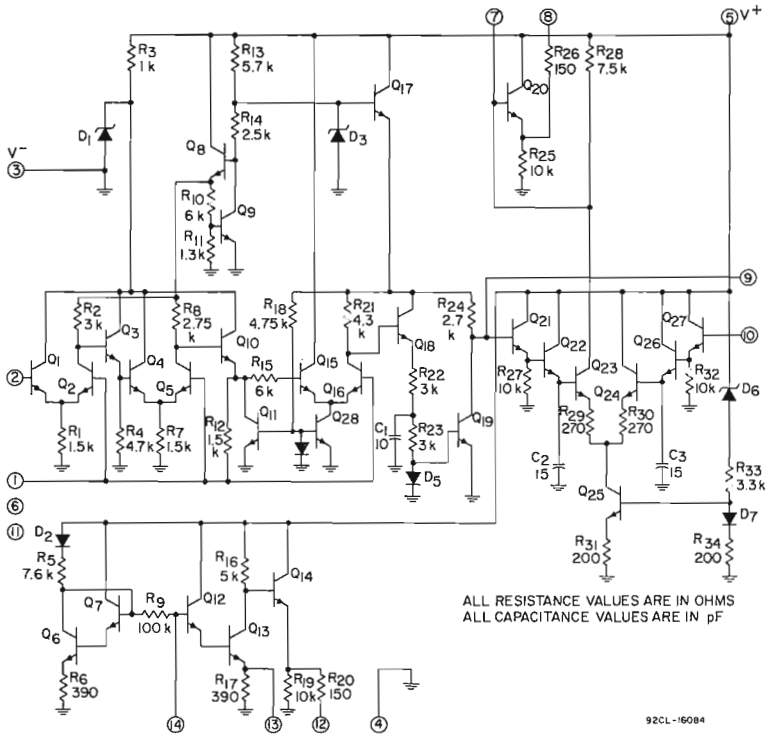


Fig. 2 - Schematic diagram of CA3075

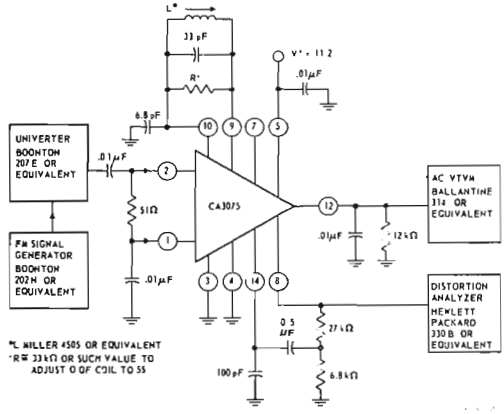


Fig.3 — Test Circuit for input limiting voltage, recovered AF voltage, and total harmonic distortion

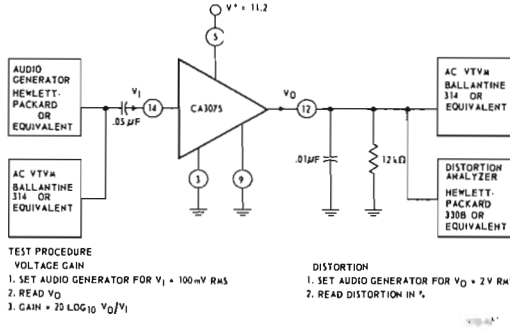


Fig.4 — Test circuit for audio preamplifier voltage gain and total harmonic distortion

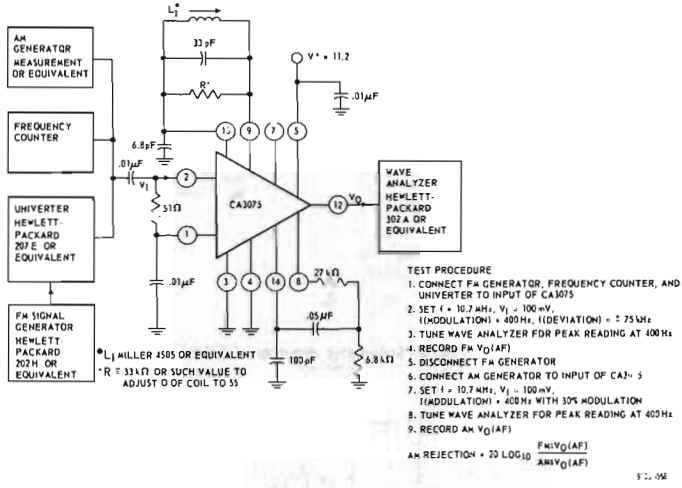


Fig.5 — Test circuit for AM rejection

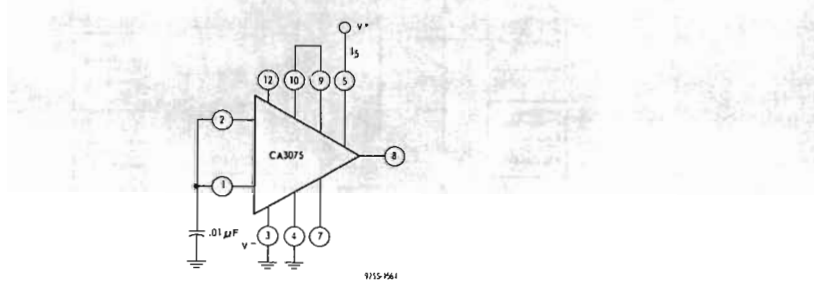


Fig. 6- Test circuit for static characteristics

RCA Solid State Division

Linear Integrated Circuits

CA3076

8-Lead TO-5

High-Gain Wide-Band IF Amplifier-Limiter

For FM IF Amplifier Applications in Communications Receivers

Features:

- exceptionally good sensitivity: input limiting voltage (knee) = 50 μV typ. at 10.7 MHz
- high gain: 80 dB with 2-kilohm load
- internal voltage supply regulator
- wide frequency capability: > 20 MHz

RCA CA3076, monolithic integrated circuit, is a high-gain wide-band amplifier-limiter for use in the IF sections of Communications and High-Fidelity FM Receivers. The CA3076, shown in the schematic diagram (Fig. 2), consists of a four stage IF amplifier-limiter section with a voltage regulator section. A typical application of the CA3076 in FM receiver circuits is shown in the block diagram (Fig. 1).

The four-stage emitter-follower-coupled IF amplifier section provides an 80-dB voltage gain with a 2-kilohm load at a frequency of 10.7 MHz. The output stage has exceptionally good limiting characteristics because of its transistor constant-current sink. The voltage regulator section provides zener-regulated, decoupled voltages for the IF amplifier.

The CA3076 utilizes an hermetically-sealed 8-lead TO-5 package.

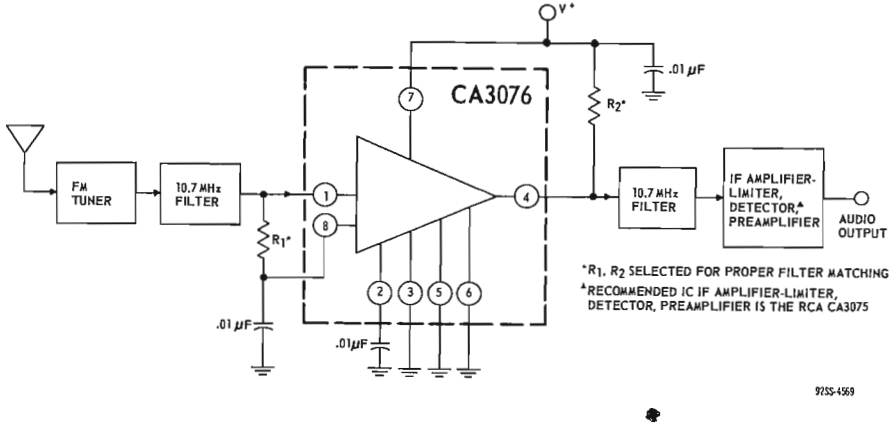


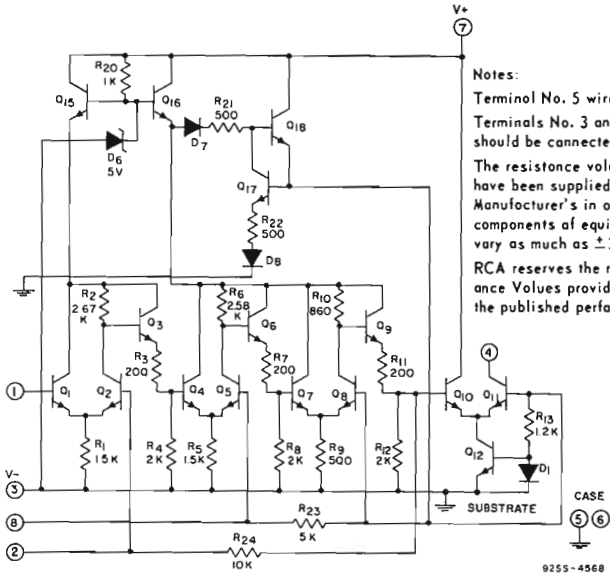
Fig. 1 - Block diagram of typical FM receiver utilizing the CA3076.

MAXIMUM RATINGS, *Absolute Maximum-Values at* $T_A = 25°C$

DC Supply Voltage [between Terminals 7 (V^+) and 3 (V^-)]	15	V
DC Current (into Terminal 7)	35	mA
Device Dissipation:		
Up to $T_A = 50°C$	500	mW
Above $T_A = 50°C$	derate linearly 5 mW/°C	
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/32 in (3.17 mm) from seating plane for 10 s max	+265	°C

ELECTRICAL CHARACTERISTICS *at* $T_A = 25°C$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CIRCUIT FIG. NO.
***Static Characteristics* – $V^+ = 8.5$ V**							
DC Current (into Term. 7)	I_7	–	10	15	24	mA	3
Quiescent Operating Current (into Term. 4)	I_4	–	–	0.65	–	mA	3
***Dynamic Characteristics* – $V^+ = 8.5$ V, $f_O = 10.7$ MHz**							
Input Limiting Voltage (knee, −3 dB point)	V_I (lim.)	–	–	50	200	μV	–
Output Voltage	V_O	$V_I = 20\mu V$	4	12	–	mV	5
Output Noise Voltage	V_N	$V_I = 0$	–	1	–	mV	5
Forward Transfer Admittance:							
Magnitude	$\lvert Y_{21} \rvert$	$V_I =$	–	6	–	mho	4
Phase	θ_{21}	$10\mu V$	–	80	–	degrees	
Reverse Transfer Admittance:							
Magnitude	$\lvert Y_{12} \rvert$	–	–	0.1	–	μmho	–
Phase	θ_{12}		–	−90	–	degrees	
Input-Impedance Components:							
Parallel Resistance	R_I	–	–	7.5	–	kΩ	–
Parallel Capacitance	C_I		–	4	–	pF	
Output-Impedance Components:							
Parallel Resistance	R_O	–	50	–	–	kΩ	–
Parallel Capacitance	C_O		–	1.7	–	pF	



Notes:

Terminol No. 5 wire-connected to the cose.

Terminals No. 3 and 6 which are connected to the substrate should be connected ta the most negative point in the circuit.

The resistonce volues included on the schematic diagram have been supplied as a convenience ta assist Equipment Manufocturer's in optimizing the selection of "outboard" components af equipment designs. The volues shown may vary as much as ±30%.

RCA reserves the right to moke any changes in the Resistance Volues provided such chonges do not odversely affect the published perfarmance chorocteristics of the device.

Fig. 2 - Schematic diagram of CA3076.

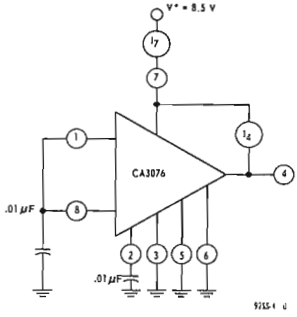


Fig. 3 - Test circuit for DC current (Terminal 7) and operating current (Terminal 4).

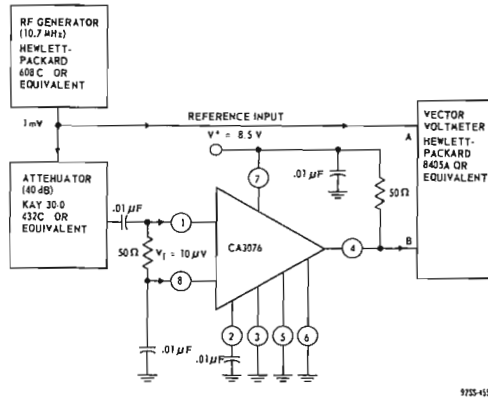


Fig. 4 - Forward transfer admittance (Y_{21}) test circuit

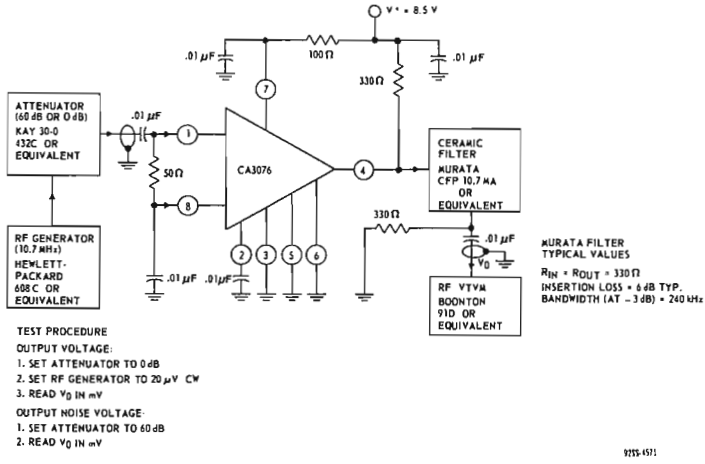


Fig. 5 - 10.7 MHz voltage gain and noise test circuit

RCA
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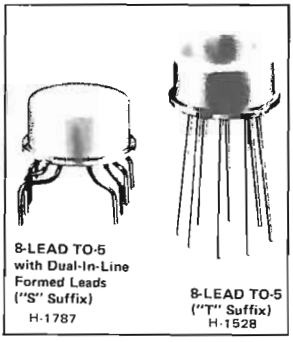
Linear Integrated Circuits

Monolithic Silicon

CA3078S CA3078T
CA3078AS CA3078AT



Micropower Operational Amplifier

Features:

- Low standby power: as low as 700 nW
- Wide supply voltage range: ±0.75 to ±15 V
- High peak output current: 6.5 mA min.
- Adjustable quiescent current
- Output short-circuit protection

Applications:

- Portable electronics
- Medical electronics
- Instrumentation
- Telemetry

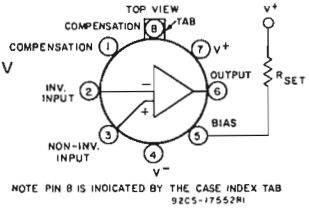


Fig.1 – Functional diagram of the CA3078T and CA3078AT.

The RCA CA3078T* and CA3078AT▲ are high-gain monolithic operational amplifiers which can deliver milli-amperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078T and CA3078AT provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5-volt battery is a practical reality with these devices.

* Formerly developmental type TA5807

▲ Formerly developmental type TA5807X

The CA3078AT is a premium device having a supply voltage range of $V^{\pm}$ = 0.75V to $V^{\pm}$ = 15V and an operating temperature range of −55°C to +125°C. The CA3078T has the same lower supply voltage limit but the upper limit is V^{+} = +6V and V^{-}=-6V. The operating temperature range is from 0°C to +70°C.

The CA3078 and CA3078A are supplied in either the standard 8-lead TO-5 package ("T" suffix), or in the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix).

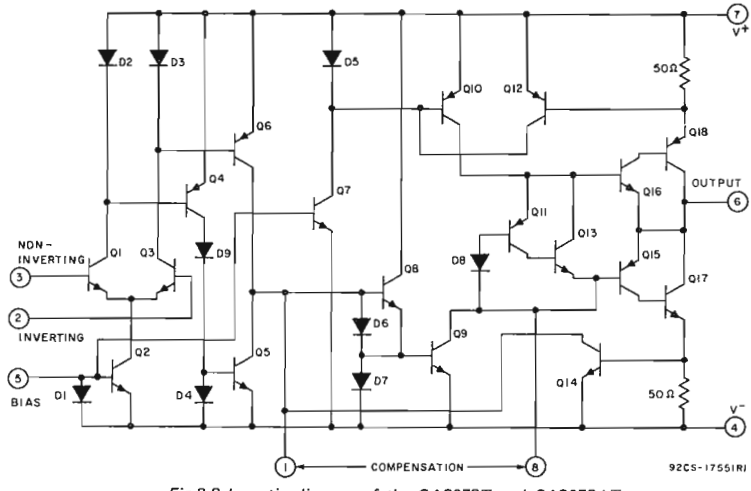


Fig.2-Schematic diagram of the CA3078T and CA3078AT.

ELECTRICAL CHARACTERISTICS

For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			CA3078AT LIMITS					UNITS
					R_{SET} = 5.1 MΩ, I_Q = 20 μA					
		V^+ & V^-	R_S KΩ	R_L KΩ	T_A = 25°C			T_A = −55 to 125°C		
					MIN	TYP	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	6	≤10	–	–	0.70	3.5	–	4.5	mV
Input Offset Current	I_{IO}		–	–	–	0.50	2.5	–	5.0	nA
Input Bias Current	I_{IB}		–	–	–	7	12	–	50	nA
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10	92	100	–	90	–	dB
Total Quiescent Current	I_Q		–	–	–	20	25	–	45	μA
Device Dissipation	P_D		–	–	–	240	300	–	540	μW
Maximum Output Voltage	V_{OM}		–	≥10	±5.1	±5.3	–	±5	–	V
Common-Mode Input Voltage Range	V_{ICR}		≤10	–	–	-5,5 to +5.8	–	-5 to +5	–	V
Common-Mode Rejection Ratio	CMRR		≤10	–	80	115	–	–	–	dB
Maximum Output Current	I_{OM}^+ or I_{OM}^-		–	–	–	12	–	6.5	30	mA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$		≤10	–	76	105	–	–	–	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$			–	76	105	–	–	–	
					R_{SET} = 13 MΩ, I_Q = 20 μA					
Input Offset Voltage	V_{IO}	15	≤10	–	–	1.4	3.5	–	4.5	mV
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10	92	100	–	88	–	dB
Total Quiescent Current	I_Q		–	–	–	20	30	–	50	μA
Device Dissipation	P_D		–	–	–	600	750	–	1350	μW
Maximum Output Voltage	V_{OM}		–	≥10	±13.7	±14.1		±13.5	–	V
Common-Mode Rejection Ratio	CMRR		≤10	–	80	106	–	–	–	dB
Input Bias Current	I_{IB}		–	–	–	7	14	–	55	nA
Input Offset Current	I_{IO}		–	–	–	0.50	2.7	–	5.5	nA

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

	CA3078AT	CA3078T
DC Supply Voltage (between V^+ and V^- terminal	36V	14V
Differential Input Voltage	±6V	±6V
DC Input Voltage	V^+ to V^-	V^+ to V^-
Input Signal Current	0.1 mA	0.1 mA
Output Short-Circuit Duration*	No Limitation	No Limitation
Device Dissipation	50 mW (up to 125°C)	500 mW (up to 70°C)
Temperature Range:		
Operating	-55 to +125°C	0 to +70°C
Storage	-65 to +150°C	-65 to +150°C
Lead Temperature (During Soldering):		
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max.	+300°C	+300°C

*Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			CA3078T LIMITS R_{SET} = 1 MΩ, I_Q = 100 μA					UNITS
		V^+ & V^-	R_S KΩ	R_L KΩ	T_A = 25°C			T_A = 0 to 70°C		
					MIN	TYP	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	6	≤10	–	–	1.3	4.5	–	5	mV
Input Offset Current	I_{IO}		–	–	–	6	32	–	40	nA
Input Bias Current	I_{IB}		–	–	–	60	170	–	200	nA
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10	88	92	–	86	–	dB
Total Quiescent Current	I_Q		–	–	–	100	130	–	150	μA
Device Dissipation	P_D		–	–	–	1200	1560	–	1800	μW
Maximum Output Voltage	V_{OM}		–	≥10	±5.1	±5.3	–	±5	–	V
Common-Mode Input Voltage Range	V_{ICR}		≤10	–	–	-5.5 to +5.8	–	-5 to +5	–	V
Common-Mode Rejection Ratio	CMRR		≤10	–	80	110	–	–	–	dB
Maximum Output Current	I_{OM}^+ or I_{OM}^-		–	–	–	12	–	6.5	30	mA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$		≤10	–	76	93	–	–	–	μV/V
Input Offset Voltage Sensitivity: Negative	$\Delta V_{IO}/\Delta V^-$			–	76	93	–	–	–	μV/V
Input Offset Voltage	V_{IO}	15	≤10	–	–	–	–	–	–	mV
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10	–	–	–	–	–	dB
Total Quiescent Current	I_Q		–	–	–	–	–	–	–	μA
Device Dissipation	P_D		–	–	–	–	–	–	–	μW
Maximum Output Voltage	V_{OM}		–	≥10	–	–	–	–	–	V
Common-Mode Rejection Ratio	CMRR		≤10	–	–	–	–	–	–	dB
Input Bias Current	I_{IB}		–	–	–	–	–	–	–	nA
Input Offset Current	I_{IO}		–	–	–	–	–	–	–	nA

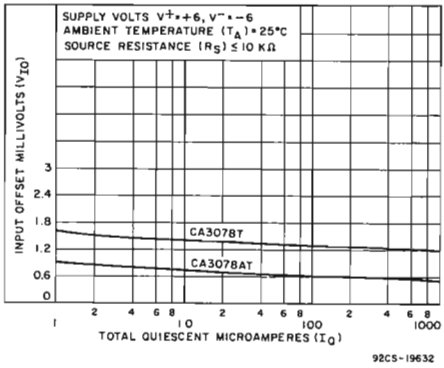


Fig.3 – Input offset voltage vs. total quiescent current.

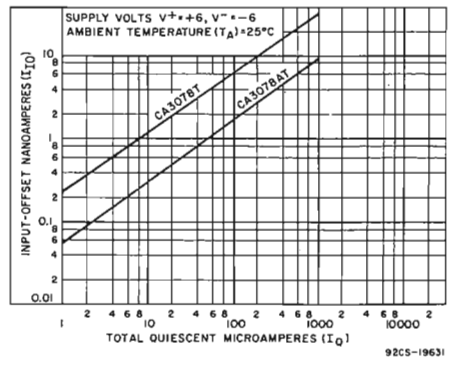


Fig.4 – Input offset current vs. total quiescent current.

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$
Typical Values Intended Only for Design Guidance

CHARACTERISTICS SYMBOLS	TYPICAL VALUES				UNITS
	CA3078AT		CA3078T		
	$V^+ = +1.3V$, $V^- = -1.3V$ $R_{SET} = 2\ M\Omega$ $I_Q = 10\ \mu A$	$V^+ = +0.75V$, $V^- = -0.75V$ $R_{SET} = 10\ M\Omega$ $I_Q = 1\ \mu A$	$V^+ = +1.3V$, $V^- = -1.3V$ $R_{SET} = 2\ M\Omega$ $I_Q = 10\ \mu A$	$V^+ = 0.75V$, $V^- = -0.75V$ $R_{SET} = 10\ M\Omega$ $I_Q = 1\ \mu A$	
V_{IO}	0.7	0.9	1.3	1.5	mV
I_{IO}	0.3	0.054	1.7	0.5	nA
I_{IB}	3.7	0.45	9	1.3	nA
A_{OL}	84	65	80	60	dB
I_Q	10	1	10	1	μA
P_D	26	1.5	26	1.5	μW
V_{OPP}	1.4	0.3	1.4	0.3	V
V_{ICR}	−0.8 to +1.1	−0.2 to +0.5	−0.8 to +1.1	−0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM^\pm}$	12	0.5	12	0.5	mA
$\Delta V_{IO}/\Delta V^\pm$	20	50	20	50	$\mu V/V$

Typical Values Intended Only for Design Guidance at $T_A = 25^oC$ and $V^+ = +6\ V$, $V^- = 6\ V$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CA3078AT		CA3078T	UNITS
			$R_{SET} = 5.1\ M\Omega$ $I_Q = 20\ \mu A$	$R_{SET} = 1\ M\Omega$ $I_Q = 100\ \mu A$	$R_{SET} = 1\ M\Omega$ $I_Q = 100\ \mu A$	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T_A$	R_S = 10 KΩ	5	6	6	$\mu V/^oC$
Input Offset Current Drift	$\Delta V_{IO}/\Delta T_A$	R_S = 10 KΩ	6.3	70	70	$pA/^oC$
Open-Loop Bandwidth	BW_{OL}	3dB pt.	0.3	2	2	kHz
Slew Rate: Unity Gain	SR	See Figs. 20, 21	0.027	0.04	0.04	$V/\mu s$
Slew Rate: Comparator	SR	See Figs. 20, 21	0.5	1.5	1.5	$V/\mu s$
Transient Response		10% to 90% Rise Time	3	2.5	2.5	μs
Input Resistance	R_I		7.4	1.7	0.87	MΩ
Output Resistance	R_O		1	0.8	0.8	KΩ
Equiv. Input Noise Voltage	$e_N(10\ Hz)$	$R_S = 0$	40	—	25	$nV/\sqrt{Hz}$
Equiv. Input Noise Current	$i_N(10\ Hz)$	R_S = 1 MΩ	0.25	—	1	$pA/\sqrt{Hz}$

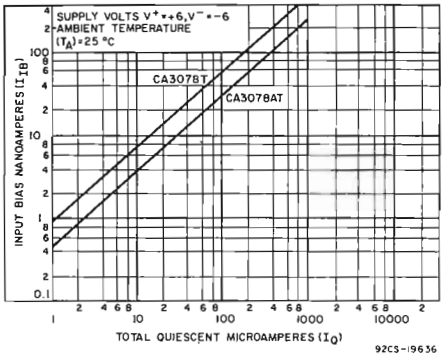


Fig.5 – Input bias current vs. total quiescent current.

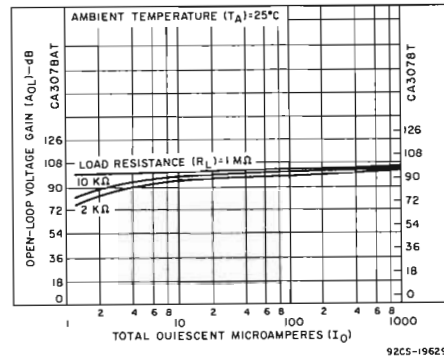


Fig.6 – Open-loop voltage gain vs. total quiescent current.

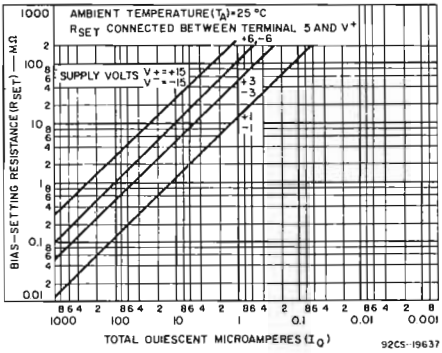


Fig.7 – Bias-setting resistance vs. total quiescent current.

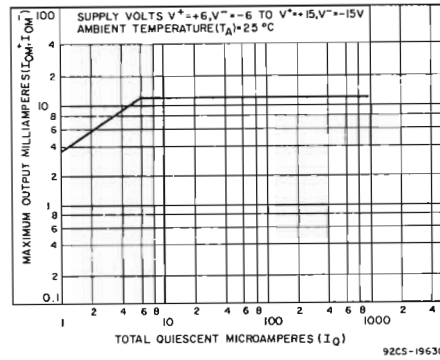


Fig.8 – Maximum output current vs. total quiescent current.

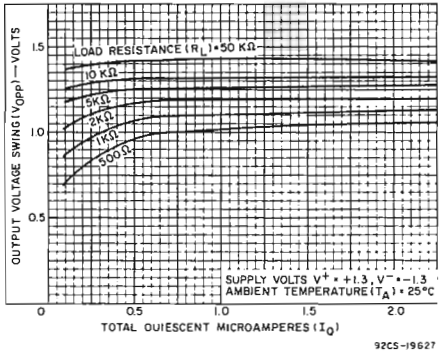


Fig.9 – Output voltage swing vs. total quiescent current.

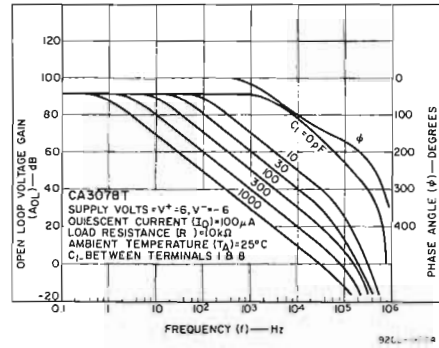


Fig.10 – Open-loop voltage gain vs. frequency for I_Q = 100 μA – CA3078T.

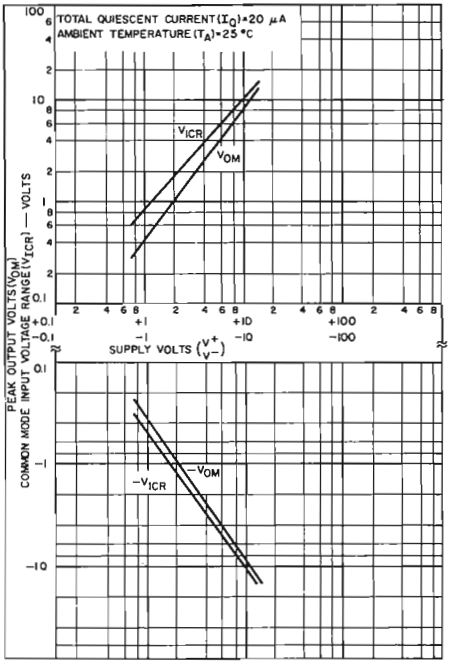


Fig.11 – Output and common-mode voltage vs. supply voltage.

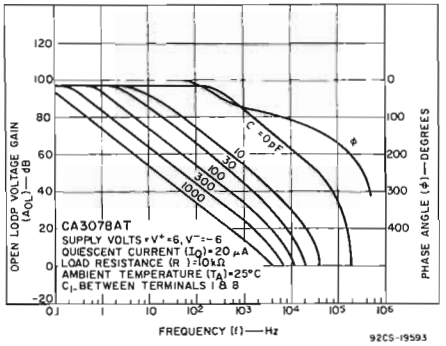


Fig.12 – Open-loop voltage gain vs. frequency for I_Q = 20 μA – CA3078AT.

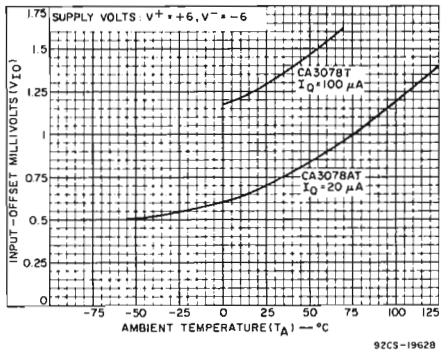


Fig.13 – Input offset voltage vs. temperature.

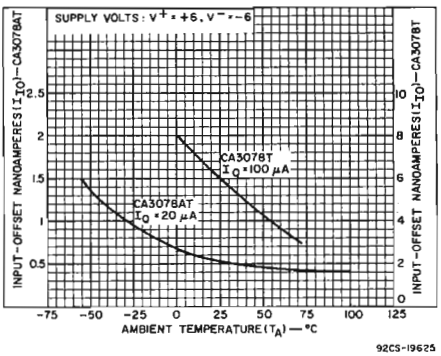


Fig.14 – Input offset current vs. temperature.

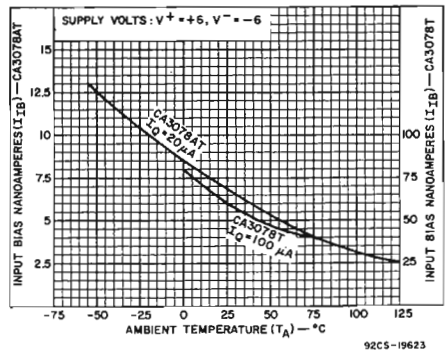


Fig.15 – Input bias current vs. temperature.

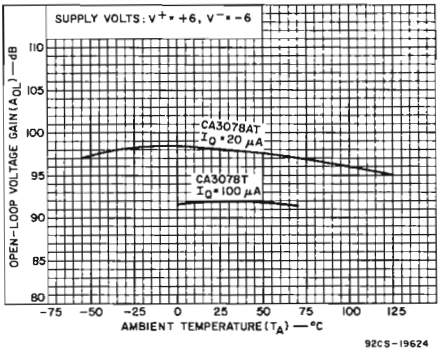


Fig.16 – Open-loop voltage gain vs. temperature.

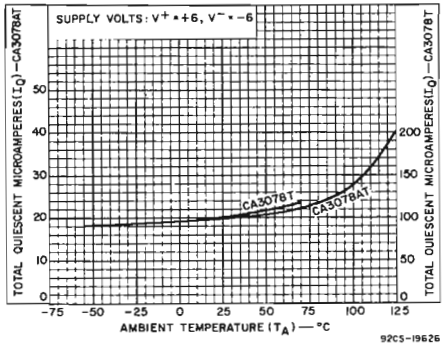


Fig.17 – Total quiescent current vs. temperature.

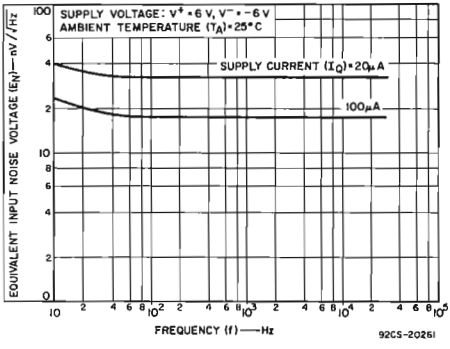


Fig.18 – Equivalent input noise voltage vs. frequency.

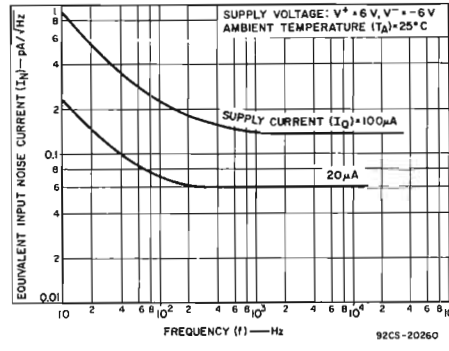


Fig.19 – Equivalent input noise current vs. frequency.

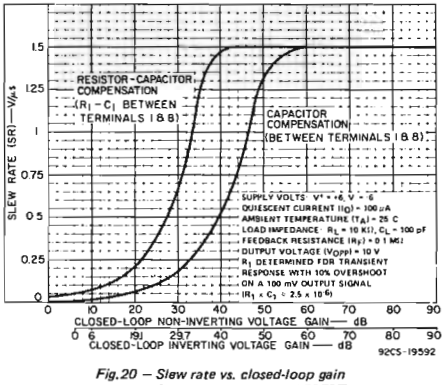


Fig.20 – Slew rate vs. closed-loop gain for I_Q = 100 μA – CA3078T.

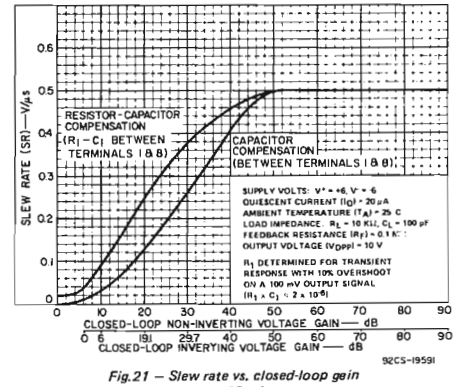


Fig.21 – Slew rate vs. closed-loop gain for I_Q = 20 μA – CA3078AT.

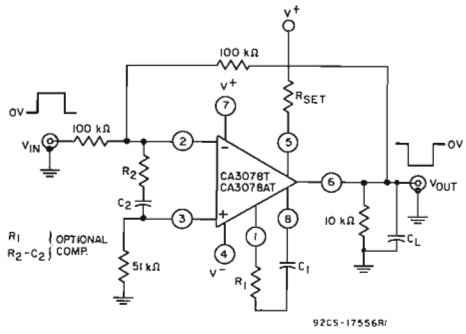


Fig.22 – Transient response and slew-rate, unity gain (inverting) test circuit.

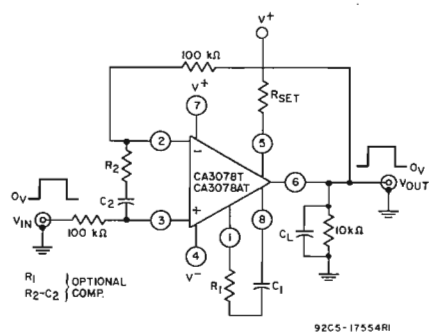


Fig.23 – Slew, rate, unity gain (non-inverting) test circuit.

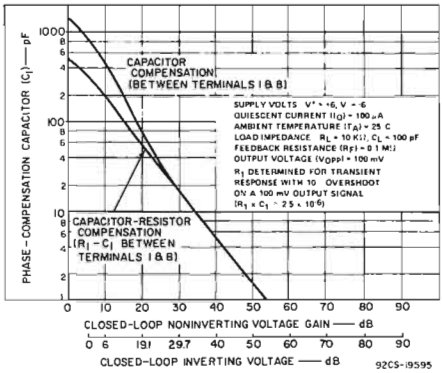


Fig.24 – Phase compensation capacitance vs. closed-loop gain – CA3078T.

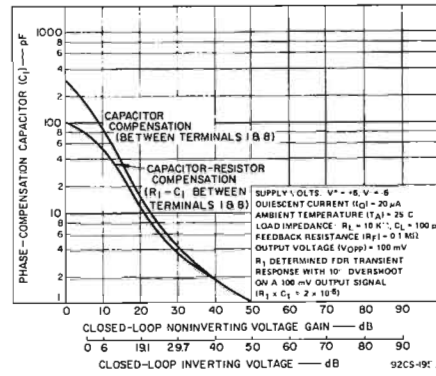


Fig.25 – Phase compensation capacitance vs. closed-loop gain – CA3078AT.

Table I - Unity-gain slew rate vs. compensation – CA3078T and CA3078AT

SUPPLY VOLTS: $V^+ = 6$, $V^- = -6$

OUTPUT VOLTAGE (V_O) = ±5V
LOAD RESISTANCE (R_L) = 10 kΩ

TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE of 100 mV
AMBIENT TEMPERATURE (T_A) = 25°C

COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) Fig. 22					UNITY GAIN (NON-INVERTING) Fig. 23				
	R1	C1	R2	C2	SLEW RATE	R1	C1	R2	C2	SLEW RATE
CA3078T – I_Q = 100 μA	kΩ	pF	kΩ	μF	V/μs	kΩ	pF	kΩ	μF	V/μs
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor & Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078AT – I_Q = 20 μA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor & Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

OPERATING CONSIDERATIONS

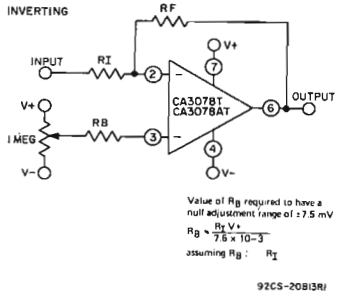
Compensation Techniques

The CA3078AT and CA3078T can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figs. 24 and 25. These curves represent the compensation necessary at quiescent currents of 20 μA and 100 μA, respectively, for a transient response with 10% overshoot. Figs. 21 and 22 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output.

Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table 1 gives an indication of slew rates that can be obtained with various compensation techniques at quiescent currents of 20 μA and 100 μA.

Single Supply Operation

The CA3078AT and CA3078T can operate from a single supply with a minimum total supply voltage of 1.5 volts. Figs. 27 and 28 show the CA3078AT or CA3078T in inverting and non-inverting 20-dB amplifier configurations utilizing a 1.5-volt type "AA" cell for a supply. The total power consumption for either circuit is approximately 675 nanowatts. The output voltage swing in this configuration is 300 mV p-p with a 20 kΩ load.



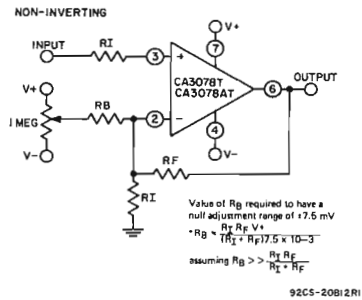


Fig.26 – Offset voltage null circuits.

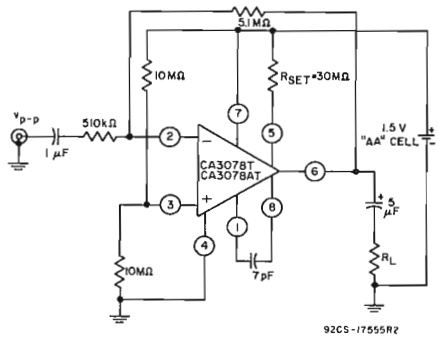


Fig.27 – Inverting 20-dB amplifier circuit.

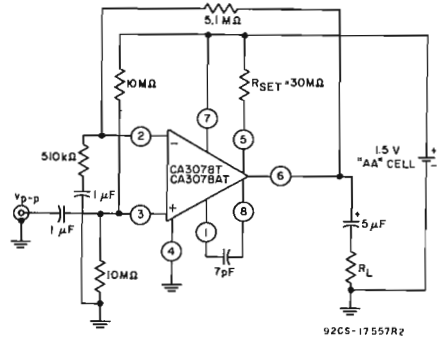


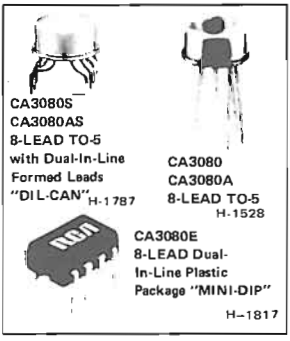
Fig.28 – Non-inverting 20-dB amplifier circuit.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3080, CA3080A Types



Operational Transconductance Amplifiers (OTA's)

Gateable-Gain Blocks

Features:

- Slew rate (unity gain, compensated): 50 V/μs
- Adjustable power consumption: 10μW to 30 mW
- Flexible supply voltage range: ±2 V to ±15 V
- Fully adjustable gain: 0 to $g_m R_L$ limit
- Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)
- Extended g_m linearity: 3 decades

Applications:

- Sample and hold
- Multiplex
- Voltage follower
- Multiplier
- Comparator

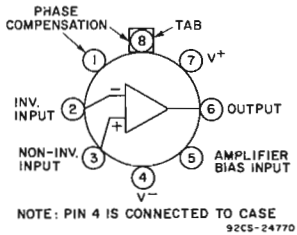
The RCA-CA3080 and CA3080A are Gateable-Gain Blocks which utilize the unique Operational Transconductance Amplifier (OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

The CA3080 and CA3080A have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

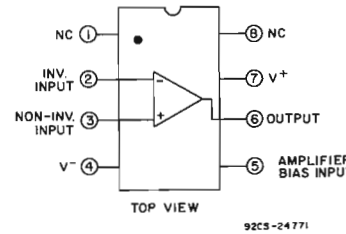
The CA3080 and CA3080A are notable for their excellent slew rate (50 V/μs), which makes them especially useful for multiplex and fast unity-gain voltage followers. These types are especially applicable for multiplex applications because power is consumed only when the devices are in the "ON" channel state.

The CA3080A is rated for operation over the full military-temperature range (−55 to +125°C) and its characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplex, etc. Operational transconductance amplifiers are also useful in programmable power-switch applications, e.g., as described in Application Note ICAN-6048, "Some Applications of a Programmable Power Switch/Amplifier" (CA3094, CA3094A, CA3094B).

These types are supplied in the 8-lead TO-5 style package (CA3080, CA3080A), and in the 8-lead TO-5 style package with dual-in-line formed leads ("DIL-CAN", CA3080S, CA3080AS). The CA3080E is also supplied in the 8-lead dual-in-line plastic ("MINI-DIP") package (CA3080E), and in chip form (CA3080H).



TO-5 Style Package



Plastic Package (CA3080E)

Fig. 1—Functional diagrams.

ELECTRICAL CHARACTERISTICS

For Equipment Design — **CA3080**

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS: Circuit Fig.	TEST CONDITIONS: $V^+ = 15$ V, $V^- = -15$ V, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	Typical Characteristics Curves Fig.	LIMITS: Min.	LIMITS: Typ.	LIMITS: Max.	UNITS
Input Offset Voltage	V_{IO}	–		3	–	0.4	5	mV
			$T_A = 0$ to 70^oC		–	–	6	
Input Offset Current	I_{IO}	–		4	–	0.12	0.6	μA
Input Bias Current	I_I	–		5	–	2	5	μA
			$T_A = 0$ to 70^oC		–	–	7	
Forward Transconductance (large signal)	g_m	–		14	6700	9600	13000	μmho
			$T_A = 0$ to 70^oC		5400	–	–	
Peak Output Current	$\|I_{OM}\|$	–	$R_L = 0$	6	350	500	650	μA
			$R_L = 0$, $T_A = 0$ to 70^oC		300	–	–	
Peak Output Voltage: Positive	V^+_{OM}	–	$R_L = \infty$	7	12	13.5	–	V
Negative	V^-_{OM}				−12	−14.4	–	
Amplifier Supply Current	I_A	–		8	0.8	1	1.2	mA
Device Dissipation	P_D	–		9	24	30	36	mW
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$	–		–	–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$	–		–	–	–	150	
Common-Mode Rejection Ratio	CMRR	–		–	80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–		7	12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I	–		15	10	26	–	kΩ

ELECTRICAL CHARACTERISTICS

Typical Values Intended Only for Design Guidance — **CA3080**

Input Offset Voltage	V_{IO}	–	$I_{ABC} = 5\ \mu A$	3	0.3	mV
Input Offset Voltage Change	$\|\Delta V_{IO}\|$	–	Change in V_{IO} between $I_{ABC} = 500\ \mu A$ and $I_{ABC} = 5\ \mu A$	–	0.2	mV
Peak Output Current	I_{OM}	–	$I_{ABC} = 5\ \mu A$	6	5	μA
Peak Output Voltage: Positive	V^+_{OM}	–	$I_{ABC} = 5\ \mu A$	7	13.8	V
Negative	V^-_{OM}				−14.5	
Magnitude of Leakage Current		10	$I_{ABC} = 0$, $V_{TP} = 0$	11	0.08	nA
			$I_{ABC} = 0$, $V_{TP} = 36$ V		0.3	
Differential Input Current		12	$I_{ABC} = 0$, $V_{DIFF} = 4$ V	13	0.008	nA
Amplifier Bias Voltage	V_{ABC}	–		16	0.71	V
Slew Rate: Maximum (uncompensated)	SR			–	75	V/μs
Unity Gain (compensated)		23			50	
Open-Loop Bandwidth	BW_{OL}	–		–	2	MHz
Input Capacitance	C_I	–	f = 1 MHz	17	3.6	pF
Output Capacitance	C_O	–	f = 1 MHz	17	5.6	pF
Output Resistance	R_O	–		18	15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	19	f = 1 MHz	20	0.024	pF

ELECTRICAL CHARACTERISTICS
For Equipment Design

CA3080A

CHARACTERISTICS	SYMBOLS	Circuit Fig.	TEST CONDITIONS ($V^+ = 15$ V, $V^- = -15$ V, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	Typical Characteristics Curves Fig.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Input Offset Voltage	V_{IO}	–	$I_{ABC} = 5\ \mu A$	3	–	0.3	2	mV
					–	0.4	2	
			$T_A = -55$ to $+125^oC$		–	–	5	
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	–	Change in V_{IO} between $I_{ABC} = 500\ \mu A$ and $I_{ABC} = 5\ \mu A$	3	–	0.1	3	mV
Input Offset Current	I_{IO}	–		4	–	0.12	0.6	μA
Input Bias Current	I_I	–		5	–	2	5	μA
			$T_A = -55$ to $+125$		–	–	8	
Forward Transconductance (large signal)	gm	–		14	7700	9600	12000	μmho
			$T_A = -55$ to $+125^oC$		4000	–	–	
Peak Output Current	$\lvert I_{OM}\rvert$		$I_{ABC} = 5\ \mu A$, $R_L = 0$	6	3	5	7	μA
			$R_L = 0$		350	500	650	
			$R_L = 0$, $T_A = -55$ to $+125^o$		300	–	–	
Peak Output Voltage:								
Positive	V^+_{OM}	–	$I_{ABC} = 5\ \mu A$	7	12	13.8	–	V
Negative	V^-_{OM}		$R_L = \infty$		−12	−14.5	–	
Positive	V^+_{OM}	–	$R_L = \infty$		12	13.5	–	
Negative	V^-_{OM}				−12	−14.4	–	
Amplifier Supply Current	I_A	–		8	0.8	1	1.2	mA
Device Dissipation	P_D	–		9	24	30	36	mW
Input Offset Voltage Sensitivity:								
Positive	$\Delta V_{IO}/\Delta V^+$	–		–	–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$				–	–	150	
Magnitude of Leakage Current		10	$I_{ABC} = 0$, $V_{TP} = 0$	11	–	0.08	5	nA
			$I_{ABC} = 0$, $V_{TP} = 36$ V		–	0.3	5	
Differential Input Current		12	$I_{ABC} = 0$, $V_{DIFF} = 4$ V	13	–	0.008	5	nA
Common-Mode Rejection Ratio	CMRR	–		–	80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–		7	12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I	–		15	10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only For Design Guidance

CA3080A

Amplifier Bias Voltage	V_{ABC}	–		16	0.71	V
Slew Rate:						
Maximum (uncompensated)	SR			–	75	V/μs
Unity Gain (compensated)		23			50	
Open-Loop Bandwidth	BW_{OL}	–	–	–	2	MHz
Input Capacitance	C_I	–	f = 1 MHz	17	3.6	pF
Output Capacitance	C_O	–	f = 1 MHz	17	5.6	pF
Output Resistance	R_O	–		18	15	MΩ
Input-to-Output Capacitance	C_{I-O}	19	f = 1 MHz	20	0.024	pF

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$

DC SUPPLY VOLTAGE (between V^+ and V^- terminals)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE	V^+ to V^-
INPUT SIGNAL CURRENT	1 mA
AMPLIFIER BIAS CURRENT	2 mA
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite
DEVICE DISSIPATION	125 mW
TEMPERATURE RANGE:	
Operating	
CA30B0	0 to + 70 °C
CA3080A	−55 to + 125 °C
Storage	−65 to + 150 °C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

* Short circuit may be applied to ground or to either supply.

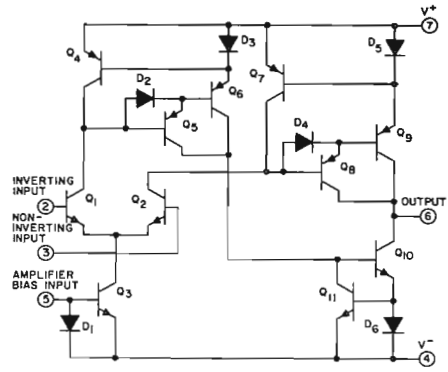


Fig.2 – Schematic diagram for CA3080 and CA3080A.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS FOR THE CA3080 AND CA3080A

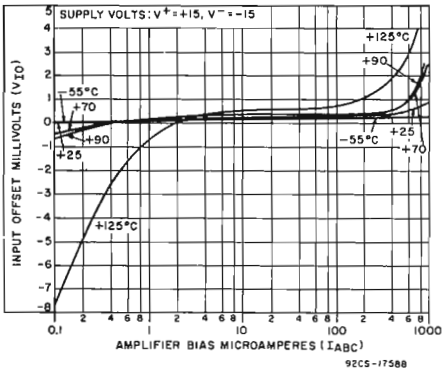


Fig.3 – Input offset voltage vs. amplifier bias current.

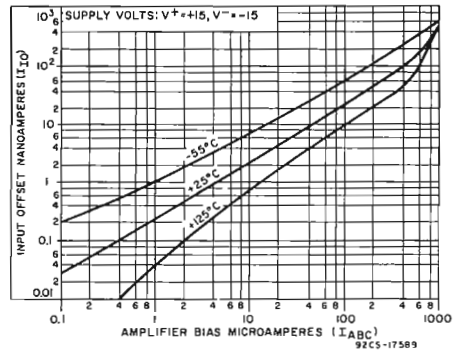


Fig.4 – Input offset current vs. amplifier bias current.

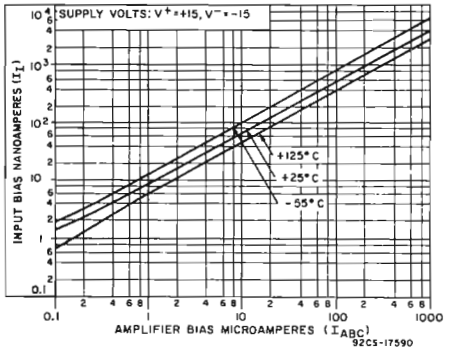


Fig.5 – Input bias current vs. amplifier bias current.

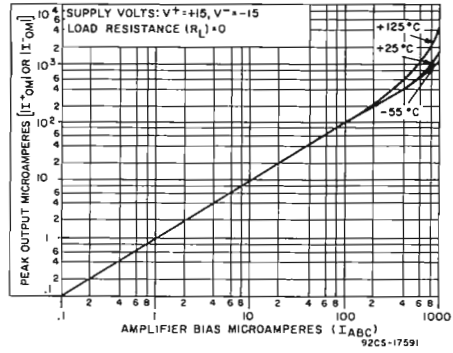


Fig.6 – Peak output current vs. amplifier bias current.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

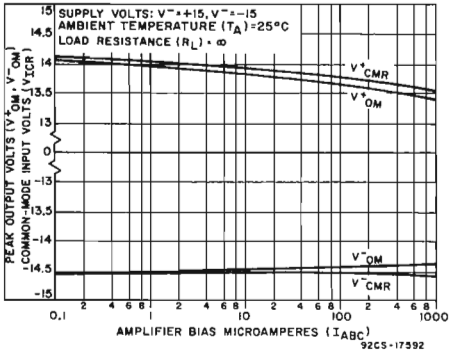


Fig.7 – Peak output voltage vs. amplifier bias current.

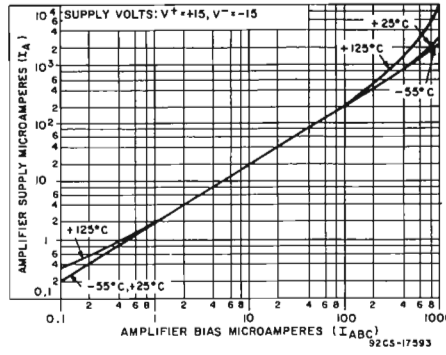


Fig.8 – Amplifier supply current vs. amplifier bias current.

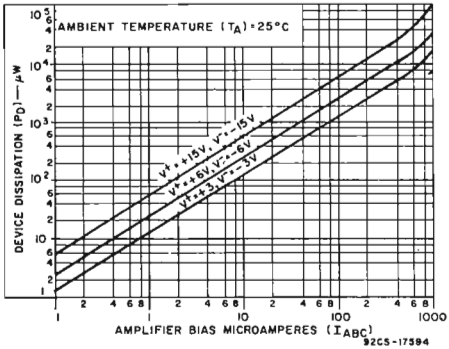


Fig.9 – Total power dissipation vs. amplifier bias current.

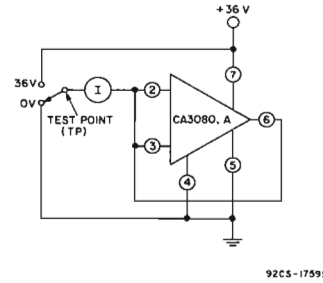


Fig.10 – Leakage current test circuit.

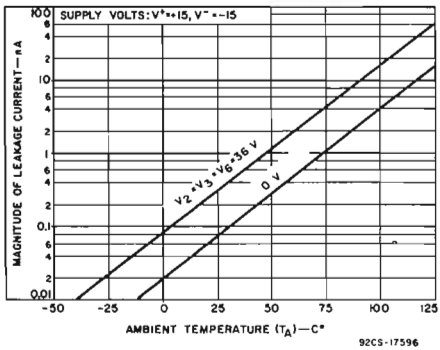


Fig.11 – Leakage current vs. temperature.

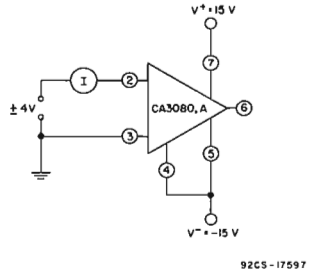


Fig.12 – Differential input current test circuit.

TYPICAL CHARACTERISTIC CURVES AND TEST CIRCUITS (Cont'd)

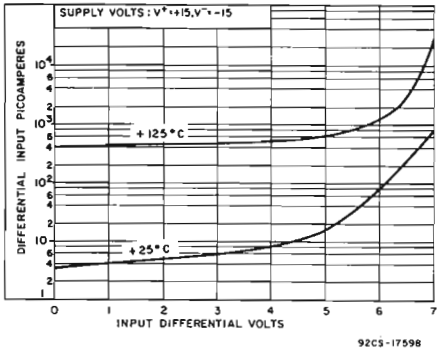


Fig. 13 – Input current vs. input differential voltage.

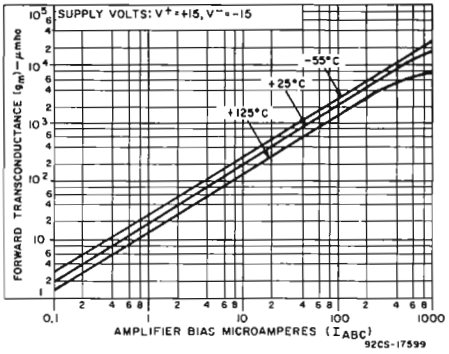


Fig. 14 – Transconductance vs. amplifier bias current.

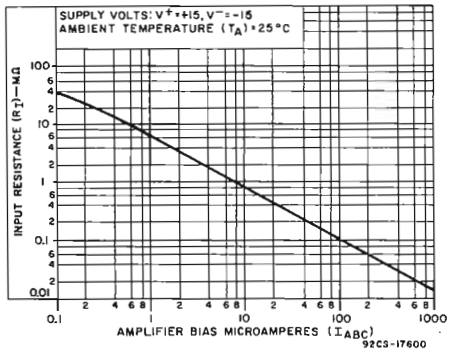


Fig. 15 – Input resistance vs. amplifier bias current.

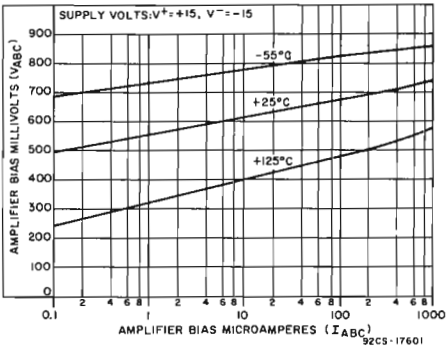


Fig. 16 – Amplifier bias voltage vs. amplifier bias current.

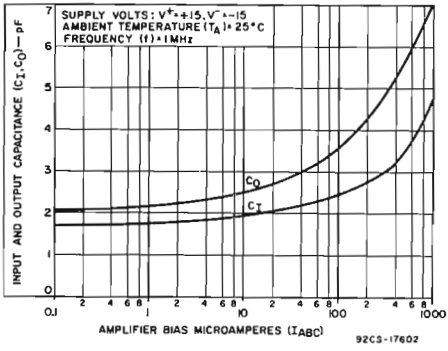


Fig. 17 – Input and output capacitance vs. amplifier bias current.

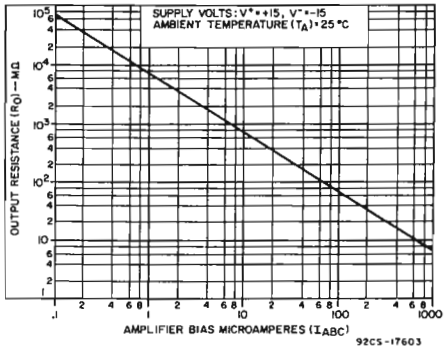


Fig. 18 – Output resistance vs. amplifier bias current.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

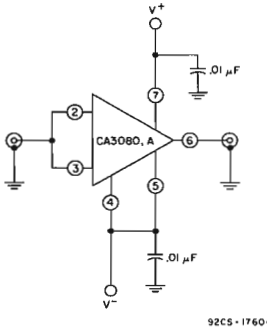


Fig.19 – Input-to-output capacitance test circuit.

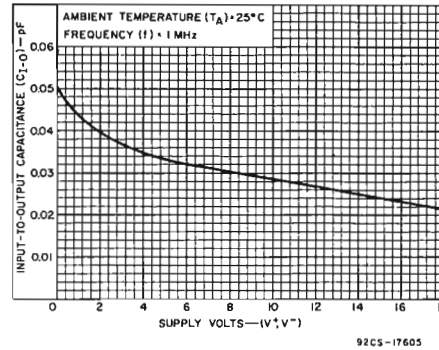
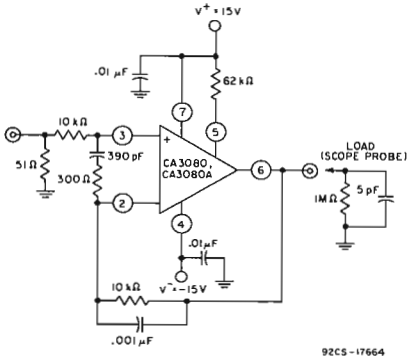


Fig.20 – Input-to-output capacitance vs. supply voltage.



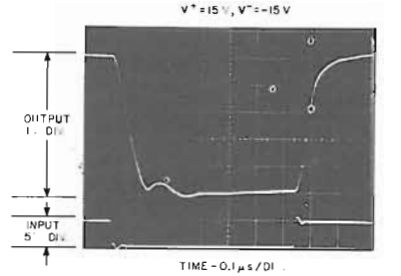
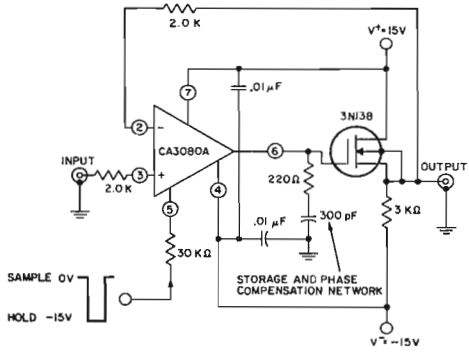


Fig.21 – Schematic diagram of the CA3080 and CA3080A in a unity-gain voltage follower configuration and associated waveform.



SLEW RATE (IN SAMPLE MODE) = 1.3 V/μs
ACQUISITION TIME* = 3 μs

* TIME REQUIRED FOR OUTPUT TO SETTLE WITHIN ±3mV OF A 4-VOLT STEP

Fig.22 – Schematic diagram of the CA3080A in a sample-hold configuration.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3081, CA3081F
CA3082, CA3082F

16-Lead Dual-In-Line
Frit-Seal (Hermetic)
Package H-1807

16-Lead Dual-In-Line
Plastic Package H-1622

General-Purpose High-Current N-P-N Transistor Arrays

CA3081–Common-Emitter Array CA3082–Common-Collector Array

Directly Drive 7-Segment Incandescent Displays and Light-Emitting-Diode (LED) Displays

Features

- 7 transistors permit a wide range of applications in either a common-emitter (CA3081) or common-collector (CA3082) configuration
- High I_C: 100 mA max. ■ Low $V_{CE\ sat}$ (at 50 mA): 0.4 V typ.

Applications

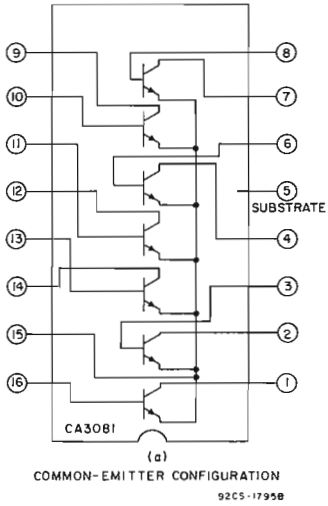
- Drivers for:
  - Incandescent display devices (e.g. RCA NUMITRON DR2000 Series and lamps)
  - LED (e.g. RCA-SG1002 GaAs High-Efficiency Emitting Diode)
  - Relay control —Thyristor firing

RCA-CA3081* and CA3082* consist of seven high-current (to 100 mA) silicon n-p-n transistors on a common monolithic substrate. The CA3081 is connected in a common-emitter configuration and the CA3082 is connected in a common-collector configuration.

The CA3081 and CA3082 are capable of directly driving seven-segment displays, such as the RCA NUMITRON devices (DR2000 and DR2010), and light-emitting diode (LED) displays. These types are also well-suited for a variety of other driver applications, including relay control and thyristor firing.

The CA3081 and CA3082 are supplied in a 16-lead dual-in-line plastic package, and the CA3081F and CA3082F in a 16-lead dual-in-line frit-seal ceramic package, which includes a separate substrate connection for maximum flexibility in circuit design.

* Formerly developmental types TA5858 and TA6033, respectively.



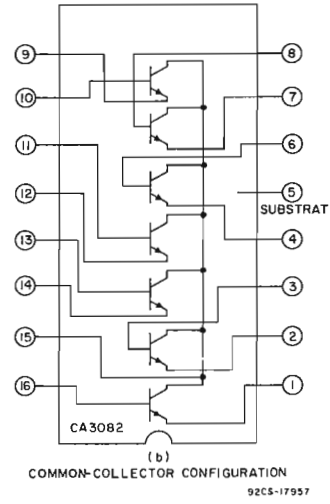


Fig. 1–Functional diagrams of types CA3081 and CA3082.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:

Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C

Ambient Temperature Range:

Operating	−55 to +125	°C
Storage	−65 to + 150	°C

Lead Temperature (During Soldering):

At distance 1/16" ±1/32" (1,59 mm ±0.79 mm) from case for 10 seconds max.	265	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CEO})	16	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CES}$	I_C = 500 μA, I_E = 0	–	20	60	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 500 μA, I_E = 0, I_B = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	16	24	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_C = 500 μA	–	5	6.9	–	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 0.5 V, I_C = 30 mA	–	30	68	–	
		V_{CE} = 0.8 V, I_C = 50 mA	–	40	70	–	
Base-to-Emitter Saturation Voltage	$V_{BE\ sat}$	I_C = 30 mA, I_B = 1 mA	3	–	0.87	1.0	V
Collector-to-Emitter Saturation Voltage: CA3081, CA3082	$V_{CE\ sat}$	I_C = 30 mA, I_B = 1 mA	–	–	0.27	0.5	V
CA3081		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.7	
CA3082		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.8	
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	1	μA

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR OF TYPES CA3081 AND CA3082

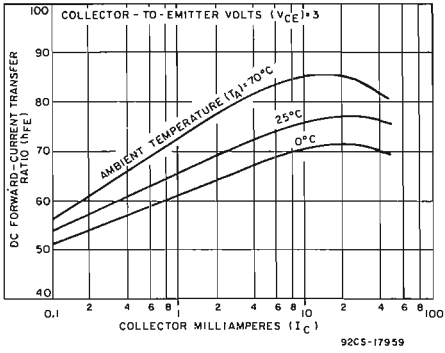


Fig.2—h_{FE} vs. I_C

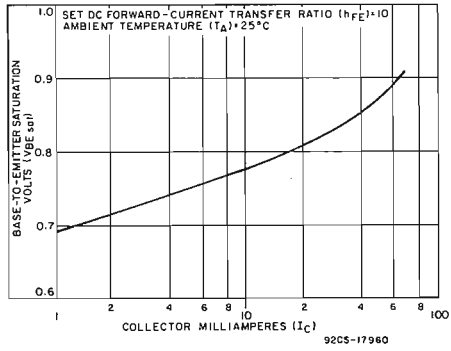


Fig.3—V_{BEsat} vs. I_C

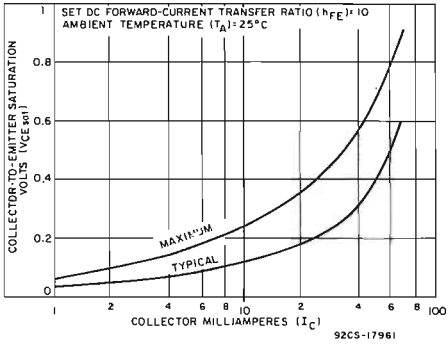


Fig.4—V_{CEsat} vs. I_C at T_A = 25°C.

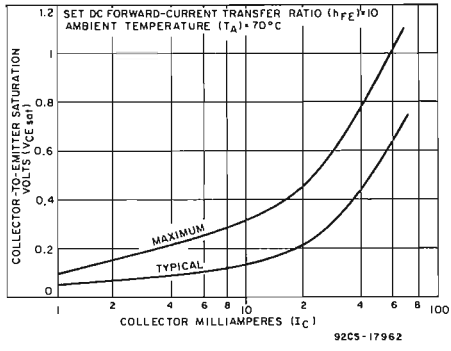


Fig.5—V_{CEsat} vs. I_C at T_A = 70°C.

TYPICAL READ-OUT DRIVER APPLICATIONS

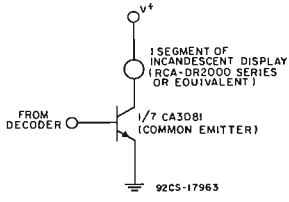
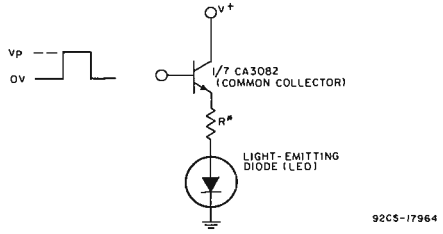


Fig.6—Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.



*THE RESISTANCE FOR R IS DETERMINED BY THE RELATIONSHIP

$$R = \frac{V_P - V_{BE} - V_F(LED)}{I\,(LED)}$$

WHERE: V_P = INPUT PULSE VOLTAGE

V_F = FORWARD VOLTAGE DROP ACROSS THE DIODE

R = 0 FOR $V_P = V_{BE} + V_F(LED)$

Fig.7—Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3083, CA3083F

16-Lead Dual-In-Line Frit-Seal (Hermetic) Package H-1807

16-Lead Dual-In-Line Plastic Package H-1622

General-Purpose High-Current N-P-N Transistor Array

Applications

- Signal processing and switching systems operating from DC to VHF
- Lamp and relay driver
- Differential amplifier
- Temperature-compensated amplifier
- Thyristor firing
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for suggested applications

RCA-CA3083 is a versatile array of five high-current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design. The CA3083 is supplied in a 16-lead dual-in-line plastic package, and the CA3083F in a 16-lead dual-in-line frit-seal ceramic package.

Features

- High I_C: 100mA max.
- Low V_{CEsat} (at 50mA): 0.7V max.
- Matched pair (Q1 and Q2)—
  V_{IO} (V_{BE} matched): ± 5 mV max.
  I_{IO} (at 1mA): 2.5 μA max.
- 5 independent transistors plus separate substrate connection

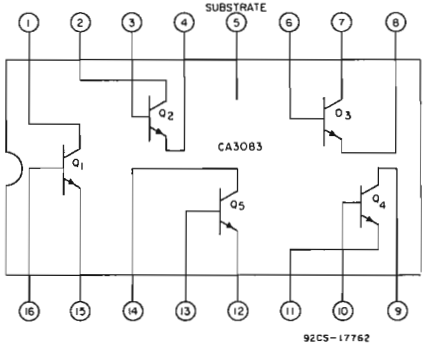


Fig.1—Functional diagram of the CA3083.

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

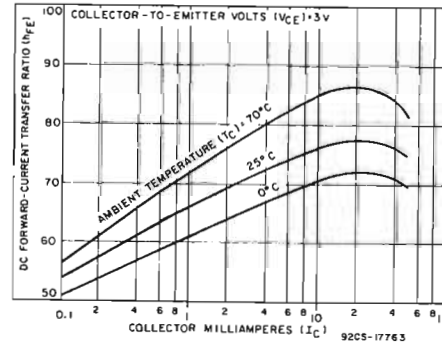


Fig.2 – h_{FE} vs I_C

MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^oC$

Power Dissipation:

Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C

Ambient Temperature Range:

Operating	−55 to +125	°C
Storage	−65 to +150	°C

Lead Temperature (During Soldering):

At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\mu A$, $I_E = 0$	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 100\mu A$, $I_B = 0$, $I_E = 0$	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 500\mu A$, $I_C = 0$	–	5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	–	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	–	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 3V$ $I_C = 10mA$	2	40	76	–	
		$V_{CE} = 3V$ $I_C = 50mA$	2	40	75	–	
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$, $I_C = 10mA$	3	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	$I_C = 50mA$, $I_B = 5mA$	4	–	0.40	0.70	V
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Absolute Input Offset Voltage	$\lvert V_{IO} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	7	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO} \rvert$	$V_{CE} = 3V$, $I_C = 1mA$	8	–	0.7	2.5	μA

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

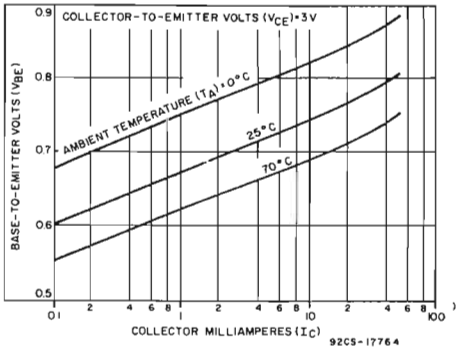


Fig.3 – V_{BE} vs I_C

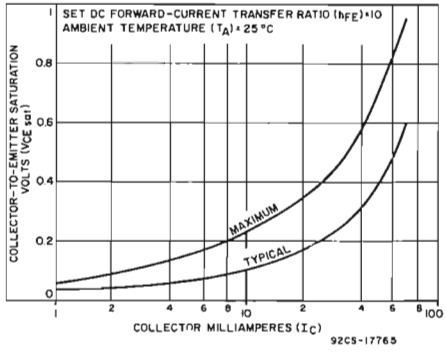


Fig.4 – V_{CEsat} vs I_C at 25°C

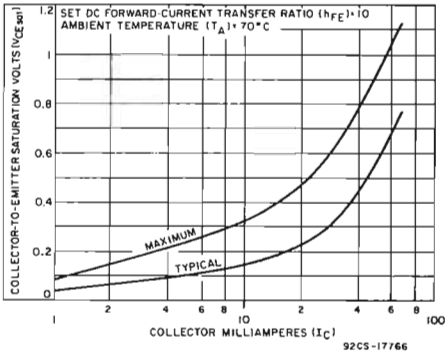


Fig.5 – V_{CEsat} vs I_C at 70°C

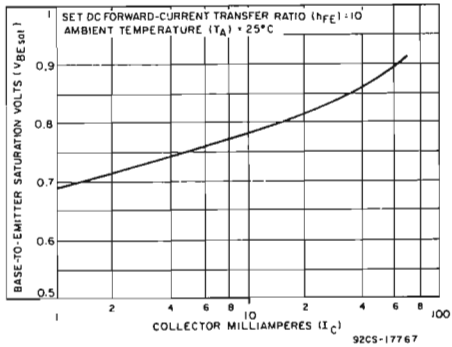


Fig.6 – V_{BEsat} vs I_C

TYPICAL STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

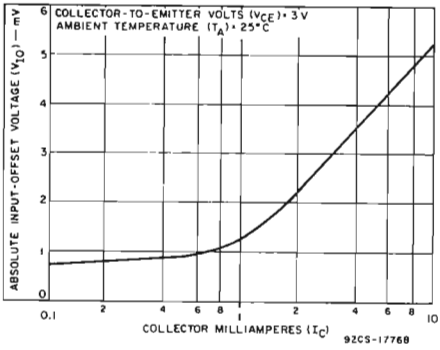


Fig.7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

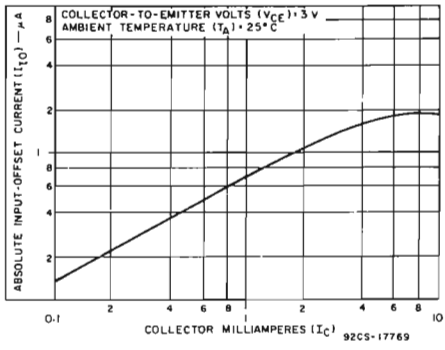


Fig.8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3084

H-1517

14-Lead Dual-In-Line Plastic Package

General-Purpose P-N-P Transistor Array

FEATURES

- Matched transistor pair (Q1 and Q2)
  V_{IO} (V_{BE} matched): ± 6mV max.
  I_{IO} (at 100 μA): ± 0.6 μA
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz

RCA-CA3084* is a general-purpose silicon p-n-p transistor array incorporating two independent transistors, a Darlington circuit, and a current-mirror pair with a shared diode.

The two independent transistors in the array may be used in a variety of circuit applications. The Darlington pair may be employed as the equivalent of a single high-beta transistor. The current-mirror pair is well suited for constant-current applications and can also be used as the active loads in a differential amplifier which uses n-p-n transistors.

The total array is especially useful for a wide range of applications in systems having low-power and low-frequency requirements. Although the transistors may be used as discrete units in conventional circuits, they offer the advantages inherent in integrated-circuit construction, that is, to provide close electrical and thermal matching.

The CA3084 utilizes the 14-lead dual-in-line plastic package.

*Formerly developmental type TA5799A.

APPLICATIONS

- General use in signal processing systems having low-power and low-frequency requirements
- Differential amplifiers
- Temperature compensated amplifiers
- Active loads for differential amplifiers using n-p-n transistors
- Complementary uses with RCA n-p-n transistor arrays

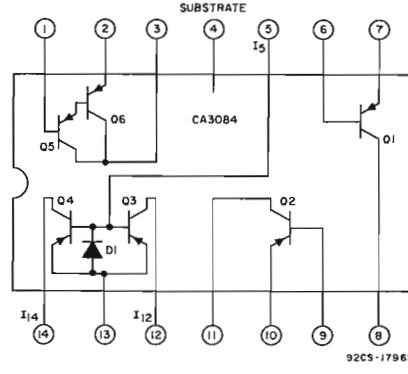


Fig. 1 – Functional diagram of the CA3084.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Characteristics Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:							
Collector-Cutoff Current	I_{CBO}	V_{CB} = −10V, I_E = 0	2	–	−0.055	−100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	3	–	−0.12	−100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_{CE} = −100μA, I_B = 0	–	−40	−70	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_{CB} = −100μA, I_E = 0	–	−40	−80	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_{EB} = −100μA, I_C = 0	–	−40	−100	–	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	I_{EI} = 100μA	–	−40	−100	–	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_E = 1mA, I_B = 100μA	4	–	−0.125	−0.25	V
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	5	−0.50	−0.59	−0.68	V
DC Forward-Current Transfer Ratio	h_{FE}		7	15	40	–	
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Magnitude of Input Offset Voltage	$\lvert V_{IO} \rvert$	I_E = 100μA, V_{CE} = −10V	8	–	0.422	6	mV
Input Offset Current	I_{IO}		–	−0.6	0	0.6	μA
For Transistors Q3 and Q4 (Current-Mirror Configuration):							
Collector Current (Normalized)	I_C/I_5	V_{CE} = −5V, V_{CIO} = −5V,	10	0.85	1.00	1.15	
Magnitude of Collector Current Ratio	$\lvert I_{C(Q3)}/I_{C(Q4)} \rvert$	Term. 13 = Gnd. I_5 = −100μA,	11	0.90	1.00	1.10	
For Transistors Q5 and Q6 (Darlington Configuration):							
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	–	–	–	−1.0	μA
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	13	0.92	1.07	1.20	V
DC Forward-Current Transfer Ratio	h_{FE}		15	100	1230	–	

ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only For Design Guidance

Magnitude of Temperature Coefficient:					
V_{BE} (for each transistor)	$\lvert \Delta V_{BE}/\Delta T \rvert$	I_E = 100μA,	6	−1.78	mV/°C
V_{IO} (as a differential amplifier)	$\lvert \Delta V_{IO}/\Delta T \rvert$	V_{CE} = −10V	9	0.54	μV/°C
V_{BE} (Darlington configuration)	$\lvert \Delta V_{BE}/\Delta T \rvert$		14	−3.7	mV/°C
For Each Transistor:					
Input Resistance	R_I	f = 1kHz, V_{CE} = −10V,	19	9	kΩ
Output Resistance	R_O	I_C = −100μA	20	– 600 –	kΩ
Forward Transconductance	g_m		22	– 3 –	mmho
Collector-to-Base Capacitance	C_{CBO}	I_{CB} = 0	23	– 3.3 –	pF
Collector-to-Emitter Capacitance	C_{CEO}	I_{CE} = 0	23	– 2.5 –	pF
Base-to-Substrate Capacitance	C_{BIO}	I_{CIO} = 0	23	– 4.5 –	pF

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Dissipation:		
Any one transistor	200	mW
Total package	750	mW
Above T_A = 55°C	derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	−40	V
Collector-to-Base Voltage (V_{CBO})	−40	V
Base-to-Substrate Voltage (V_{BIO})*	−40	V
Emitter-to-Base Voltage (V_{EBO})	−40	V
Collector Current (I_C)	−10	mA

*The base of each transistor of the CA3084 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any base voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (4) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

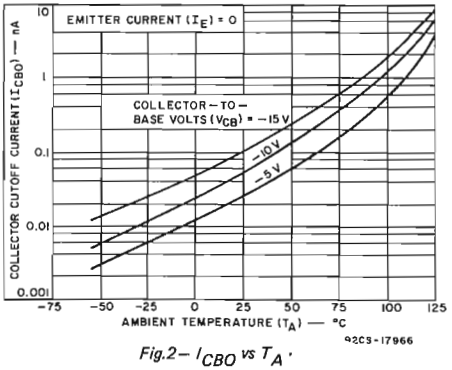


Fig.2 – I_{CBO} vs T_A.

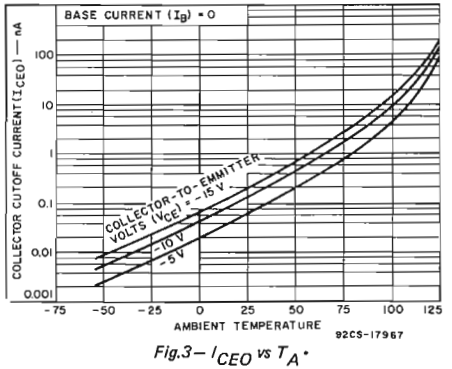


Fig.3 – I_{CEO} vs T_A.

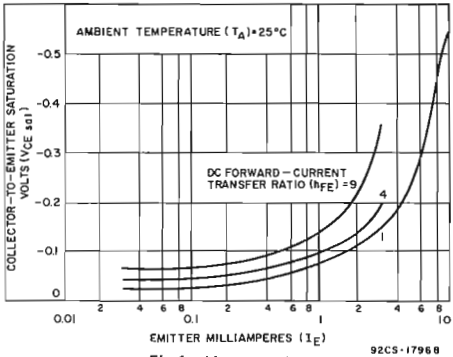


Fig.4 – V_{CEsat} vs I_E.

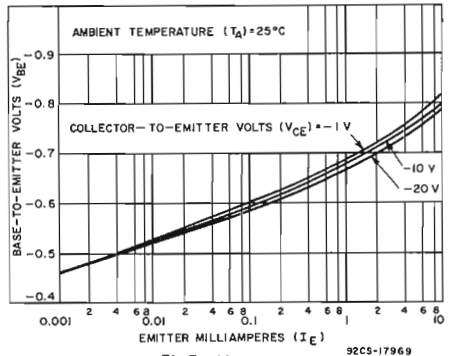


Fig.5 – V_{BE} vs I_E.

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

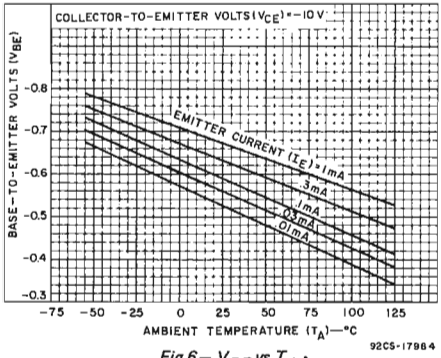


Fig.6 – V_{BE} vs T_A.

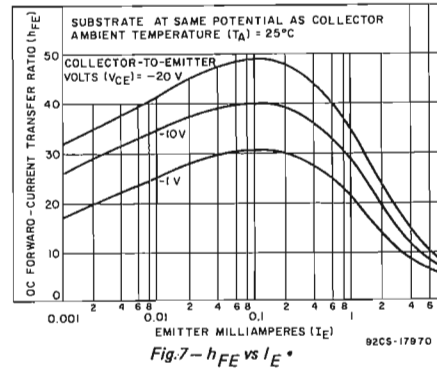


Fig.7 – h_{FE} vs I_E.

STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

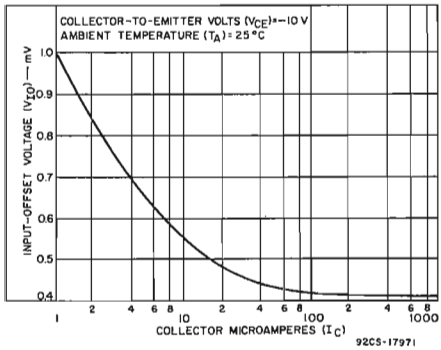


Fig.8—V_{IO} vs I_C, (transistors Q1 and Q2 as a differential amplifier).

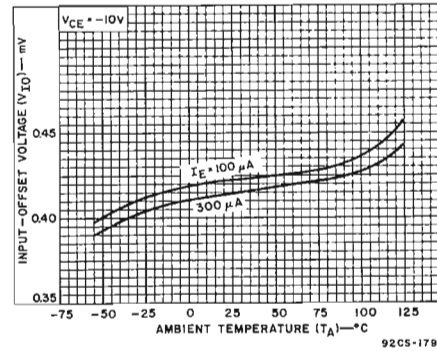


Fig.9—V_{IO} vs T_A (transistors Q1 and Q2 as a differential amplifier).

STATIC CHARACTERISTICS FOR CURRENT-MIRROR CONFIGURATION

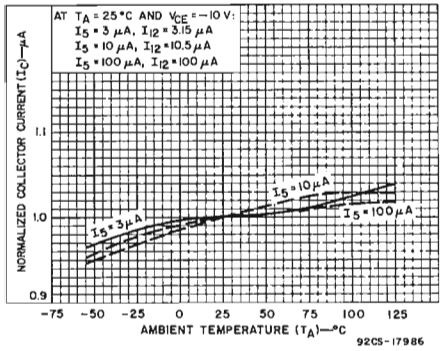


Fig.10—Normalized I_C vs T_A (transistors Q3 and Q4 in a current-mirror configuration.

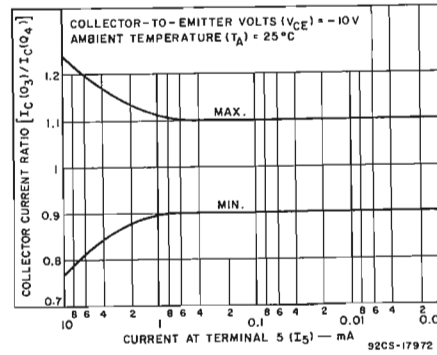


Fig.11—I_C ratio vs I_5 (transistors Q3 and Q4 in a current-mirror configuration.

STATIC CHARACTERISTICS FOR CURRENT-MIRROR CONFIGURATION

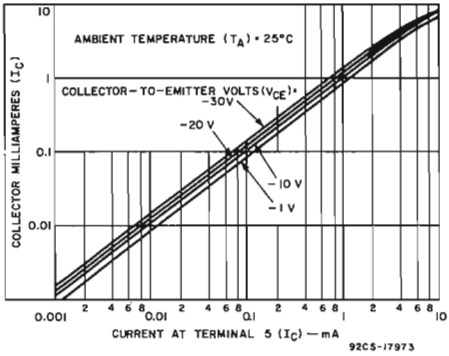


Fig.12 – I_C vs I_5 (transistors Q3 and Q4 in a current-mirror configuration).

STATIC CHARACTERISTICS FOR DARLINGTON CONFIGURATION

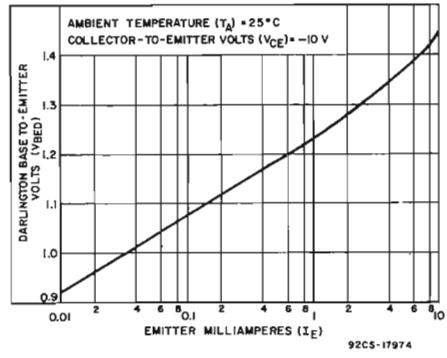


Fig.13 – V_{BE} vs I_E (transistors Q5 and Q6 in a darlingtron configuration).

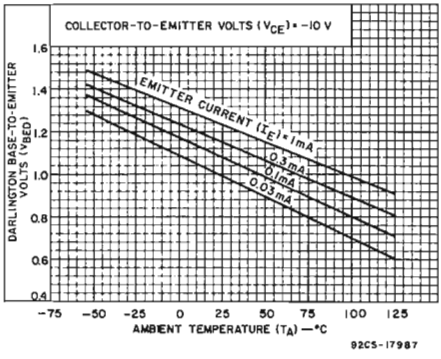


Fig.14 – V_{BE} vs T_A (transistors Q5 and Q6 in a darlington configuration).

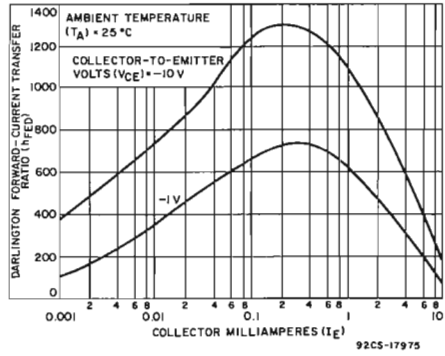


Fig.15 – h_{FE} vs. I_E (transistors Q5 and Q6 in a darlington configuration).

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

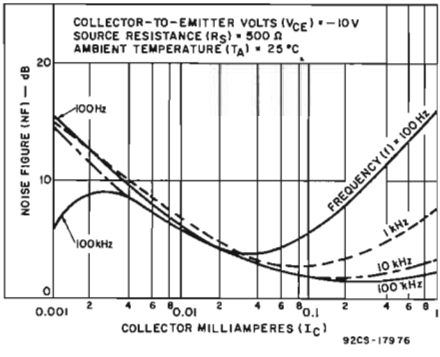


Fig.16 – NF vs I_C at R_S = 500 Ω

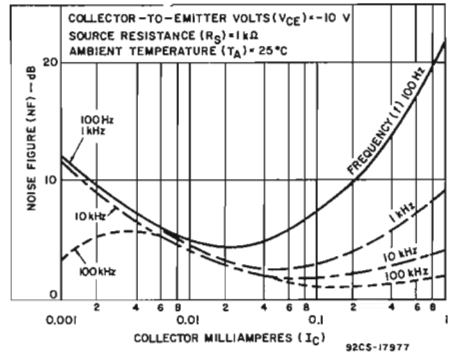


Fig.17 – NF bs I_C at R_S = 1 kΩ

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR (Cont'd)

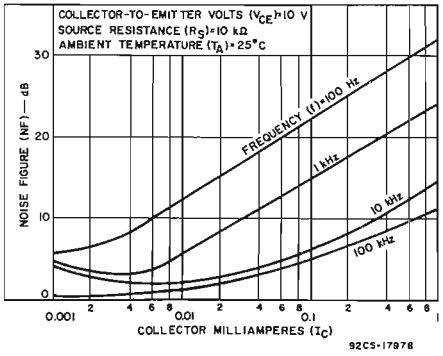


Fig.18– NF vs I_C at R_S = 10kΩ

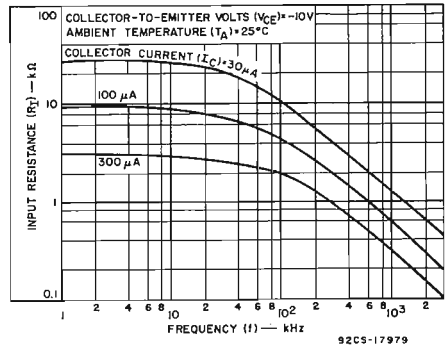


Fig.19– R_I vs f

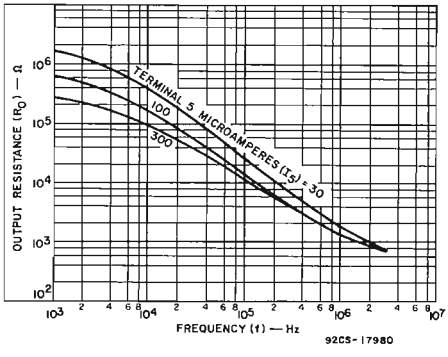


Fig.20– R_O vs f

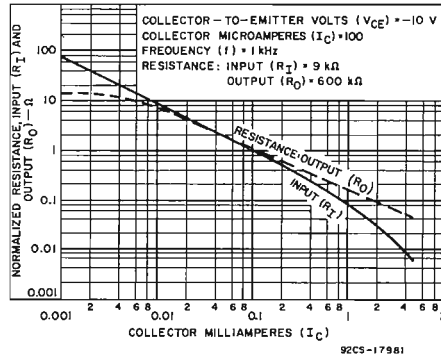


Fig.21– Normalized R_I and R_O vs I_C

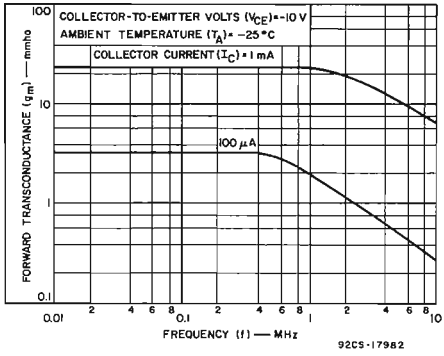


Fig.22– g_m vs f

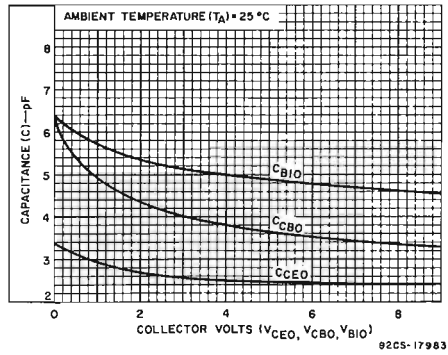
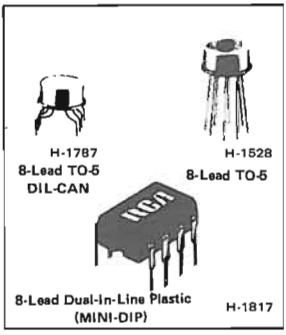


Fig.23– Transistor capacitances vs collector voltages (V_{CEO}, V_{CBO}, V_{CIO})

RCA Solid State Division

Linear Integrated Circuits

CA3085, CA3085A, CA3085B Types



Positive Voltage Regulators

For Regulated Voltages from 1.7 V to 46 V at Currents up to 100 mA

Features

- Up to 100 mA output current
- Input and output short-circuit protection
- Load and line regulation: 0.025%
- Pin compatible with LM100 Series
- Adjustable output voltage

Applications

- Shunt voltage regulator
- Current regulator
- Switching voltage regulator
- High-current voltage regulator
- Combination positive and negative voltage regulator
- Dual tracking regulator

RCA-CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7 to 46 volts at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown in Fig. 1. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

The CA3085A and CA3085B have output current capabilities up to 100 mA and the CA3085 up to 12 mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100 mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5 to 30 V (CA3085), 7.5 to 40 V (CA3085A), and 7.5 to 50 V (CA3085B) and a minimum regulated output voltage of 26 V (CA3085), 36 V (CA3085A), and 46 V (CA3085B).

The CA3085A is unilaterally interchangeable with the CA3055.

These types are supplied in the 8-lead TO-5 style package (CA3085, CA3085A, CA3085B, and the 8-lead TO-5 with dual-in-line formed leads ("DIL-CAN", CA3085S, CA3085AS, CA3085BS). The CA3085 is also supplied in the 8-lead dual-in-line plastic package ("MINI-DIP", CA3085E), and in chip form (CA3085H).

Type	V_{IN} Range V	V_{OUT} Range V	Max. I_{OUT} mA	Max. Load Regulation % V_{OUT}
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100 mA, however, regulation is not specified beyond 12 mA.

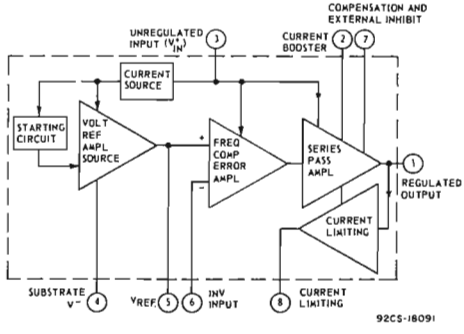


Fig. 1—Block diagram of CA3085 Series.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

POWER DISSIPATION: WITHOUT HEAT SINK	WITH HEAT SINK (TO-5 ONLY)
up to T_A = 55°C ..... 630 mW	up to T_C = 55°C .... 1.6 W
above T_A = 55°C derate linearly @6.67 mW/°C	above T_C = 55°C .... derate linearly at 16.7 mW/°C

TEMPERATURE RANGE:

Operating ..... −55 to +125°C
Storage ..... −65 to +150°C

UNREGULATED INPUT VOLTAGE:

CA3085 ..... 30 V
CA3085A ..... 40 V
CA3085B ..... 50 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERMINAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	*	*	*	*	*	+10 0
6	–	–	*	*	*	*	*	*
7	–	–	–	+3 −10	+3 −10	*	*	* 0
8	–	–	–	–	+5 −1	*	*	*
1	–	–	–	–	–	+10 −‡	0 −‡	+‡ 0
2	–	–	–	–	–	–	0 –	+‡ 0
3	–	–	–	–	–	–	–	+‡ 0
4	–	–	–	–	–	–	–	Substrate & Case

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡30 V for CA3085
40 V for CA3085A
50 V for CA3085B

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–

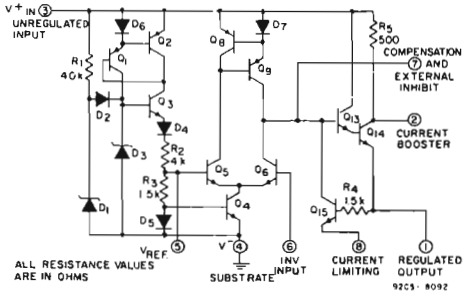


Fig.2—Schematic diagram of CA3085 Series.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: Test Circuit Fig. No.	TEST CONDITIONS: T_A = 25°C [Unless indicated otherwise]	CA3085 MIN.	CA3085 TYP.	CA3085 MAX.	CA3085A MIN.	CA3085A TYP.	CA3085A MAX.	CA3085B MIN.	CA3085B TYP.	CA3085B MAX.	UNITS
Reference Voltage	V_{REF}	4	V^+_{IN} = 15V	1.4	1.6	1.8	1.5	1.6	1.7	1.5	1.6	1.7	V
Quiescent Regulator Current	$I_{quiescent}$	4	V^+_{IN} = 30V	–	3.3	4.5	–	–	–	–	–	–	mA
			V^+_{IN} = 40V	–	–	–	–	3.65	5	–	–	–	
			V^+_{IN} = 50V	–	–	–	–	–	–	–	4.05	7	
Input Voltage Range	$V_{IN(range)}$	–	–	7.5	–	30	7.5	–	40	7.5	–	50	V
Maximum Output Voltage	$V_{O(max.)}$	4	V^+_{IN} = 30, 40, 50V#; R_L = 365Ω; Term. No. 6 to Gnd.	26	27	–	36	37	–	46	47	–	V
Minimum Output Voltage	$V_{O(min.)}$	4	V^+_{IN} = 30V	–	1.6	1.8	–	1.6	1.7	–	1.6	1.7	V
Input-Output Voltage Differential	V_{IN}-V_{OUT}	–	–	4	–	28	4	–	38	3.5	–	48	V
Limiting Current	I_{LIM}	7	V^+_{IN} = 18V, V^+_{OUT} = 10V R_{SCP}* = 6Ω	–	96	120	–	96	120	–	96	120	mA
Load Regulation●	–	–	I_L = 1 to 100mA, R_{SCP} = 0	–	–	–	–	0.025	0.15	–	0.025	0.15	%V_{OUT}
		–	I_L = 1 to 100mA, R_{SCP} = 0 T_A = 0°C to +70°C	–	–	–	–	0.035	0.6	–	0.035	0.6	
		–	I_L = 1 to 12mA, R_{SCP} = 0	–	0.003	0.1	–	–	–	–	–	–	
Line Regulation▲	–	–	I_L = 1mA, R_{SCP} = 0	–	0.025	0.1	–	0.025	0.075	–	0.025	0.04	%/V
		–	I_L = 1mA, R_{SCP} = 0 T_A = 0°C to +70°C	–	0.04	0.15	–	0.04	0.1	–	0.04	0.08	
Equivalent Noise Output Voltage	V_{NOISE}	11	V^+_{IN} = 25V, C_{REF} = 0	–	0.5	–	–	0.5	–	–	0.5	–	mV p-p
			C_{REF} = 0.22μF	–	0.3	–	–	0.3	–	–	0.3	–	
Ripple Rejection	–	12	V^+_{IN} = 25V, f = 1kHz, C_{REF} = 0	–	50	–	–	50	–	45	50	–	dB
			C_{REF} = 2μF	–	56	–	–	56	–	50	56	–	
Output Resistance	r_o	12	V^+_{IN} = 25V, f = 1kHz	–	0.075	1.1	–	0.075	0.3	–	0.075	0.3	Ω
Temperature Coefficient of Reference and Output Voltages	$\Delta V_{REF}/\Delta V_o$	–	I_L = 0, V_{REF} = 1.6V	–	0.0035	–	–	0.0035	–	–	0.0035	–	%/°C
Load Transient Recovery Time: Turn On	t_{ON}	16	V^+_{IN} = 25V, +50mA Step	–	1	–	–	1	–	–	1	–	μs
Turn Off	t_{OFF}		V^+_{IN} = 25V, −50mA Step	–	3	–	–	3	–	–	3	–	μs
Line Transient Recovery Time: Turn On	t_{ON}	–	V^+_{IN} = 25V, f = 1kHz, 2V Step	–	0.8	–	–	0.8	–	–	0.8	–	μs
Turn Off	t_{OFF}	–		–	0.4	–	–	0.4	–	–	0.4	–	μs

30V (CA3085), 40V(CA3085A), 50V(CA3085B)

* RSCP: Short-circuit protection resistance

● Load Regulation = $\frac{\Delta V_{OUT}}{V_{OUT(initial)}} \times 100\%$

▲ Line Regulation = $\frac{(\Delta V_{OUT})}{[V_{OUT(initial)}]\ (\Delta V_{IN})} \times 100\%$

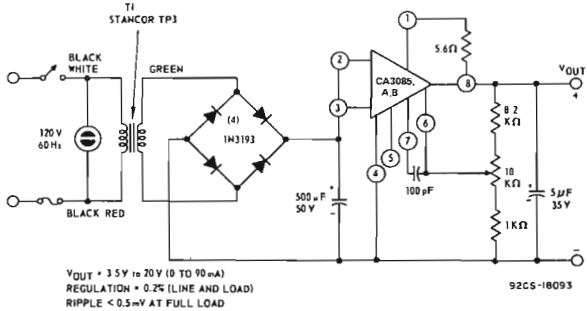
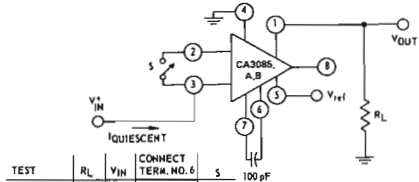


Fig.3—Application of the CA3085 Series in a typical power supply.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES



TEST	R_L	V_{IN}	CONNECT TERM. NO. 6	S
V_{REF}	∞	+1.6	OPEN	OPEN
$I_{QUIESCENT}$	∞	+40	OPEN	OPEN
V_{OUT} (MAX.)	365Ω	+40	GROUND	CLOSED
V_{OUT} (MIN.)	10k	+30	TERM. NO. 1	OPEN

Fig.4—Test circuit for V_{REF}, $I_{quiescent}$, V_{OUT}(max.), V_{OUT}(min.).

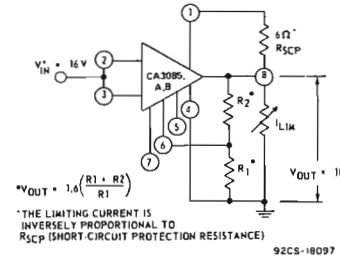


Fig.7—Test circuit for limiting current

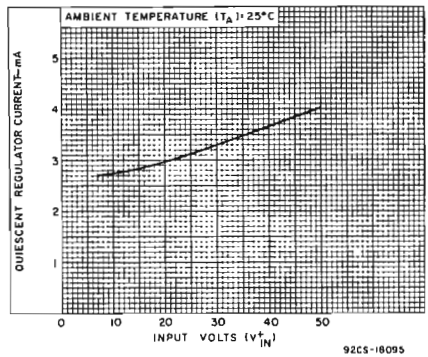


Fig.5—$I_{quiescent}$ vs. V^+_{IN}.

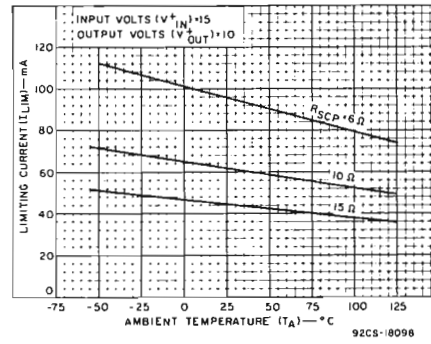


Fig.8—I_{LIM} vs. T_A.

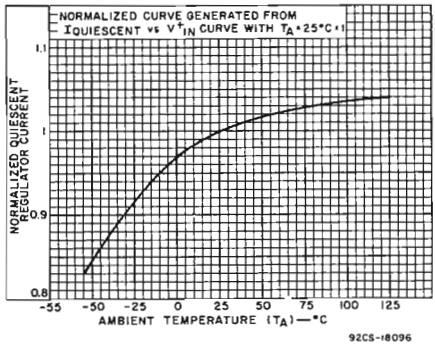


Fig.6—Normalized $I_{quiescent}$ vs. T_A.

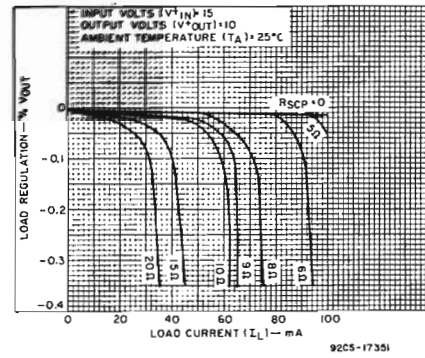


Fig.9—Load regulation characteristics.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

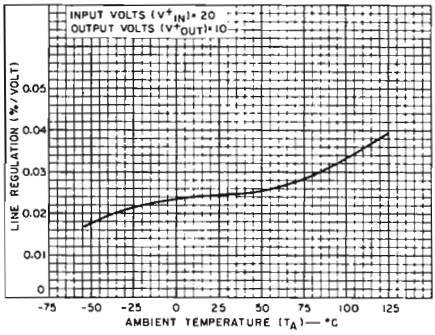


Fig.10—Line regulation temperature characteristics.

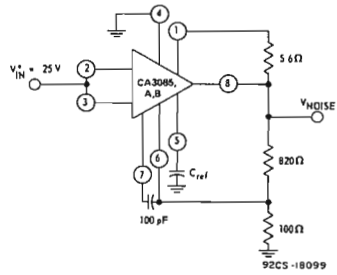


Fig.11—Test circuit for noise voltage.

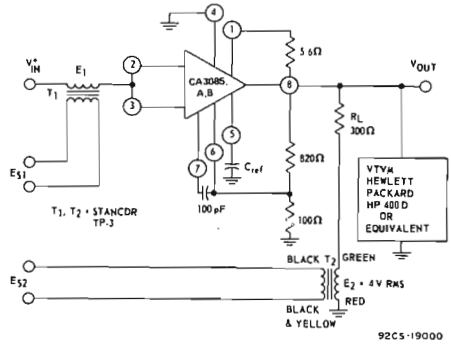


Fig.12—Test circuit for ripple rejection and output resistance.

TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

Output Resistance

Conditions:

1. V_{IN} = +26V, C_{REF} = 0, Short E_1
2. Set E_{S2} at 1kHz so that E_2 = 4V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP4000 or equivalent
4. Calculate R_{OUT} from $R_{OUT} = V_{OUT}(R_L/E_2)$

Ripple Rejection — I

Conditions:

1. V_{IN} = +25V, C_{REF} = 0, Short E_2
2. Set E_{S1} at 1kHz so that E_1 = 3V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP4000 or equivalent
4. Calculate Ripple Rejection from 20log (E_1/V_{OUT})

Ripple Rejection — II

Conditions

1. Repeat Ripple Rejection I with C_{REF} = 2 μF

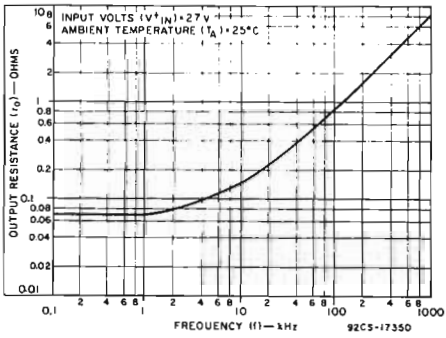


Fig.13—r_o vs. f.

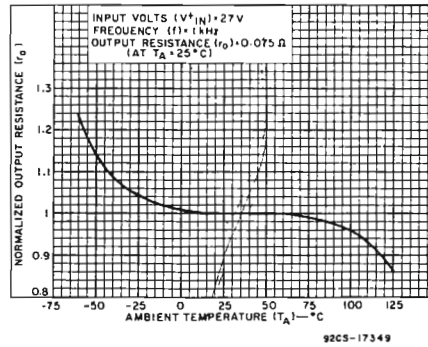


Fig.14—Normalized r_o vs. T_A.

TEST CIRCUIT AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

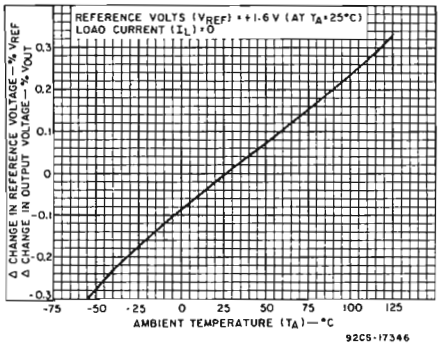


Fig.15—Temperature coefficient of V_{REF} and V_{OUT}.

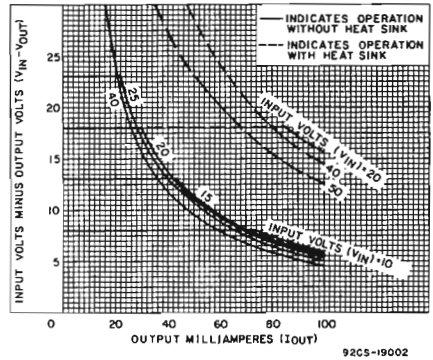


Fig.17—Dissipation limitation (V_{IN}—V_{OUT} vs. I_{OUT}).

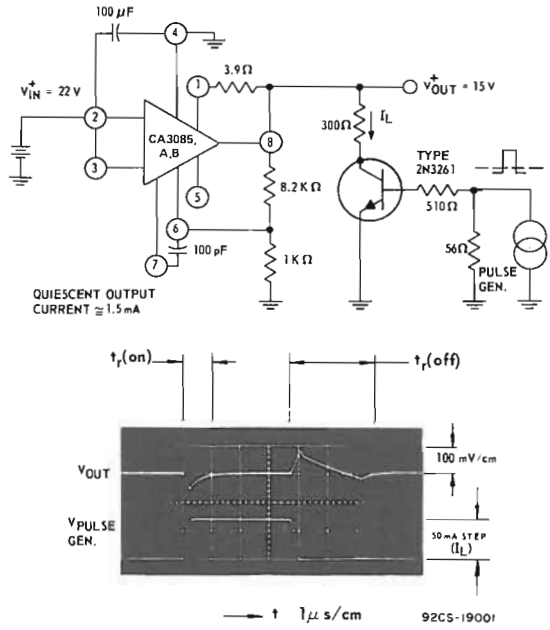


Fig.16—Turn-on and turn-off recovery time test circuit with associated waveforms.

TYPICAL REGULATOR CIRCUITS USING THE CA3085 SERIES

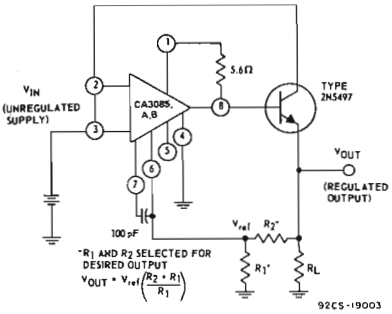


Fig.18—Typical high-current voltage regulator circuit.

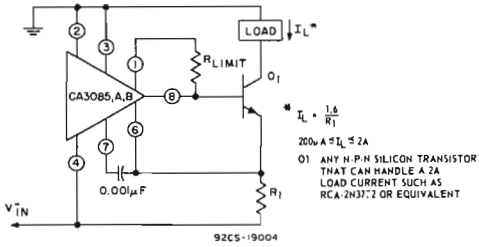


Fig.19—Typical current regulator circuit.

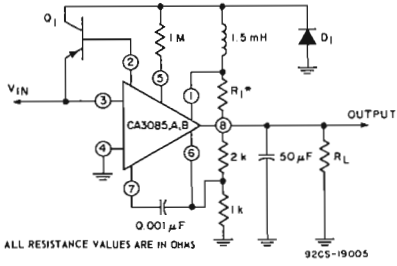


Fig.20—Typical switching regulator circuit.

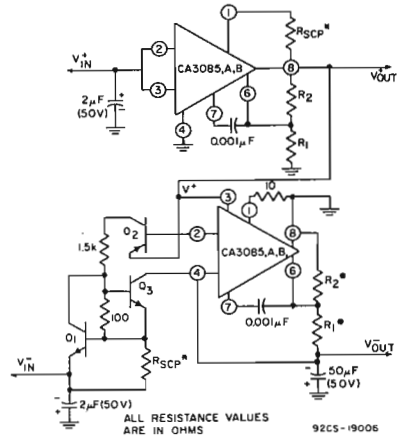


Fig.21—Combination positive and negative voltage regulator circuit.

RCA Solid State Division

Linear Integrated Circuits

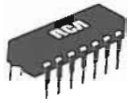
Monolithic Silicon

CA3086 CA3086F

14-Lead Dual-In-Line Frit-Seal (Hermetic) Package

H-1806

14-Lead Dual-In-Line Plastic Package



H-1517

General-Purpose N-P-N Transistor Array

Three Isolated Transistors and One Differentially–Connected Transistor Pair

For Low–Power Applications from DC to 120MHz

Applications

- General-purpose use in signal processing systems operating in the DC to 120-MHz range
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.

RCA-CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120 MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

The CA3086 is supplied in a 14-lead dual-in line plastic package. The CA3086F is supplied in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

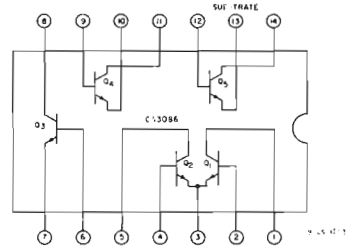


Fig.1 – Functional diagram of the CA3086.

MAXIMUM RATINGS, Absolute–Maximum Values at T_A = 25°C

DISSIPATION:		
Any one transistor	300	mW
Total package up to T_A = 55°C	750	mW
Above T_A = 55°C	derate linearly 6.67	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	–55 to + 125	°C
Storage	–65 to + 150	°C
LEAD TEMPERATURE (During soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) From case for 10 seconds max.	+ 265	°C
The following ratings apply for each transistor in the device:		
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	15	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	20	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}*	20	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5	V
COLLECTOR CURRENT, I_C	50	mA

* The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesireble coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS			UNITS
			Typ. Characteristic Curves Fig. No.	Min.	Typ.	Max.	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	2	–	0.002	100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	3	—	See Curve	5	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 1mA	4	40	100	–	

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

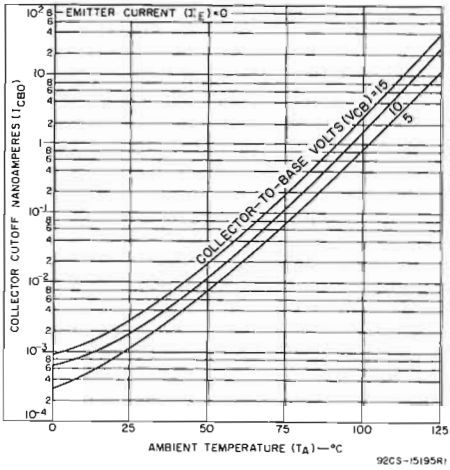


Fig.2– I_{CBO} vs T_A.

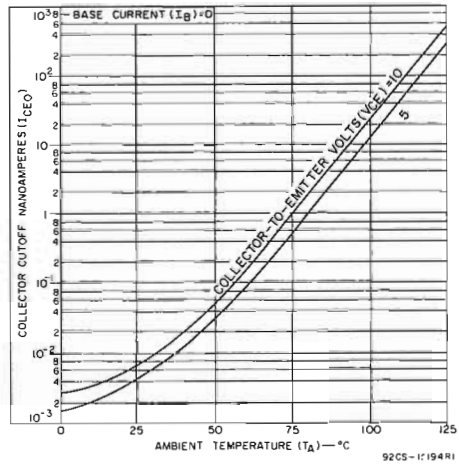


Fig.3– I_{CEO} vs T_A.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$
Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ. Characteristics Curves Fig. No.	TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V	I_C = 10 mA	4	100	
			I_C = 10 μA	4	54	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V	I_E = 1 mA	5	0.715	V
			I_E = 10 mA	5	0.800	V
V_{BE} Temperature Coefficient	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1mA		6	–1.9	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_B = 1mA, I_C = 10mA		–	0.23	V
Noise Figure (low frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, R_S = 1k Ω		–	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		7	100	–
Short-Circuit Input Impedance	h_{ie}			7	3.5	kΩ
Open-Circuit Output Impedance	h_{oe}			7	15.6	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}			7	1.8×10^{-4}	–
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 3V, I_C = 1mA		8	31 – j1.5	mmho
Input Admittance	Y_{ie}			9	0.3 + j0.04	mmho
Output Admittance	Y_{oe}			10	0.001 + j0.03	mmho
Reverse Transfer Admittance	Y_{re}			11	See Curve	–
Gain-Bandwidth Product	f_T	V_{CE} = 3V, I_C = 3mA		12	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0		–	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0		–	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0		—	2.8	pF

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

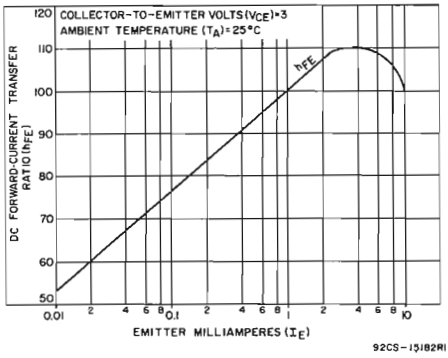


Fig.4 – h_{FE} vs I_E.

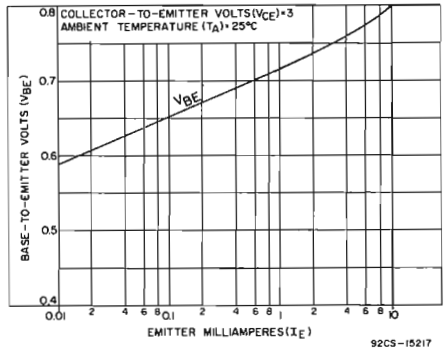


Fig.5 – V_{BE} vs I_E.

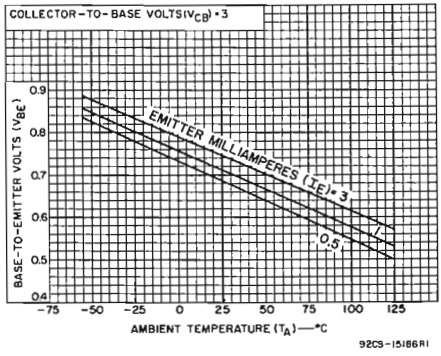


Fig.6 – V_{BE} vs T_A.

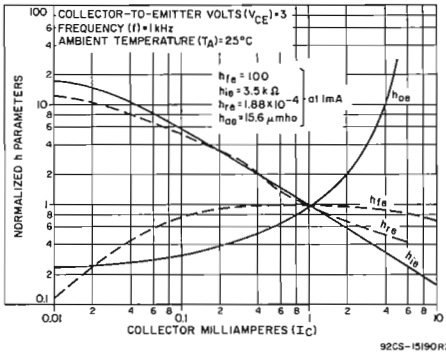


Fig.7 – Normalized h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C.

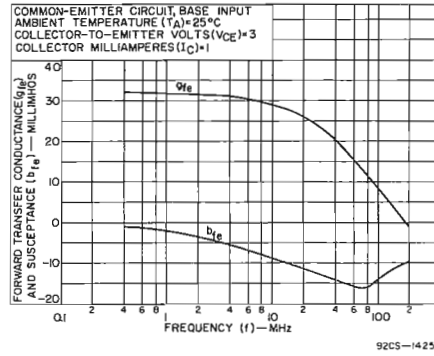


Fig.8 – y_{fe} vs f.

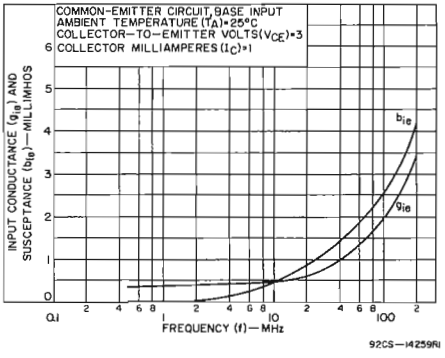


Fig.9 – y_{ie} vs f.

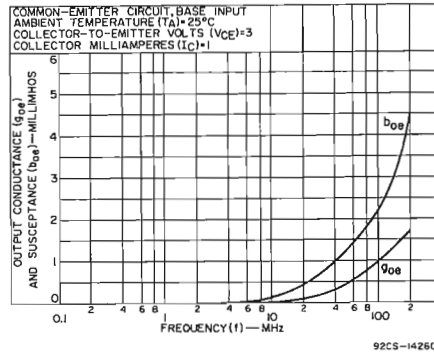


Fig.10 – y_{oe} vs f.

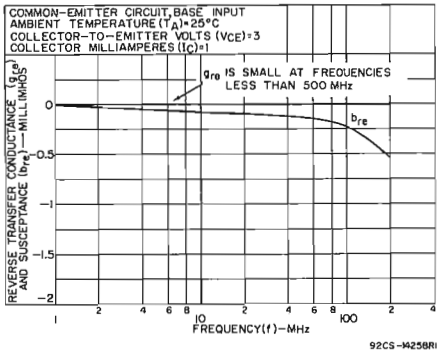


Fig.11 – y_{re} vs f.

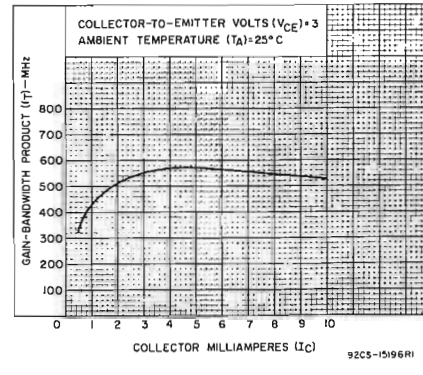


Fig.12 – f_T vs I_C.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3088E

H-1622

16-Lead Dual-In-Line Plastic Package

AM Receiver Subsystem

Includes: AM Converter, IF Amplifiers, Detector and Audio Preamplifier

For Applications in a Variety of AM Broadcast and Communications Receivers and Applications Requiring an Array of Amplifiers

Features:

- Excellent overload characteristics
- AGC for IF amplifier
- Buffered output signal for tuning meter
- Low harmonic distortion (THD)
- Delayed AGC for RF amplifier
- Terminals for optional inclusion of tone control
- Internal Zener diode provides voltage regulation
- Two IF amplifier stages
- Low-noise converter and first IF amplifier
- Operates from wide range of power supplies: $V^+ = 6$ to 16 volts
- Optional AC and/or DC feedback on wide-band amplifier
- Array of amplifiers for general-purpose applications
- Suitable for use with optional external RF stage, either MOS or bipolar

RCA-CA3088E*, a monolithic integrated circuit, is an AM subsystem that provides the converter, IF amplifier, detector, and audio preamplifier stages for an AM receiver.

The CA3088E also provides internal AGC for the first IF amplifier stage, delayed AGC for an optional external RF amplifier, a buffer stage to drive a tuning meter, and terminals facilitating the optional use of a tone control.

Fig. 2 is a functional diagram of the CA3088E. The signal from the low-noise converter is applied to the first IF amplifier and is then coupled to the second IF amplifier. This IF signal is then detected and externally filtered. The resultant audio signal is applied to an audio preamplifier. Optionally, a tone control circuit may be connected at the junction of the detector circuit and the audio preamplifier. The gain of the first IF amplifier stage is controlled by an internal AGC circuit. The CA3088E supplies a delayed AGC signal output for use with an external RF amplifier. A buffered output signal is also available for driving a tuning meter. A DC voltage, internally regulated by a Zener diode, supplies the second IF amplifier, the AGC and tuning meter circuits and may also be used with any other stage.

The CA3088E features four independent transistor amplifiers, each incorporating internal biasing for temperature tracking. These amplifiers are particularly useful in general-purpose amplifier, oscillator, and detector applications in a wide variety of equipment designs.

*Formerly Developmental Type TA5842.

MAXIMUM RATINGS, *Absolute Maximum Values, at* $T_A = 25^oC$

DC SUPPLY VOLTAGE:		
Across Term. 5 and Terms. 3, 6, 13, 16, respectively	16	V
DC CURRENT:		
At Terms. 3, 6, 13, 16, respectively	10	mA
At Term. 10	30	mA
DEVICE DISSIPATION:		
Up to $T_A = 50^oC$	760	mW
Above $T_A = 50^oC$	derate linearly 7.6	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS T_A = 25°C, V+ = 12 V	TEST CIRCUIT FIG. NO.	TYPICAL VALUES	UNITS
Static (DC) Characteristics					
DC Voltages:					
Terms. 1, 4, 9, 11	$V_{1, 4, 9, 11}$		1	0.7	V
Terms. 2, 7, 8	$V_{2, 7, 8}$			1.4	V
Term. 10	V_{10}			5.6	V
Term. 12	V_{12}			0	V
Term. 15	V_{15}			3.5	V
DC Current:					
Term. 3	I_3		1	0.35	mA
Term. 6	I_6			1.0	mA
Term. 10	I_{10}			20	mA
Term. 13	I_{13}			0	mA
Term. 16	I_{16}			1.2	mA
Dynamic Characteristics					
Detector Output		30% Modulation	4	75	mV RMS
Audio Amplifier Gain	A_{AF}	f = 1 kHz	4	30	dB
Audio Distortion		V_{OUT} = 100 mV	4	0.2	%
Sensitivity:		f_{IN} = 1 MHz			
At Converter Stage Input		Signal-to-Noise Ratio (S/N) = 20 dB	2	200	μV/m
At RF Stage Input			4	100	μV/m
Total Harmonic Distortion	THD	30% Modulation	4	1.0	%
Input Resistance:	R_I	No AGC, Input signal frequency (f_{IN}) = 1 MHz			
At Transistor Q1				3500	Ω
At Transistor Q5				2000	Ω
Input Capacitance:	C_I				
At Transistor Q1				12	pF
At Transistor Q5				17	pF
Feedback Capacitance:	C_{FB}				
At Transistor Q1				1.5	pF
At Transistor Q5				1.5	pF

The typical characteristics for the CA3088E are intended for guidance purposes in evaluating this device for equipment design.

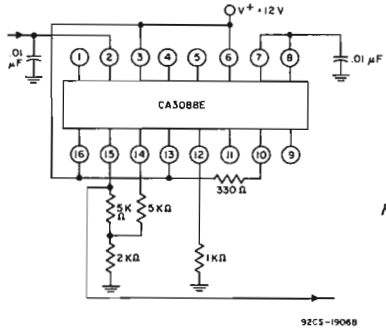


Fig.1—Test circuit for DC characteristics.

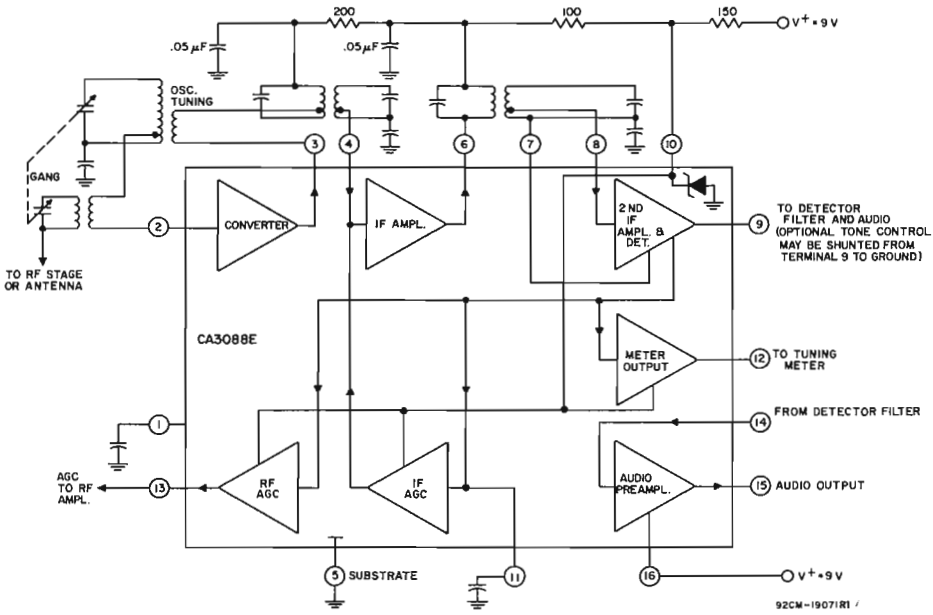


Fig.2—Functional block diagram of the CA3088E.

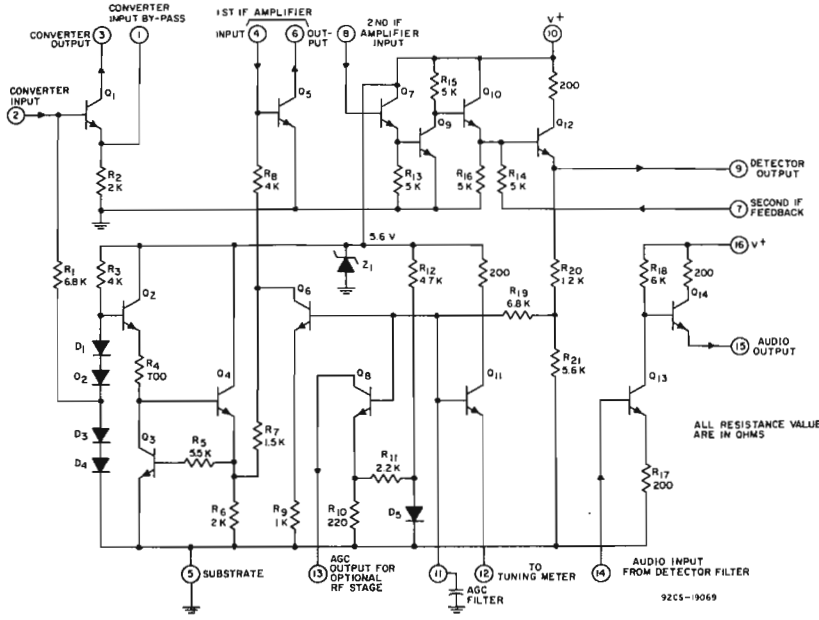


Fig.3—Schematic diagram of the CA3088E.

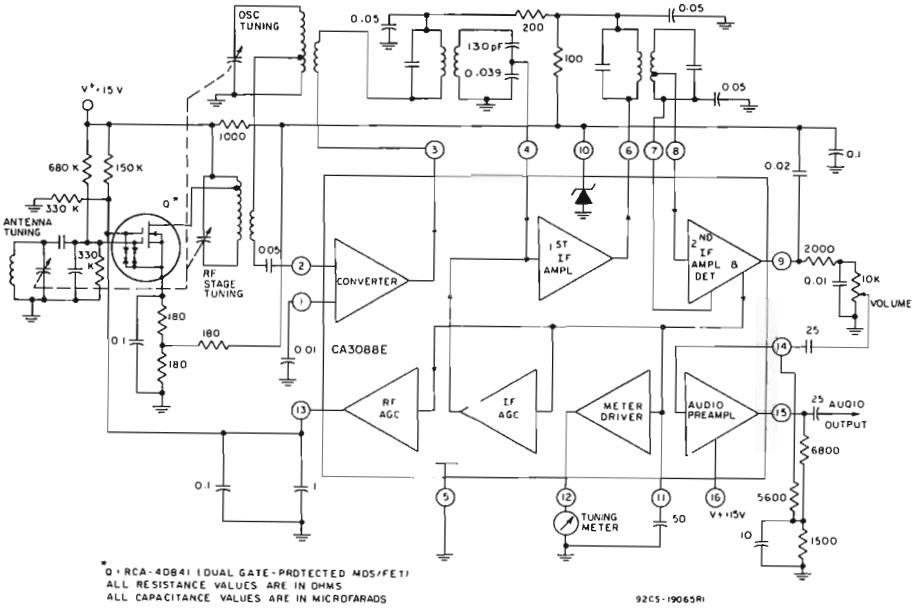


Fig.4–Typical AM broadcast receiver using the CA3088E with optional RF amplifier stage.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3089E

16-Lead Dual-in-Line Plastic Package

FM IF System

Includes———IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Muting (Squelch), and Tuning Meter

For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers

Features:

- Exceptional limiting sensitivity: 12 μV typ. at −3 dB point
- Low distortion: 0.1% typ. (with double-tuned coil)
- Single-coil tuning capability
- High recovered audio: 400 mV typ.
- Provides specific signal for control of interchannel muting (squelch)
- Provides specific signal for direct drive of a tuning meter
- Provides delayed AGC voltage for RF amplifier
- Provides a specific circuit for flexible AFC
- Internal supply-voltage regulators

RCA-CA3089E* is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Fig. 1 is a block diagram showing the CA3089E features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3089E is ideal for high-fidelity operation. Distortion in a CA3089E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

* Formerly Developmental Type No. TA5628.

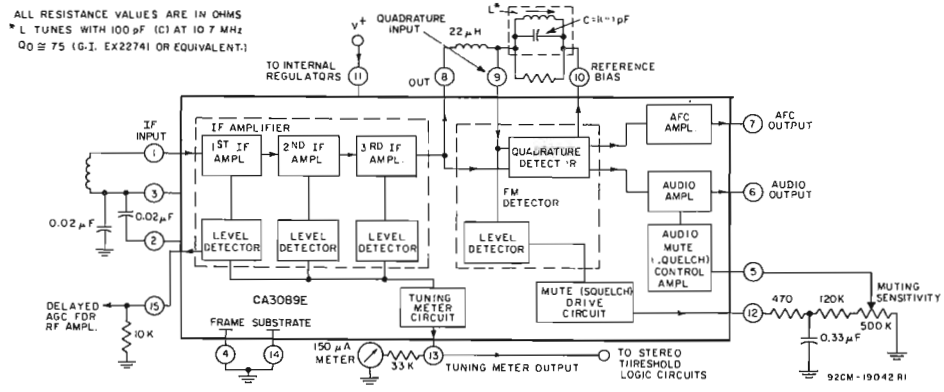


Fig. 1-Block diagram of the CA3089E.

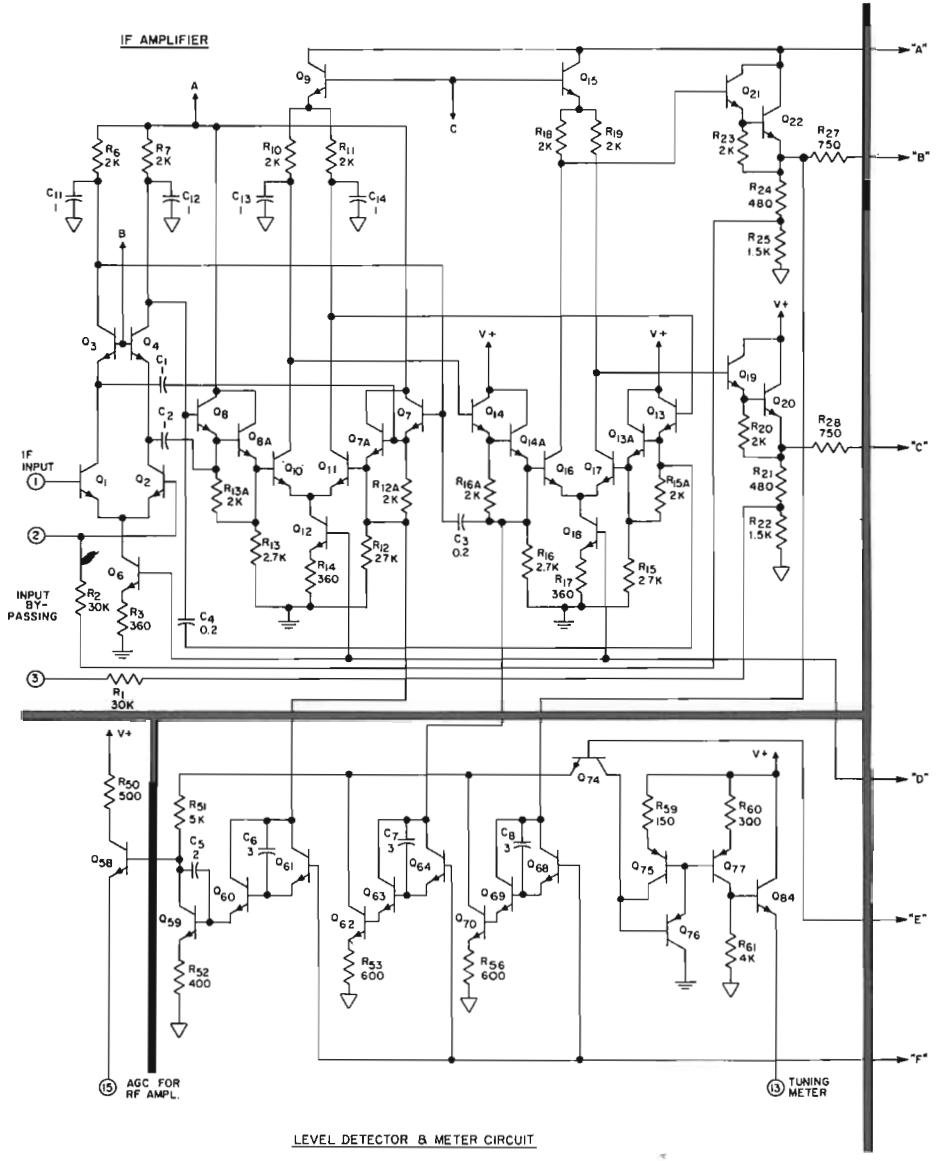


Fig.2-Schematic diagram of the CA3089E.

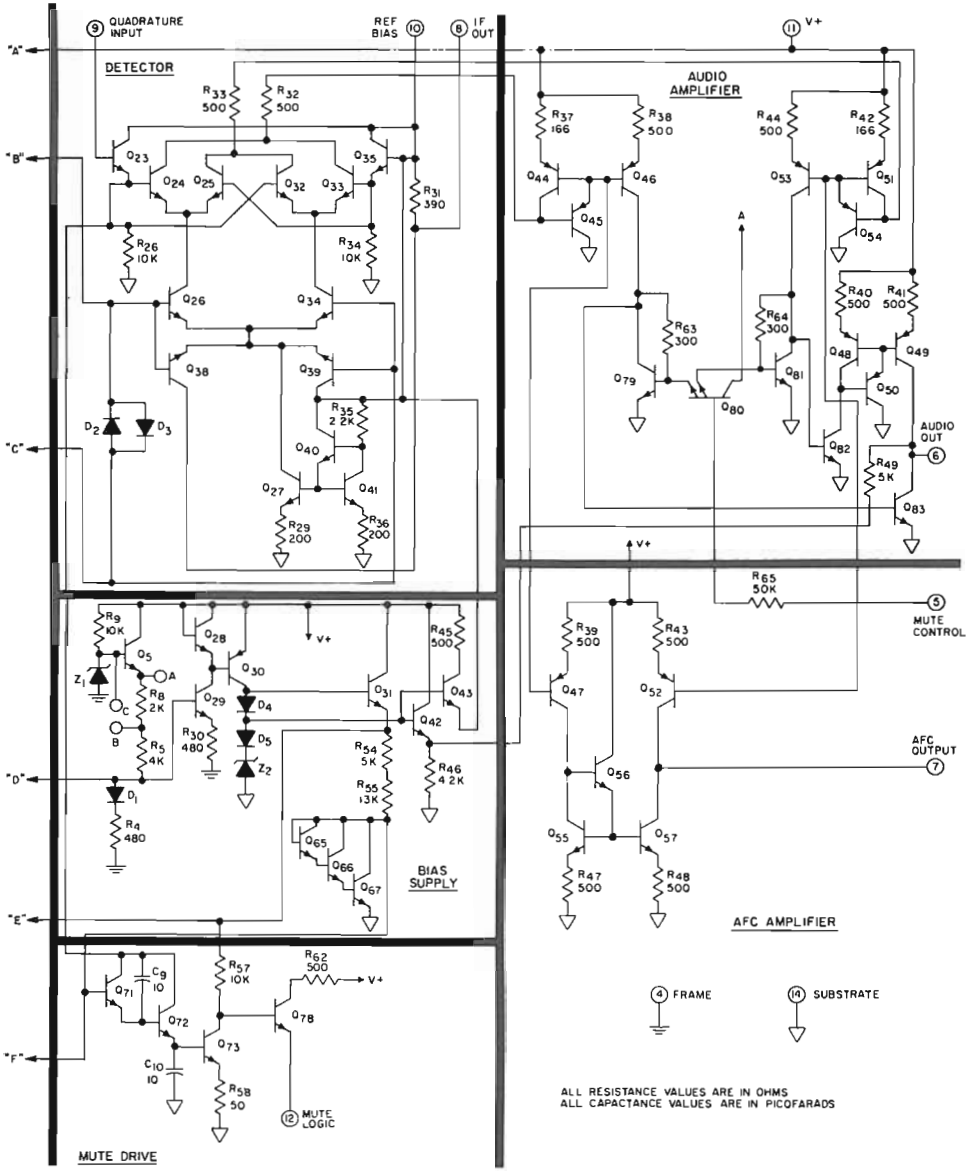


Fig.2-Schematic diagram of the CA3089E.

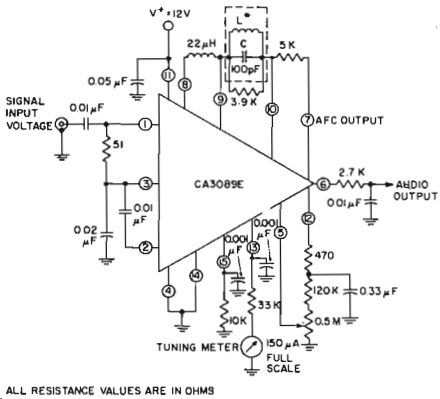
MAXIMUM RATINGS, *Absolute Maximum Values, at $T_A = 25^oC$*

DC Supply Voltage:		
Between Terminals 11 and 4	16	V
Between Terminals 11 and 14	16	V
DC Current (out of Terminal 15)	2	mA
Device Dissipation:		
Up to $T_A = 60^oC$	600	mW
Above $T_A = 60^oC$	derate linearly 6.7 mW/^oC	
Ambient Temperature Range:		
Operating	−55 to +125	^oC
Storage	-65 to +150	^oC
Lead Temperature (During Soldering):		
At distance not less than 1/32" (0.79mm) from case for 10 seconds max.	+265	^oC

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$, $V^+ = 12$ Volts

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		Circuit Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
Static (DC) Characteristics								
Quiescent Circuit Current	I_{11}	No signal input, Non muted		3, 4	16	23	30	mA
DC Voltages:								
Terminal 1 (IF Input)	V_1				1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)	V_2				1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)	V_3				1.2	1.9	2.4	V
Terminal 6 (Audio Output)	V_6				5.0	5.6	6.0	V
Terminal 10 (DC Reference)	V_{10}				5.0	5.6	6.0	V
Dynamic Characteristics								
Input Limiting Voltage (-3 dB point)	V_I(lim)	—		3, 4	—	12	25	μV
AM Rejection (Term. 6)	AMR	V_{IN} = 0.1V, AM Mod. = 30%	f_0 = 10.7 MHz,		45	55	—	dB
Recovered AF Voltage (Term. 6)	V_O(AF)				300	400	500	mV
Total Harmonic Distortion: *		V_{IN} = 0.1 V	$f_{mod.}$ = 400 Hz, Deviation = ±75 kHz					
Single Tuned (Term. 6)	THD			3	—	0.5	1.0	%
Double Tuned (Term. 6)	THD			4	—	0.1	—	%
Signal plus Noise to Noise Ratio (Term. 6)	S + N/N			3, 4	60	67	—	dB

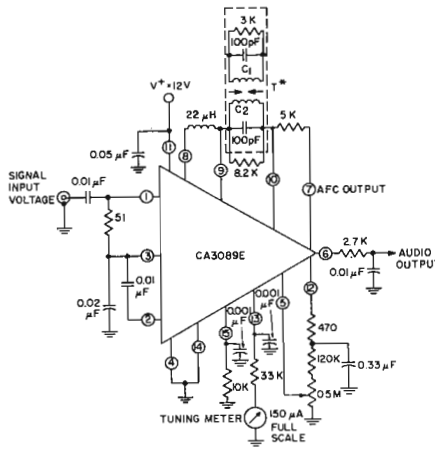
* THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.



ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O(UNLOADED) ≅ 75 (G.I. AUTOMATIC MFG DIV. EX22741 OR EQUIVALENT)

92CM-19041R1

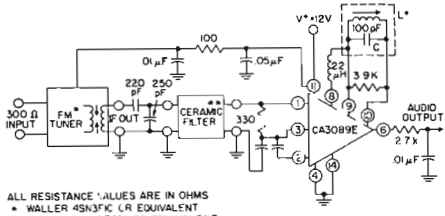
Fig.3-Test circuit for CA3089E using a single-tuned detector coil.



ALL RESISTANCE VALUES ARE IN OHMS
* T: PRI. – Q_O(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C1) 20 t OF 34s ON 7/32" DIA. FORM
SEC. – Q_O(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C2) 20 t OF 34s ON 7/32" DIA. FORM
kQ (PERCENT OF CRITICAL COUPLING) ≅ 70%
(ADJUSTED FOR COIL VOLTAGE V_C) = 150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4 mm

92CM-19041R1

Fig.4-Test circuit for CA3089E using a double-tuned detector coil.



ALL RESISTANCE VALUES ARE IN OHMS
* WALLER 4SN3FC LR EQUIVALENT
** MURATA SFG 10.7MA OR EQUIVALENT
* L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O UNLOADED ≅ 75 (G.I EX22741 OR EQUIVALENT)

92CS-19045

Performance data at f_o = 98 MHz, f_{MOD} = 400 Hz, Deviation = ±75 kHz:

-3dB Limiting Sensitivity	2µV (Antenna Level)
20dB Quieting Sensitivity	1µV (Antenna Level)
30dB Quieting Sensitivity	1.5µV (Antenna Level)

Fig.5-Typical FM tuner using the CA3089E with a single-tuned detector coil.

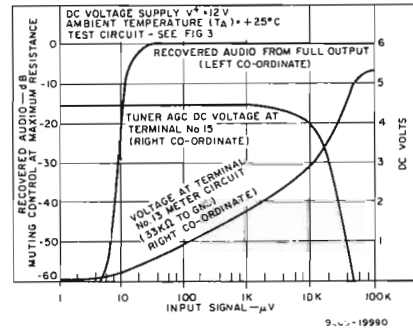


Fig.6-Muting action, tuner AGC, and tuning meter output as a function of input signal voltage.

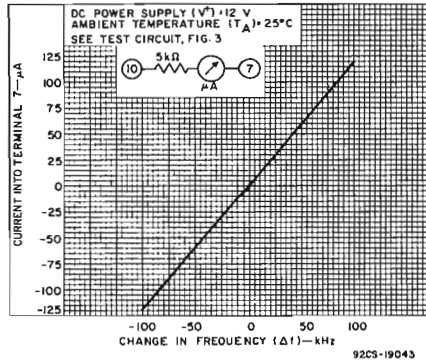
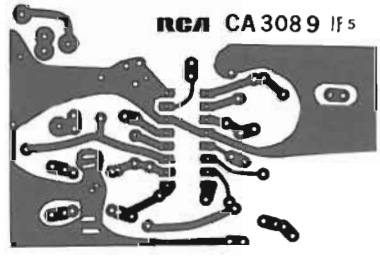
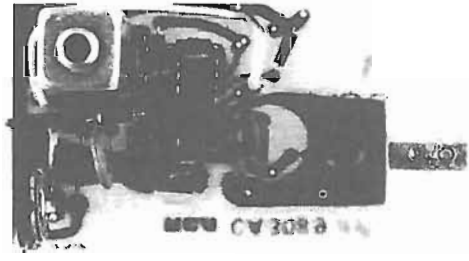


Fig.7-AFC characteristics (current at Term. 7 as a function of change in frequency).



a) Bottom view of printed-circuit board.



b) Component side — top view.

Fig.8-Actual size photographs of the CA3089E and outboard components mounted on a printed-circuit board.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3090AQ

16-Lead quad-in-line plastic package

H-1706

Stereo Multiplex Decoder

For FM Stereo Multiplex Systems

Features:

- Requires the use of only one low-inductance tuning coil
- Automatic stereo switching
- Directly drives a stereo indicator lamp up to 100 mA
- Includes driver for stereo-lamp indicator
- Operates from a wide range of power supplies: 10 to 16 volts
- Requires only one adjustment for alignment
- Switching from monaural to stereo and stereo to monaural produces no audible thumps
- Low distortion: under 0.22% (typ.)
- Separate dc input permits stereo defeat or enable
- High signal output: directly drives audio amplifiers
- Excellent SCA (storecast) rejection: 55 dB typ.
- High audio channel separation: 40 dB typ.

RCA-CA3090AQ*, a monolithic silicon integrated circuit, is a stereo multiplex decoder intended for FM multiplex systems.

The CA3090AQ is the successor to the CA3090Q; it offers three major advantages over the CA3090Q as follows:

1. Can directly drive a stereo indicator lamp with a current drain of up to 100 mA.
2. Stereo Defeat/Enable control-voltage specifications.
3. Capable of operation with lower distortion.

This stereo multiplex decoder requires only one low-inductance tuning coil (requires only one adjustment for complete alignment), provides automatic stereo switching, energizes a stereo indicator lamp, and operates from a wide range of voltage supplies.

Figure 1 shows the block diagram for the CA3090AQ. The input signal from the detector is amplified by a low-distortion preamplifier and simultaneously applied to both the 19-kHz and 38-kHz synchronous detectors. A 76-kHz signal, generated by a local voltage-controlled oscillator (VCO), is counted down by two frequency dividers to a 38-kHz signal and to two 19-kHz signals in phase quadrature. The 19-kHz pilot-tone supplied by the FM detector is compared to the locally generated 19-kHz signal in a synchronous detector. The resultant signal controls the voltage controlled oscillator (VCO) so that it produces an output signal to phase-lock the stereo decoder with the pilot tone. A second synchronous detector compares the locally generated 19-kHz signal with the 19-kHz pilot tone. If the pilot tone exceeds an externally adjustable threshold voltage, a Schmitt trigger circuit is energized. The signal from the Schmitt trigger lights the stereo indicator, enables the 38-kHz synchronous detector, and automatically switches the CA3090AQ from monaural to stereo operation. The output signal from the 38-kHz detector and the composite signal from the preamplifier are applied to a matrixing circuit from which emerge the resultant left and right channel audio signals. These signals are applied to their respective left and right post amplifiers for amplification to a level sufficient to drive most audio amplifiers.

The CA3090AQ may be used without the stereo defeat/enable function (see Fig. 6) if a control voltage for this function is not readily available. In this case, Terminal 4 should be grounded.

The CA3090AQ utilizes the 16-lead quad-in-line plastic package and operates over the ambient temperature range of −55°C to +125°C.

* Formerly Developmental Type No. TA6262G.

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^{\circ}C$

DC SUPPLY VOLTAGE	16 V
CURRENT AT TERM. 12	100 mA
INPUT SIGNAL VOLTAGE (COMPOSITE)■	400 mV
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance not less than 1/32" (0.79 mm) from case for 10 s max.	+265°C

■ For stereo operation, a minimum input signal voltage (composite) of 40 mV is required.

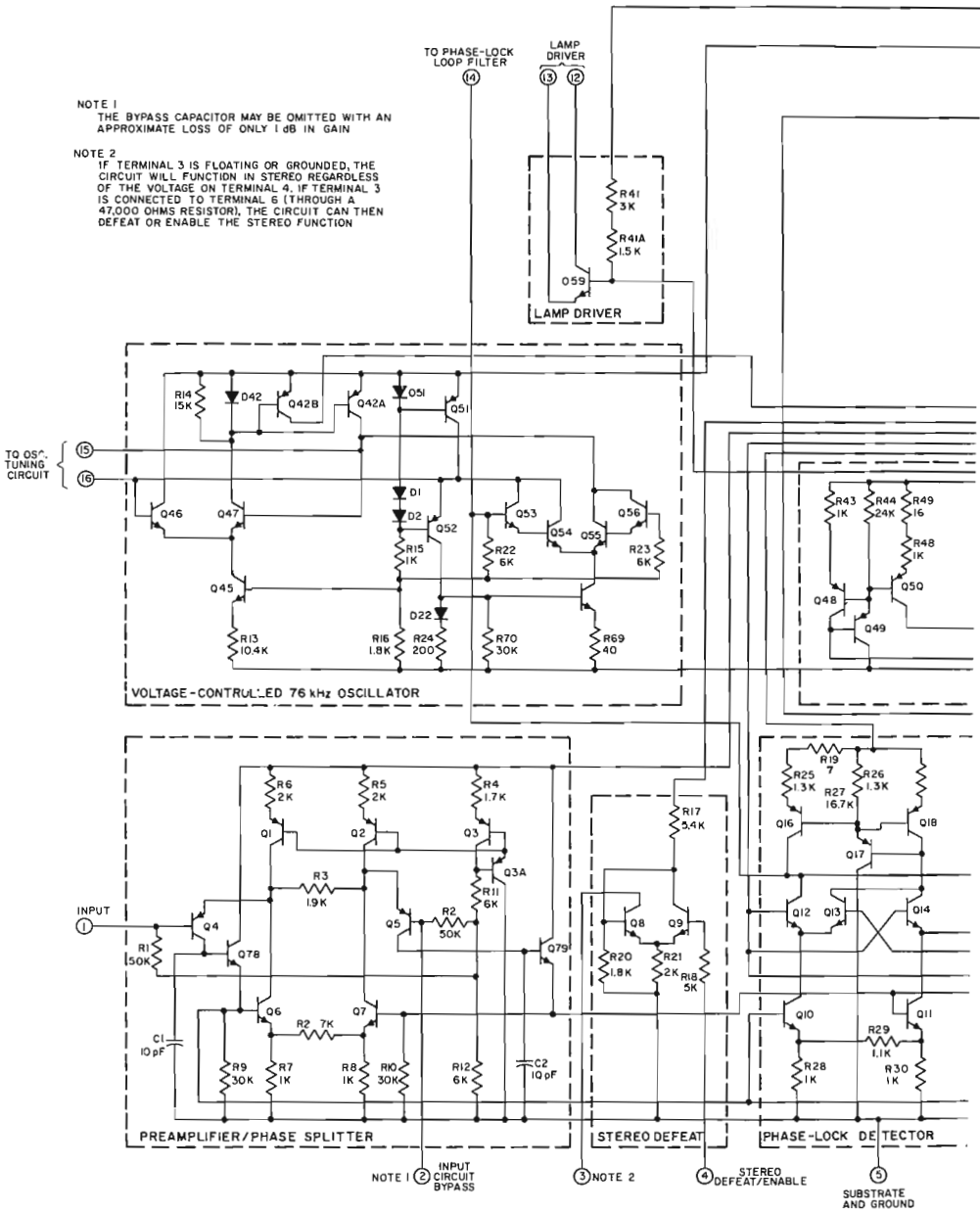


Fig. 1 — Schematic diagram of CA3090AQ.

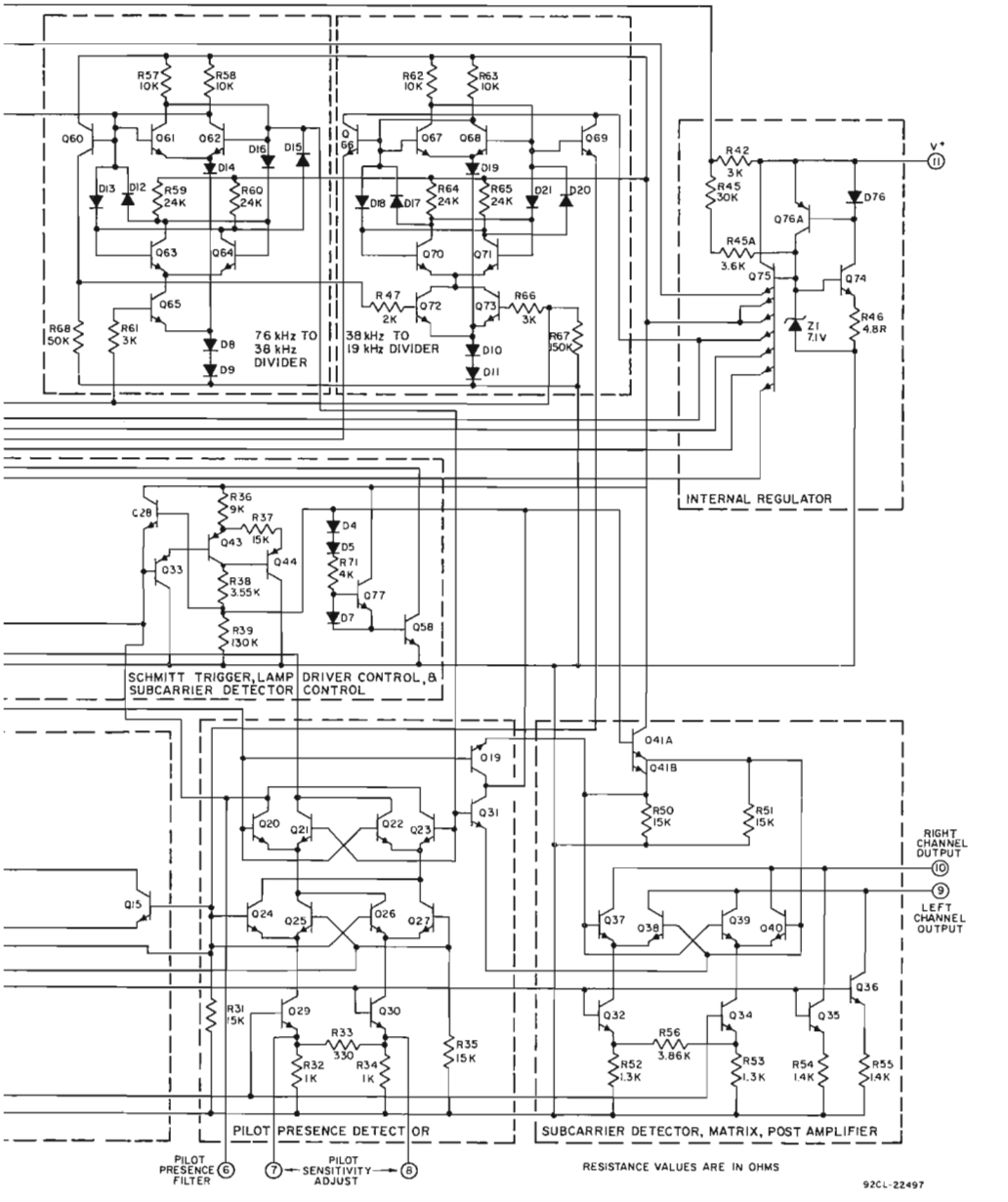


Fig. 1 – Schematic diagram of CA3090AQ.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TERMINAL MEASURED AND SYMBOL	TEST CONDITIONS $T_A = 25^\circ C$, $V+ = 12$ V (unless specified otherwise)	LIMITS Min.	Typ.	Max.	UNITS
Static Characteristics						
Total Current (Terms. 9, 10, 11)	I_{total}	Lamp OFF	–	22	27	mA
DC Voltage: Term. 1	V_1		1.6	2.3	3.1	V
Term. 6 (Indicator Lamp OFF)	V_6		–	2.1	3.6	V
Terms. 9 and 10	$V_{9\ \&\ 10}$		4.7	6.4	8.4	V
Term. 12 (Indicator Lamp OFF)	V_{12}	$V^+ = 16$ V	12.7	–	–	V
Voltage Differential (Term. 2–Term. 1)	$V_2 - V_1$		–	0	0.1	V
Current at Term. 12 (In actual use external circuit resistance (e.g. lamp should limit Term. 12 to the maximum rated value of 100 mA.)		V_{IN} (at f = 19 kHz) = 18 mV	75	100	–	mA
Dynamic Characteristics						
Input Impedance	Z_{IN}		–	50k	–	Ω
Channel Separation (L + R Reference)*		V_{IN} = 180 mV	25	40	–	dB
Channel Balance (Monaural)			–	0.3	3	dB
Monaural Gain			3	6	9	dB
Stereo/Monaural Gain Ratio*			–	±0.3	±3	dB
Indicator Lamp – Turn-ON Voltage		19-kHz pilot-tone @ Term. 1	–	4	–	mV
Capture Range (Deviation from 76-kHz center frequency)		19-kHz pilot-tone voltage = 18 mV	±6.6	±10	–	%
Distortion (75-μs de-emphasis): 2nd Harmonic		V_{IN} = 240 mV	–	0.2	–	%
3rd, 4th, and 5th Harmonic			–	<0.1	–	%
19-kHz Rejection			–	35	–	dB
38-kHz Rejection			–	48	–	dB
SCA (storecast) Rejection			–	70	–	dB
Stereo Defeat Voltage (V_4)			–	1.2	<0.9	V
Stereo Enable Voltage (V_4)			>1.6	1.2	–	V

* For stereo operation, test conditions require a composite stereo input signal (modulated at 1 kHz) including a 19-kHz (18 mV) pilot-tone signal.

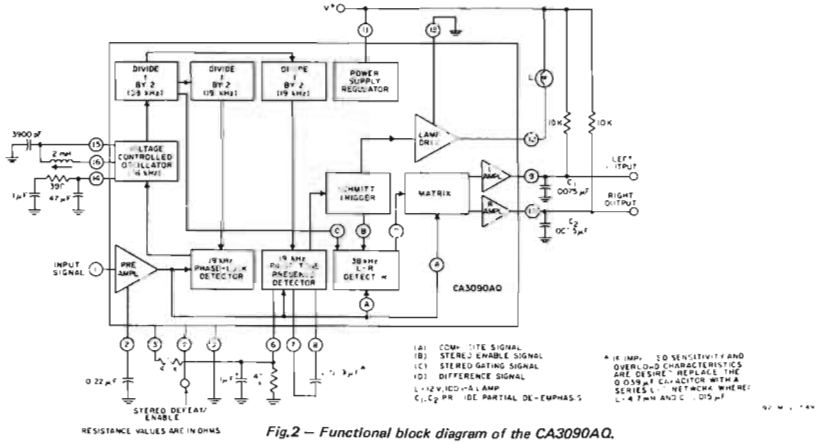


Fig. 2 – Functional block diagram of the CA3090AQ.

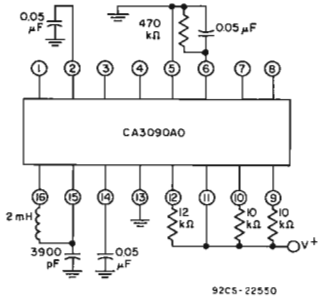


Fig. 3 – Test circuit for DC characteristics.

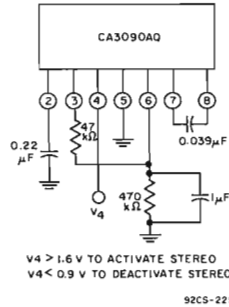


Fig. 5 – Test circuit for use with stereo defeat/enable.

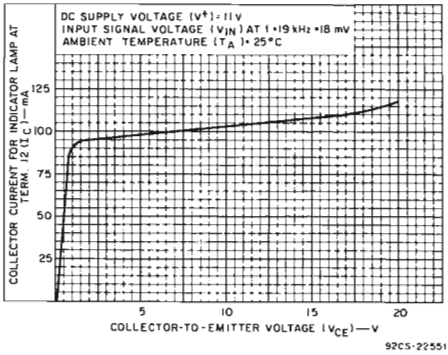


Fig. 4 – Indicator lamp characteristics (I_C vs. V_{CE}).

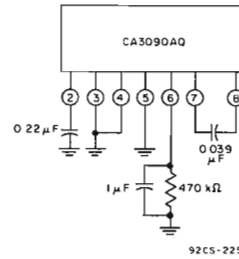


Fig. 6 – Test circuit for use without stereo defeat/enable.

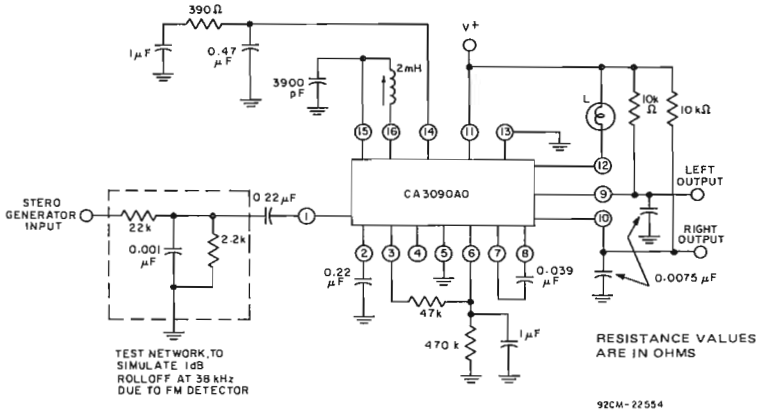


Fig. 7 — Test circuit for measurement of dynamic characteristics.

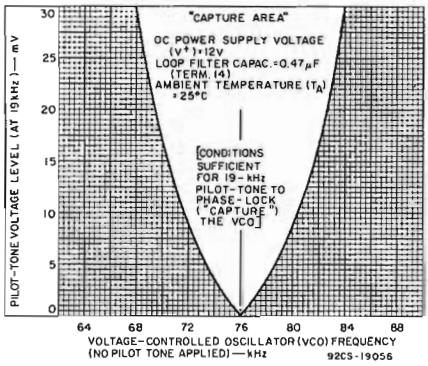


Fig. 8 — Pilot-tone voltage level vs. VCO frequency with no pilot-tone applied.

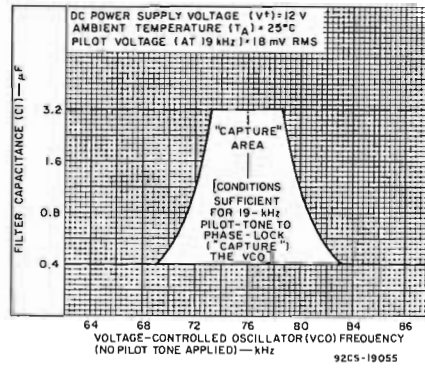
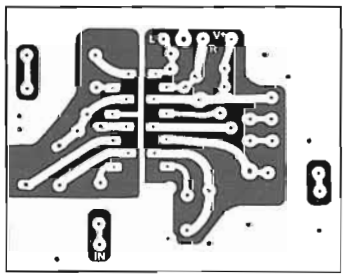
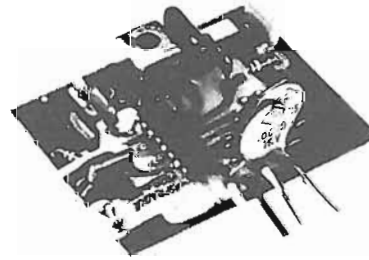


Fig. 9 — Filter capacitance vs. VCO frequency with no pilot-tone applied.



A—Foil side.



B—Component side.

Fig. 10 — Photographs of the CA3090AQ and outboard components mounted on a 2 X 2½-inch printed-circuit board to constitute a complete stereo multiplex decodar.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA3091D

14-Lead Dual-In-Line
Ceramic Package

Four-Quadrant Multiplier

Applications:

- Multiplier ■ Divider ■ Squarer ■ Square Rooter
- Power-series approximator
- Full-wave rectifier
- Automatic level controller
- RMS converter
- Frequency discriminator
- Voltage-controlled filters and oscillators

RCA-CA3091D*, a monolithic silicon integrated circuit, is a four-quadrant multiplier that provides an output voltage that is the product of two input (x and y) voltages.

This device functions as a multiplier, divider, squarer, square rooter, and power-series approximator. In addition, this device is useful in applications such as ideal full-wave rectifiers, automatic level controllers, RMS converters, frequency discriminators, and voltage-controlled filters and oscillators.

The CA3091D comprises five basic circuits (See Fig. 1), including: a multiplier block, two linearity compensators, a current converter, a current source for biasing, and a regulator (reference voltage). A brief description of the operation, functions and typical applications is given in the section "Operating Considerations". In addition there is a separate section on "Symbols, Terms, and Definitions" that defines the terms and symbols used throughout the data bulletin.

The CA3091D is supplied in 14-lead dual-in-line ceramic package and operates over the full military temperature range of -55°C to +125°C.

* Formerly Developmental Type TA5855A.

Features:

- "Accuracy": ±4% (max.)
- "Linearity": 3.0% (max.)
- Feedthrough: 9 mV p-p (typ.)
- 3-db bandwidth: 4.4 MHz
- Low power operation capability: ±6.0 V, 4 mW drain
- Low power-supply sensitivity: 36 mV/V typ.
- Smooth overload characteristics — no foldback if full-scale input signal is exceeded
- Negligible warm-up drift
- Broadband operation capability (flat to 1 MHz) — both inputs have similar characteristics for reduced high-frequency phase shift between the inputs
- Low-level linearity correction circuitry minimizes low-level feedthrough for improved small-signal accuracy
- All multiplication is performed with widebend circuitry — this permits two signals of frequencies much higher than the -3 db frequency of the multiplier to produce a difference frequency that is within the multiplier's bandwidth
- High immunity to parasitic oscillation
- Essentially free from excess peaking — provides improved frequency response
- Requires no level shifting at the output — current-source operation at the output permits output signal to be referenced to ground or other levels within the output voltage swing capabilities of the multiplier
- Internal bias regulator

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DC Supply Voltages:		
Between Terms. 12 and 1	+18	V
Between Terms. 4 and 1	−18	V
DC Supply Currents:		
At Term. 12 with DC Supply Voltage = +15 V	4	mA
At Term. 4 with DC Supply Voltage = −15 V	16	mA
Bias Current (At Term. 3)	1	mA
* Input Current	±1	mA
Output Short-Circuit Duration	No limitation	
Voltage Reference Current	10	mA
Linearity Correction Currents:		
At Terminals 7 and 8	10	mA
Device Dissipation (Up to 125°C)	200	mW
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (during soldering):		
At distance not less than 1/32 inch (0.79 mm) from case for 10 seconds max.	+265	°C

* External resistance is required to limit the current to the indicated ±1 mA value.

ELECTRICAL CHARACTERISTICS, For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS			UNITS
		$T_A = 25^oC$, $I_{IB} = 0.5$ mA $V^+ = 15$ V, $V^- = -15$ V	Circuit and/or Char. Curve	Min.	Typ.	Max.	
STATIC CHARACTERISTICS							
INPUT CIRCUIT							
Input Balance (Correction) Currents:							
At x Input	I_{IC}	x = 0	–	−20	−2.1	+20	μA
At y Input		y = 0	–	−20	−8.7	+20	μA
Feedthrough Linearity Balance (Correction) Current	I_{OC}		–	−34	−2.9	+34	μA
OUTPUT CIRCUIT							
Output Offset Current	I_{OO}	x & y = 0,	–	−10	−0.23	+10	μA
Output Offset Voltage	V_{OO}	I_{OO} thru $R_L = 33k\Omega$	–	−0.330	−0.0076	+0.330	V
Output Peak Current Swing	$\|I_O\|$	Thru $R_L = 24k\Omega$	3	0.41	0.45	–	mA
Output Peak Voltage Swing	$\|V_O\|$	Across $R_L = 33k\Omega$	4	12	12.9	–	V
DC SUPPLIES & BIASING							
Current Drain (Idling):							
At Term. 4		$V^- = -15$ V	–	–	2.9	4.5	mA
At Term. 12		$V^+ = +15$ V	–	–	2.0	3.0	mA
Reference Voltage	V_{ref}	Measured across Terms. 6 & 4 at I = 1mA	–	5.5	6.1	6.7	V
DYNAMIC CHARACTERISTICS							
Output Current	I_O	With I = 0.2mA at each input	–	–	0.21	0.32	mA
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$			11	0.69	1.0	1.7	
Accuracy		Worst case at 25°C	–	–	2.6	4.0	% of 10 V
Linearity				–	1.7	3.0	
Feedthrough Voltage:							
At y = 20V p-p, x = 0			–	–	9	20	mV p-p
At x = 20V p-p, y = 0			–	–	9	20	

ELECTRICAL CHARACTERISTICS, Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
		T_A = 25°C, I_{IB} = 0.5 mA V^+ = 15 V, V^- = −15 V	Circuit and/or Char. Curve		
STATIC CHARACTERISTICS					
INPUT CIRCUIT					
Input Resistance:					
At x Input	R_I	$\lvert I_x \rvert \leq 0.2$ mA	5	1.3	kΩ
At y Input		$\lvert I_y \rvert \leq 0.2$ mA		0.5	kΩ
Input Capacitance:					
At x Input	C_I	at 1 MHz	–	5.8	pF
At y Input				5.8	pF
OUTPUT CIRCUIT					
Output Resistance	R_O		6	1.0	MΩ
Output Capacitance:	C_O	at 1 MHz		4.0	pF
DC Supply Voltage Sensitivity:					
At Term. 4	$\frac{\Delta V_O}{\Delta V^-}$		11	26	mV/V
At Term. 12	$\frac{\Delta V_O}{\Delta V^+}$			36	mV/V
DYNAMIC CHARACTERISTICS					
Bandwidth (At -3dB point):					
Through x Input	BW		8, 10	4.8	MHz
Through y Input			8, 9	4.4	MHz
3° Error Frequency:					
Through x Input			–	360	kHz
Through y Input				310	kHz
Maximum Slew Rate	SR	7pF in parallel with 10 MΩ load	7	27	V/μs
Temperature Coefficients:					
Output Offset Current	$\Delta I_{OO}/\Delta T$	x & y = O	–	−0.021	μA/°C
x-Input Balance Current	$\Delta I_{IC}/\Delta T$	x = O	–	−0.063	μA/°C
y-Input Balance Current		y = O	–	−0.063	μA/°C
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$	k_N		–	−0.76	%/%/°C
Accuracy			–	0.11	%/°C
Linearity			–	0.06	%/°C
Feedthrough:					
At x = O			–	5.6	mV/°C
At y = O				5.7	mV/°C

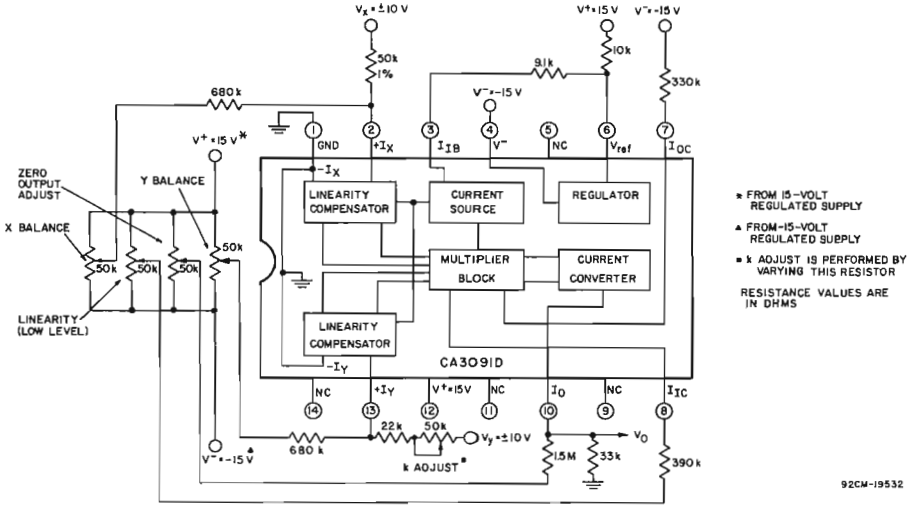


Fig.1—Functional block diagram of CA3091D with typical multiplier outboard(peripheral)circuitry.

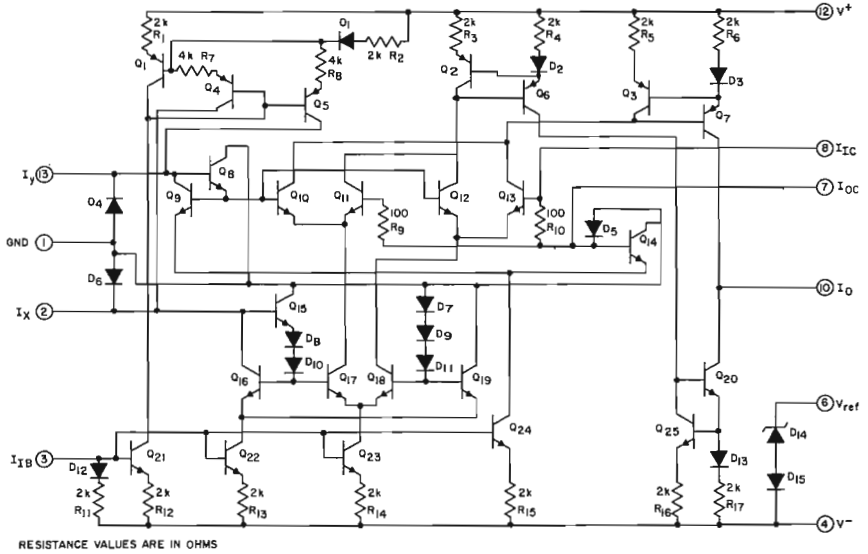


Fig.2—Schematic diagram of the CA3091D.

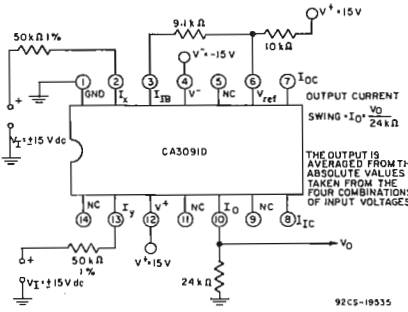


Fig.3—Test circuit for measurement of output current swing capability.

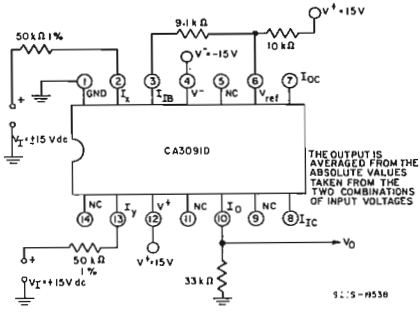


Fig.4—Test circuit for measurement of output voltage swing capability.

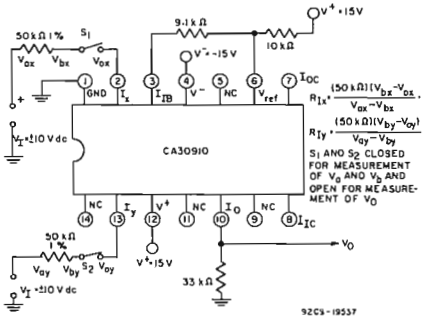


Fig.5—Test circuit for measurement of input resistance.

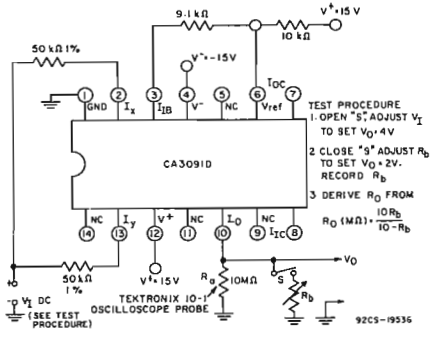


Fig.6—Test circuit for measurement of output resistance.

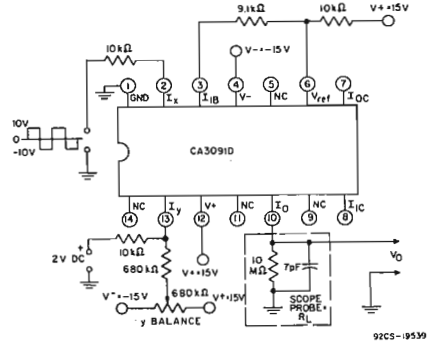


Fig.7—Test circuit for measurement of maximum slew rate.

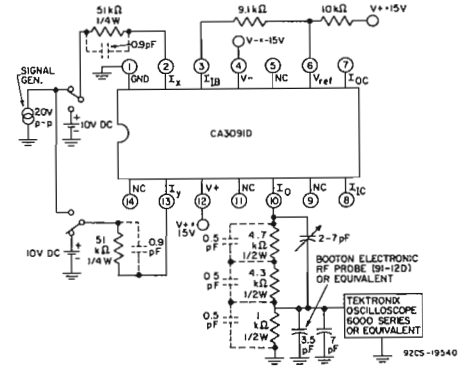


Fig.8—Test circuit for measurement of frequency response.

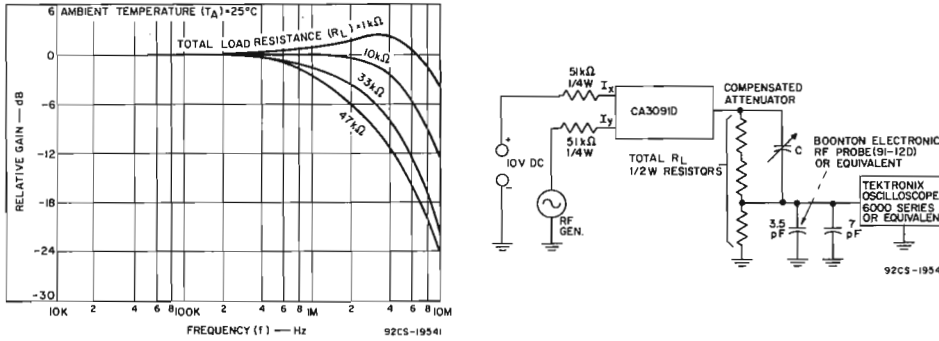


Fig.9- y–input frequency response characteristic curve with associated test circuit.

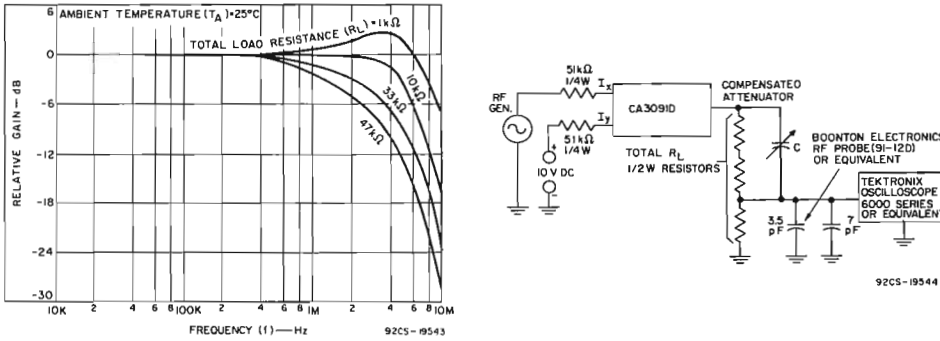


Fig.10- x–input frequency response characteristic curve with associated test circuit.

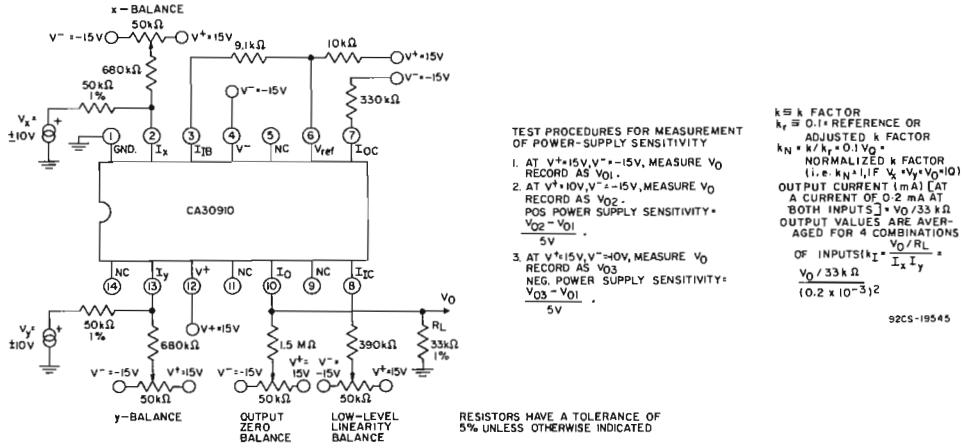
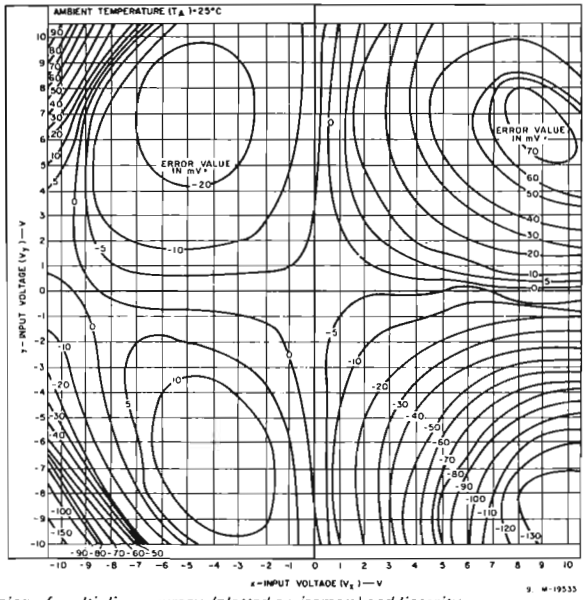


Fig.11–Test circuit for measurement of current gain and power-supply sensitivity.



Note: See "Contour Map" in "Symbols, Terms and Definitions" Section.

Fig.12—Contour mapping of multiplier accuracy (plotted on isomers) and linearity.

SYMBOLS, TERMS AND DEFINITIONS

Output Offset Current
The multiplier output current produced when both of the multiplier input signals are in the zero state.

Output Zero
Sets the output at the zero level when the x and y inputs are in the zero state. (It is implied that all other zeroing adjustments have been effected.)

R_I
Input Resistance — Converts the input voltage to an input current.

R_L
Output (Load) Resistance — Converts the output current to a voltage.

R_O
Output Resistance — See V_O and I_O for the equations associated with these properties.

Regulator Diode
A temperature compensated Zener diode, included in the multiplier circuit, to provide a stable I_{IB}.

Scale Factor or k factor (k)
Represents the basic gain of the multiplier as expressed in the equation $V_O = kV_xV_y$

The equation indicates the ideal transfer function for the multiplier. The normalized k factor is expressed by $k_N = k/k_{ref}$ where k_{ref} is the ideal or reference k factor. The ideal factor, k_{ref} is the value at which the k factor is set when the k-factor adjust control is trimmed. Optimum operation of the CA3091D is achieved when the k-factor is 0.1.

V_{IM}
The maximum ac sine-wave voltage to be applied to the multiplier; a 20-volt p-p sine wave is the nominal maximum swing voltage recommended for use with 50-kilohm input resistors.

V_{MID}
An ac or dc voltage that approximately satisfies the equation

$$V_{MID} = V_{IM}/\sqrt{2}.$$

V_O
The output product voltage derived from the expression

$$(kV_xV_y = V_o)$$

V_{ref}.
Temperature compensated zener connected to the −15 volt supply to provide a reference voltage as an aid in setting up a stable I_{IB}.

V_x, V_y
The input voltages to be multiplied.

x-Balance Circuit
Sets the output to the zero level when the x-input is in the zero state.

y-Balance Circuit
Sets the output to the zero level when the y-input is in the zero state.

SYMBOLS, TERMS AND DEFINITIONS — continued

Accuracy
Accuracy defines the degree of error encountered in the operation of the multiplier. It is portrayed on a contour map by isomers (contour lines). Isomers with the highest values indicate "less-accurate" operation of the multiplier. (See illustrative Contour Map in Fig. 12.)

Contour Map
The contour map, shown in Fig. 12, is a graphical portrayal of the multiplier errors in the x, y input plane. Each contour line, termed "isomer", connects those points whose error values (in millivolts) are equal in magnitude. For example, a −20 mV contour line with points at V_X = 5V and V_Y = −3V indicates that the output voltage is 20 mV less than the theoretical output product (kV_XV_Y). This error voltage, presented in percent of full-scale input (±10 V), defines the "accuracy" of the device. Thus, a 20-mV error voltage represents an "accuracy" of 0.2% as derived from the equation:

$$\text{Accuracy} = 20\ \text{mV}/10 \times 100\% = 0.2\%.$$

A contour map provides a true indication of multiplier performance in each of the four quadrants. Each CA3091D is comprehensively tested and must provide the specified accuracy in the four quadrants.

Current Converter
This portion of the IC combines the multiplier's differential-amplifier output currents and converts them to a single-ended output current.

Current Sources
These circuits provide the biasing currents for the various circuits in the IC. The I_{IB} terminal provides the control current for the current-source circuit.

Feedthrough
Feedthrough occurs when an output signal is produced even though one of the input signals is zero. Consequently, feedthrough signal characteristics constitute a source of error in the operation of a multiplier. In the CA3091D, for example, the feedthrough signal output is specified to be less than 20 mV p-p when either terminal is set at 20 V p-p and the other terminal is set to zero.

I_{IB}
Circuit biasing control current.

I_{IC}
See I_{OC}.

I_O
Output product current ($k_I I_X I_Y = I_O$), where $k_I = kR_I^2 / R_L$

I_{OC}, I_{IC}
Compensatory input and output currents required to correct unlinearity along the x axis. (Optional for low-level signal use.)

I_X, I_Y
Input currents to be multiplied.

k
Voltage Scale Factor (determines the gain of the multiplier).

k_I
Current Scale Factor (k_I) = $(R_I^2 / R_L)k$.

k adjust
Scale-Factor Adjustment.

Linearity
"Linearity" indicates the degree of multiplier error (i.e. deviation from "straight-line" characteristics) along each of the four boundaries of the input x, y field. These boundaries are formed when one input is held at one of the two maximum values (10 volts or −10 volts) and the other input is swept through the voltage range. (See Contour Map for additional information.)

Linearity Adjust
An external circuit to provide vernier adjustment for optimum linearity. This control should be adjusted before adjusting the y-balance control.

Linearity Balance Circuit (Low-Level)
This circuit makes the multiplier's transfer function linear for low-level x-input signals.

Linearity Compensator
Internal circuitry that converts input current into a non-linear voltage, a requisite for producing a linear output in the differential amplifiers of the multiplier circuit.

Multiplier Circuitry
Provides the product of the two input voltages.

Multiplier Transfer Function
This function mathematically describes the interaction of the two inputs and the resulting output signal. The basic transfer function for a multiplier is

$$k(V_X + V_{Xe})(V_Y + V_{Ye}) = V_O + V_{Oe}$$

where: k = k factor and represents the basic gain of the multiplier

V_X, V_Y = the external inputs to be multiplied

V_O = the desired value of the product output signal

V_{Xe}, V_{Ye} = the "effective" errors that occur at the inputs of the multiplier and cause an output signal when either input is in a zero state.

V_{Oe} = the error voltage that develops at the output of the multiplier

DC correction factors are added to the multiplier inputs and output to compensate for the errors and offset variations. A complex linearity error term appears in the transfer function; however, this term is not included in the above equation for the purpose of clarity.

OPERATING CONSIDERATIONS

Operation of a Multiplier

A multiplier is, essentially, a gain-controlled amplifier (See Fig. 13) that multiplies the input signal (V_x) with the external gain controlling signal (V_y) to produce the resultant output (V_o). The gain is externally adjustable by a coefficient (k). Stated simply, a multiplier produces an output voltage that is the linear product of two input voltages.

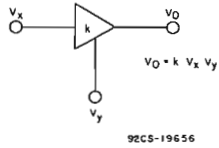
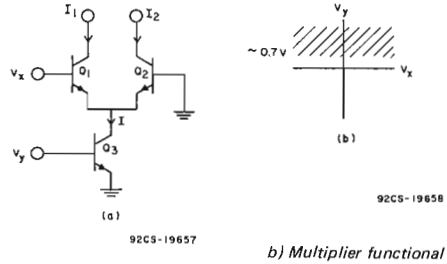


Fig.13—Gain-controlled amplifier.

The basic multiplier, shown in Fig. 14a, is a two-quadrant multiplier. The input signal (V_x) may have either a positive or negative polarity whereas, the external gain-controlling signal (V_y) must be positive and greater than the base-to-emitter voltage (Fig. 14b). The output current ($I_1 - I_2$) of the differential amplifier, comprised of transistors Q1 and Q2, is related to both the input signal (V_x) and the current source (I). Since the current source (I) is related to the gain controlling signal (V_y) the output current ($I_1 - I_2$), therefore, is related to both V_x and V_y.



a) Basic circuit.

b) Multiplier functional only in shaded region.

Fig.14—Two-quadrant multiplier.

This relationship is essentially non-linear; thus an appropriate linearization circuit must be provided in the input stage to achieve the following linear relationship:

$$I_1 - I_2 = k' V_x V_y \qquad \text{(Eq. 1)}$$

where k' is a constant

Figure 15 shows a typical arrangement of three differential amplifiers to form a four-quadrant multiplier. This arrangement incorporates the operating principles of the two-quadrant multiplier, but, in addition, it permits both of the input signals (V_x and V_y) to have positive or negative polarities (or zero). When either input is zero, the output current ($I_1 - I_2$) must, theoretically, be zero as is shown by the following:

1. Assume $V_x = 0$,
   then $i_1 = i_2$ and $i_3 = i_4$
   therefore $i_1 + i_4 = i_2 + i_3$.
   Since $I_1 = i_1 + i_4$ and $I_2 = i_2 + i_3$,
   then $I_1 = I_2$.
   This equality is independent of V_y
2. Now assume $V_y = 0$,
   then $i_5 = i_6$.
   Sine $i_5 = i_1 + i_2$ and $i_6 = i_3 + i_4$,
   then $i_1 + i_2 = i_3 + i_4$.
   Since $i_1 = i_3$ and $i_2 = i_4$
   then $i_1 + i_4 = i_3 + i_2$.
   Therefore $I_1 = I_2$.
   This equality is independent of V_x.

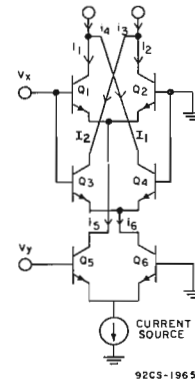


Fig.15—Basic four-quadrant multiplier.

The multiplying operation discussed in the previous section applies when neither V_x nor V_y is zero. The output current ($I_1 - I_2$) then satisfies Equation 1,

$$I_1 - I_2 = k' V_x V_y.$$

The multiplying action of the four-quadrant multiplier is dependent on current unbalance in the three differential amplifiers. Ideally, the multiplying operation should not occur if either V_X or V_Y is O. However, in practical applications slight current unbalances do exist. It is necessary, therefore, to null out such unbalances with external potentiometers prior to operation.

TYPICAL OPERATING CONSIDERATIONS

The RCA-CA3091D, shown in Fig. 2, is a four-quadrant multiplier that incorporates the basic multiplier principle, previously discussed in "Operation of a Multiplier". Because the design of this multiplier is based on the multiplication of two input currents to produce an output current it is necessary to convert the input voltages to input currents and the output current to an output voltage by inserting resistors at both input and output terminals. Fig. 1 shows the four-quadrant multiplier with its peripheral circuitry for nulling current unbalances.

The Bias Current (I_{IB}) at Term. 3 sets the operating current level for the entire multiplier circuit by means of a current-source circuit. Therefore, it is essential that this bias current level remain constant under all operating conditions. To maintain this steady state, a temperature compensated zener diode is provided on the chip and connected to the Reference Voltage (Term.6).

Linearity of the differential amplifier transconductance function is accomplished by linearity compensators as shown in Fig. 1. To correct low-level signal unbalances that may occur between Differential Amplifiers A and B, an external potentiometer is connected to Terminals 7 and 8 (See Fig. 1). The Current Converter circuit, which consists of a set of current mirrors, supplies the output current ($I_1 - I_2$). It is important that circuit unbalances be corrected prior to operation. Table I describes the alignment procedures for correcting these unbalances.

A multifunctional circuit board (Figs. 16 and 17) is available for performing the four basic applications, such as, multiplying, dividing, squaring and taking the square root.

When the CA3091D is used as a multiplier (Fig. 18) or as a squarer (Fig. 18) only the basic pheripheral circuitry on the multifunctional circuit board is utilized and the general-purpose operational amplifier (CA3741T) is disabled from operation. Follow the ac alignment procedures for these two applications before operating the circuit.

When the CA3091D is used as a divider (Fig. 20), the operational amplifier is required in order to provide the proper negative feedback. The limitations for operation as a divider are that $0 \leq V_Y \leq 10V$ and $-10V \leq V_Z \leq 10V$. Note, the range of V_Y is limited to the positive polarity; if V_Y was permitted to go negative, the feedback loop would go positive and, thereby, create an unstable operating condition.

Alignment of the divider (Fig. 19) differs from multiplier and squarer alignment because of the additional variances introduced by the operational amplifier. A coupling capacitor is

Table I

AC Alignment Procedures For CA3091D, Four-Quadrant Multiplier

(Refer to Fig. 16, for circuit pertaining to following alignment procedures.)

Step No.	Voltage Setting		Control Adjust	Test Equipment Used	Measure	Notes
	V_x	V_y				
1	–	–	–	–	–	Set all potentiometers to center of range.
2	O	V_{IM}	x Balance	AC VM	V_O	Adjust for a minimum reading.
3	O	V_{IM}	Linearity	AC VM	V_O	Adjust for a minimum reading.
4	–	–	–	–	–	Repeat Staps 1 and 2 until no further improvement is noted.
5	V_{IM}	O	y Balance	AC VM	V_O	Adjust for a minimum reading.
6	O	O	Zero Output	DC VM	V_O	Adjust for zero output.
7	V_{MID}	V_{MID}	R_k	AC/DC VM	V_O	Adjust for $V_{MID}^2/10$ at the output.
8	–	–	–	–	–	Check multiplier for alignment in all four quadrants.

V_{IM} – Is the maximum AC swing of the sine wave that will be applied to the multiplier. A 20-volt p-p value is the nominal maximum swing of the AC sine wave with input resistors of 50 kilohms.

V_{MID} – An AC or DC voltage that approximately satisfies the equation $V_{MID} = V_{IM}/\sqrt{2}$. For example, if a 50-kilohm rasistor is used with a 7-volt input, then R_k should be adjusted for a 4.9-volt output.

provided at the output of the divider alignment circuit in order to separate the ac signal from the dc signal and, thus, avoid interaction between the calibrating potentiometers.

The alignment procedure for the square-rooter function (Fig. 21) is identical to the alignment procedure for the divider function. The input voltage range is limited to $0 < V_I \leqslant 10V$. This limitation is necessary in order to prevent the output voltage (V_O) from latching to the negative output saturation voltage of the operational amplifier. Table II describes the divider alignment procedure.

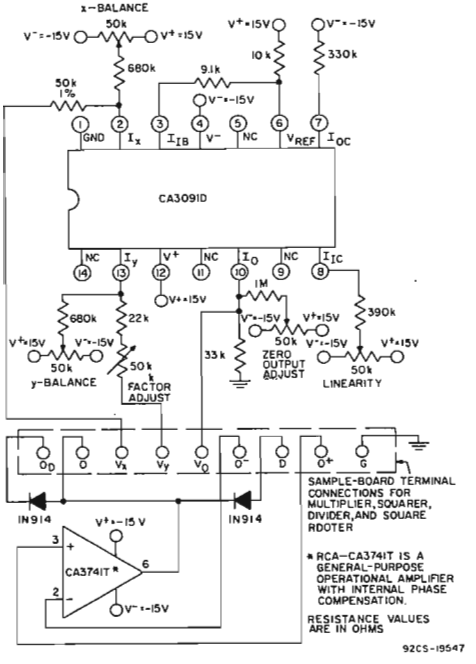
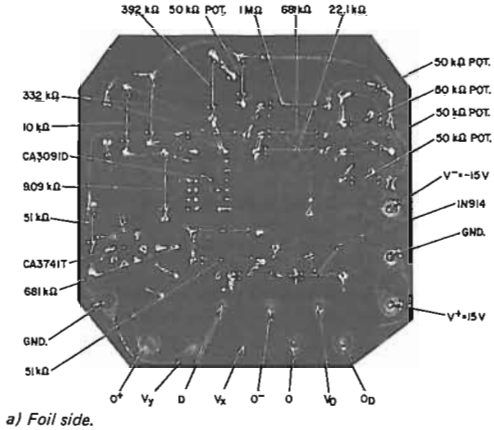
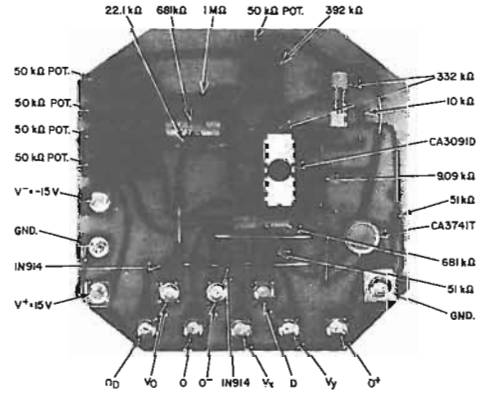


Fig.16—Typical multifunction circuit arrangement utilizing the CA3091D and CA3741T.



a) Foil side.

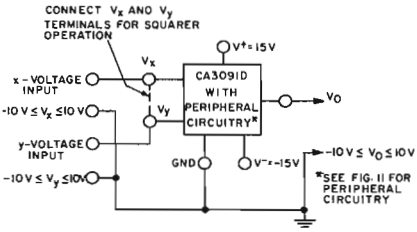


b) Component side.

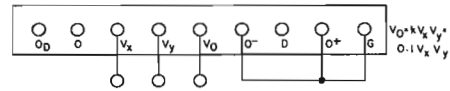
Fig.17—Photographs of a printed-circuit board for multifunction applications (multiplier, squarer, divider, square rooter) utilizing the CA3091D and CA3741T.

Table II — Divider Alignment Procedure

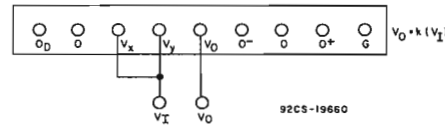
Step No.	Set V_z V	Set V_y V	Measure	Output Coupling	Test Equipment Used	Adjust	Notes
1	—	—	—	—	—	—	Set all potentiometers to center of range.
2	0	V_S	V_O	ac	ac – VM	O_{zero}	Adjust for minimum reading.
3	0	10V dc	V_O	dc	dc – VM	$x_{balance}$	Adjust for OV dc output.
4	V_S	V_S	V_O	ac	ac – VM	$y_{balance}$	Adjust for minimum reading.
5	5V dc	5V dc	V_O	dc	dc – VM	k_{adjust}	Adjust for 10 V dc output.



a) Circuit arrangement for multiplier or squarer operation.



b) Terminal connections for multiplying operation.



c) Terminal connections for squarer operation.

Fig.18—Multifunction circuit-board arrangement with terminal connections for multiplier and squarer operation.

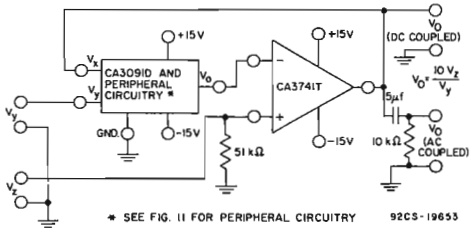


Fig.19—(a) Divider alignment circuit.

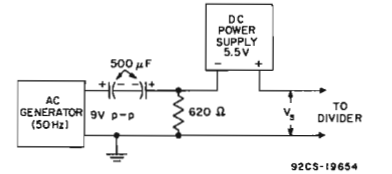
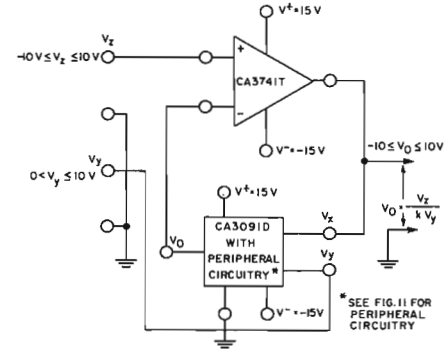
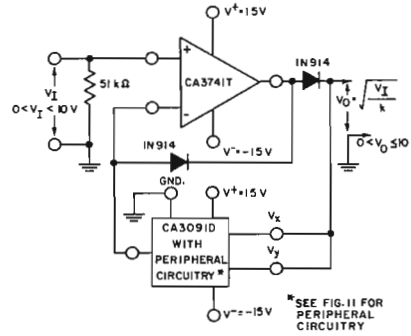


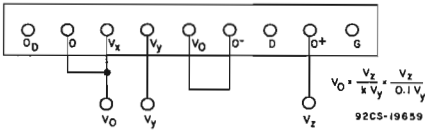
Fig.19—(b) Circuit to provide offset ac signal for use in divider alignment procedure.



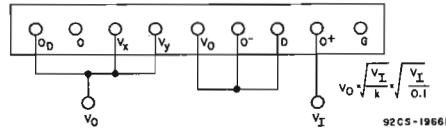
a) Circuit arrangement for divider operation.



a) Circuit arrangement for square-rooter operation.



b) Terminal connections for divider operation.



b) Terminal connections for square-rooter operation.

Fig.20—Multifunction circuit-board arrangement with terminal connections for divider operation.

Fig.21—Multifunction circuit-board arrangement with terminal connections for square-rooter operation.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3093E

16-Lead Dual-In-Line Plastic Package '41622

General-Purpose High-Current N-P-N Transistor-Zener Diode-Diode Array

Applications

- Signal processing and switching systems operating from DC to VHF
- Lamp and relay driver
- Differential amplifier
- Temperature-compensated amplifier
- Thyristor firing
- Temperature-compensated shunt regulator
- Temperature-compensated series regulator
- Level shifting
- Voltage-level clamping
- Current regulator
- Voltage clamping
- Simple off-line regulated supply
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for applications in addition to those given on pages 5 & 6 of this bulletin.

RCA CA3093E* is a versatile array of three high-current (to 100mA) NPN transistors, two 10%-tolerance Zener diodes and one conventional diode, all on a common monolithic substrate. Two of the transistors (Q_1 and Q_2) are matched at 1 mA for applications in which offset parameters are of special importance. The combination of positive Zener voltage temperature coefficients and negative forward base-emitter voltage temperature coefficients provides a unique temperature compensation capability.

Independent connections for each transistor and diode plus a separate terminal for the substrate permit maximum flexibility in circuit design.

*Formerly developmental type TA6119

#Z_1, Z_2 and D1 are transistors internally connected as shown below.

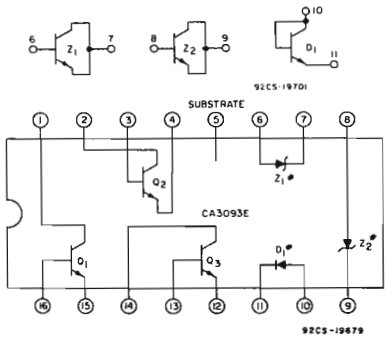


Fig. 1 — Functional diagram of the CA3093E (bottom view)

Features:

- 6 independent devices plus separate substrate connection
- Compensating temperature coefficients — V_{BE} and V_{D1} vs. V_Z

Transistors

- High I_C (100mA max)
- Matched pair (Q1 & Q_2)
  V_{IO} = ± 5mV max
  I_{IO} = 2.5 μA max
  } at I_C = 1mA
  $\Delta V_{IO}/\Delta T$ = 5 μV/°C typ
- h_{FE} = 40 min @ I_C = 10mA or 50mA
- Low V_{CEsat} . . . 0.7V max @ 50mA

Zener Diodes

- Two 1/4W Zeners
- V_Z = 7V ± 10%
- z_Z = 15Ω typ

Diode

- Close forward voltage match to V_{BE}'s of Q_1 and Q_2
- V_{PIV} = 5.5V min.

MAXIMUM RATINGS, *Absolute-Maximum Values at* T_A = 25°C

Power Dissipation:

Any one transistor	500	mW
Any one Zener Diode	250	mW
Total package	750	mW
Above 25°C ..... Derate linearly	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−55 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C

The following maximum ratings apply for each transistor

Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})*	20	V
Emitter-to-Base Voltage (V_{EBO})	5.5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	35	mA

The following maximum ratings apply for each Zener Diode or Diode

Zener Diode dc Current (I_Z)	35	mA
Zener Diode-to-Substrate Voltage (V_{ZIO})*	20	V
Diode (D1) Forward Current (I_{DF})	50	mA
Diode (D1) Reverse Voltage (V_{DR})	5.5	V
Diode (D1)-to-Substrate Voltage (V_{DIO})*	20	V

*The collector of each transistor, the cathode of each Zener diode, and the anode of the diode are isolated from the substrate by an internal diode. The substrate must be connected to a voltage which is more negative than any of these isolated terminals in order to maintain isolation between devices and provide normal transistor action. To avoid undesired coupling between devices, the substrate terminal (5) should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	5.5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	1	μA
DC Forward Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	40	76	–	
		V_{CE} = 3V, I_C = 50mA	40	75	–	
Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	–	0.40	0.70	V
Forward Base-to-Emitter Temp. Coefficient	$\Delta V_{BE}/\Delta T$	I_E = 10mA	–	-1.9	–	mV/°C
For Transistors Q1 and Q2 (As a Differential Amplifier):						
Absolute Input Offset Voltage	$\lvert V_{IO} \rvert$	V_{CE} = 3V, I_C = 1mA	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO} \rvert$		–	0.7	2.5	μA
Temp. Coefficient of Offset Voltage	$\lvert \Delta V_{IO}/\Delta T \rvert$	–	–	5	–	μV/°C
For Each Zener Diode						
Zener Voltage	V_Z	I_Z = 10mA	6.3	7	7.7	V
Zener Impedance	z_Z	I_Z = 10mA, f = 1 kHz	–	15	25	Ω
Zener Reverse Current	I_{ZR}	V_Z = +5V	–	–	1	μA
Zener Voltage Temp. Coefficient	$\Delta V_Z/\Delta T$	I_Z = 10mA	– i.e.	+3.6 +.05	–	mV/°C %/°C
Zener-to-Substrate Breakdown Voltage	$V_{(BR)ZIO}$	I_Z = 100μA (Terminals 7 & 9)	20	60	–	V
Dissipation		Refer to Example In Application "a"	–	–	250	mW
For Diode (D1)						
Diode Forward Voltage	V_{DF}	I_C = 10mA, V_{CE} = 3V	0.65	0.74	0.85	V
Diode Forward Current	I_{DF}		–	–	50	mA
Diode Reverse-Breakdown Voltage	$V_{(BR)DR}$	I_{DR} = 500μA	5.5	6.9	–	V
Diode-to-Substrate Breakdown Voltage	$V_{(BR)DIO}$	I_{Diode} = 100μA (Terminal 10)	20	60	–	V
Diode Forward-Voltage Temp. Coefficient	$\Delta V_{DF}/\Delta T$	I_{DF} = 5mA	–	-1.9	–	mV/°C

TYPICAL STATIC CHARACTERISTICS

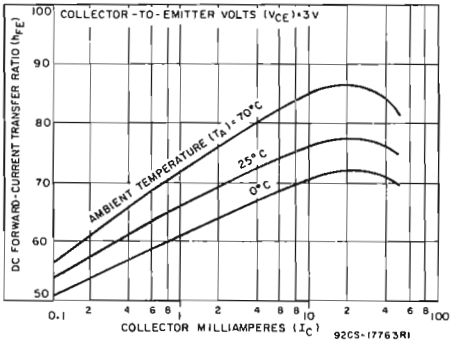


Fig. 2 – h_{FE} vs I_C

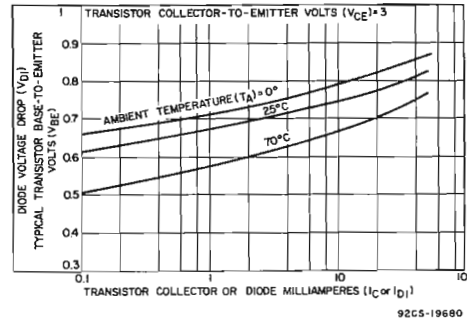


Fig. 3 – V_{BE} vs I_C and V_{D1} vs I_{D1}

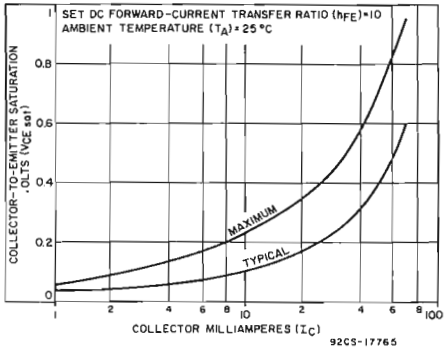


Fig. 4 – V_{CEsat} vs I_C at 25°C

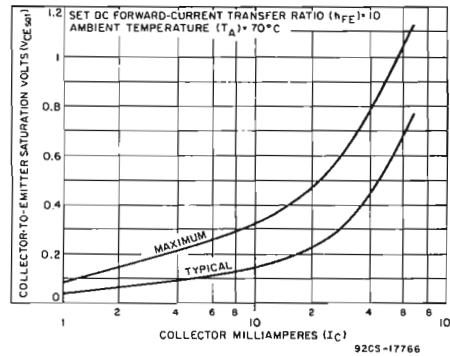


Fig. 5 – V_{CEsat} vs I_C at 70°C

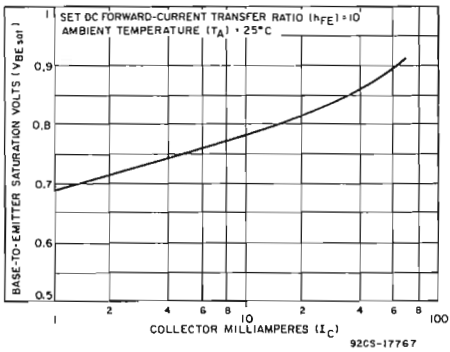


Fig. 6 – V_{BEsat} vs I_C

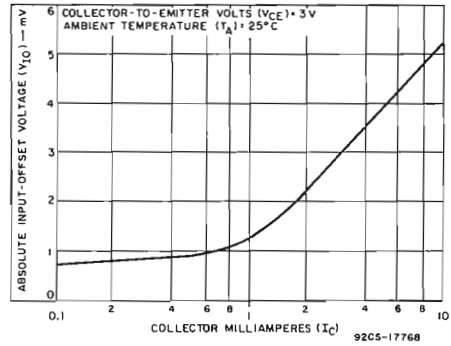


Fig. 7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

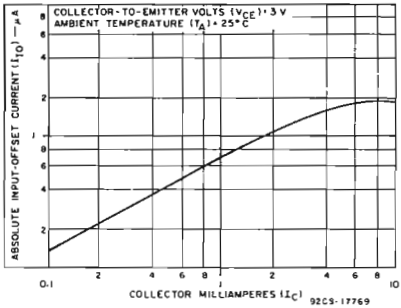


Fig. 8 — I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

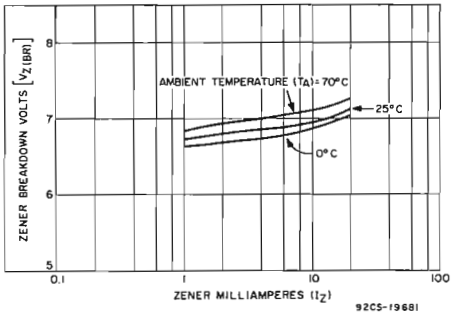


Fig. 9 — Typical Zener breakdown voltage vs current

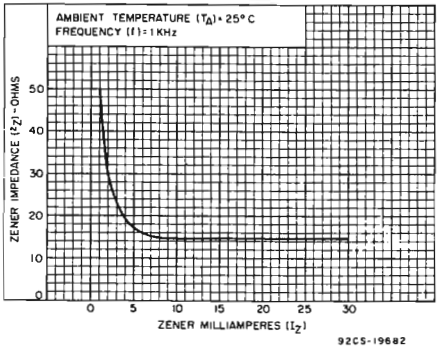
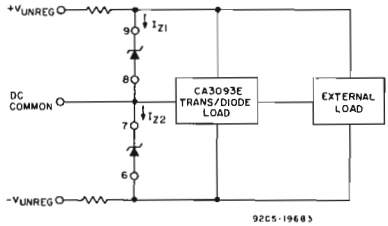


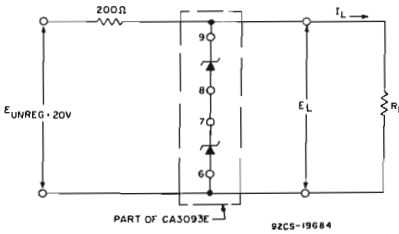
Fig. 10 — Typical Zener impedance vs current

TYPICAL APPLICATIONS

a) ±7V Regulator supplying CA3093E Transistors plus an external load.



b) 14V Regulator for Q1, Q2, Q3



Sample Computation for Determining Permissible Zener Dissipation at +25°C.

CA3093E Ratings at T_A = +25°C
Total Diss. Max = 750 mW (Derate @ 6.67 mW/°C above 25°C)
Each Zener Diss. Max = 250 mW
Max. Zener Current = 35 mA

Assume CA3093E Transistor/Diode Load Dissipation = 350 mW then max. total Zener Diss. ($P_{Z1} + P_{Z2}$) = 750 - 350 = 400 mW

$$(I_{Z1} + I_{Z2}) \text{ max} = \frac{400 \text{ mW}}{7V} = 57 \text{ mA}$$

(Note: Max. current rating on each Zener is 35 mA)

Typical Load Regulation for I_L = 0 to 25 mA

$\Delta E_L/E_L \times 100 \approx -6\%$ (no load to full load)

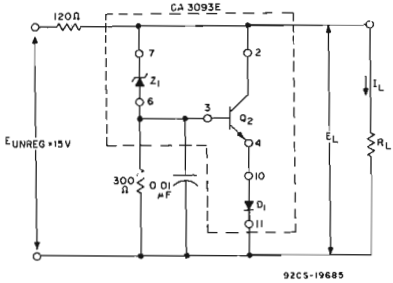
Typical Line Regulation

$$\frac{(\Delta E_L/E_L) \times 100}{\Delta E \text{ unreg.}} \approx \pm 0.9\%/V$$

Typical Temperature Characteristic

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = +0.05\%/°C$$

c) 8.6V Temp.-Compensated Shunt Regulator



Typical Temperature Characteristic @ R_L = 330Ω

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = \pm\ 0.007\%/°C$$

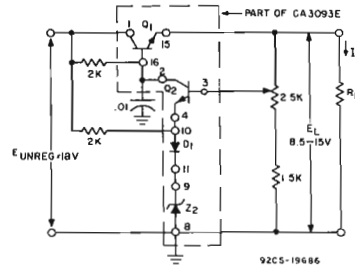
Typical Load Regulation I_L = 0 to 40 mA

$(\Delta E_L/E_L) \times 100 = -3\%$ (no load to full load)

Typical Line Regulation at R_L = 330Ω

$$\frac{\Delta E_L/E_L}{\Delta E \text{ unreg.}} \times 100 = \pm\ 0.55\%/V$$

d) Temp.-Compensated Series Voltage Regulator



Typical Temperature Characteristic @ E_L = 12V

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = \pm\ 0.009\%/°C$$

Typical Load Regulation @ E_L = 12V

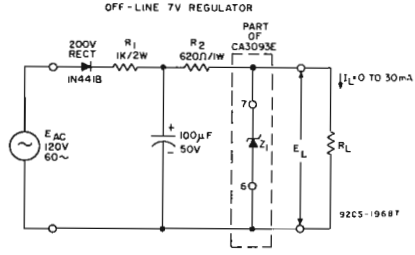
I_L = 0 to 40 mA

$$\frac{\Delta E_L}{E_L} \times 100 = \pm\ 0.4\% \text{ (no load to full load)}$$

Typical Line Regulation @ E_L = 12V

$$\frac{(\Delta E_L/E_L) \times 100}{\Delta E \text{ unreg.}} = \pm\ 0.45\%/V$$

e) Off-Line 7V Regulator



Typical E_L Ripple Voltage = 70 mV_{p-p}

Typical Load Regulation = $\frac{\Delta E_L}{E_L} \times 100 = -8.5\%$ (no load to full load)

I_L = 0 to 30 mA

Typical Line Regulation = $\frac{(\Delta E_L/E_L) \times 100}{\Delta E_{AC}} = \pm\ .075\%/V$

RCA
Solid State
Division

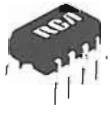
Linear Integrated Circuits

Monolithic Silicon

CA3094, CA3094A, CA3094B Types

S-Suffix Types
8-LEAD TO-5
with Dual-In-Line
Formed Leads
"DIL-CAN"
H-1787

T-Suffix Types
8-LEAD TO-5
H-1528



CA3094E
8-LEAD DUAL-
IN-LINE PLASTIC
PACKAGE
"MINI-DIP" H-1817

Programmable Power Switch/ Amplifier

CA3094: For Operation Up to 24 Volts
CA3094A: For Operation Up to 36 Volts
CA3094B: For Operation Up to 44 Volts

For Control & General-Purpose Applications

Features:

- Designed for *single* or dual power supply
- Programmable: strobing, gating, squelching, AGC capabilities
- Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)
- High-power, single-ended class A amplifier will deliver power output of 0.6 watt (1.6 W device dissipation)
- Total harmonic distortion (THD) @ 0.6 W in class A operation – 1.4% typ.
- High current-handling capability – 100 mA (avg.), 300 mA (peak)
- Sensitivity controlled by varying bias current
- Output: "sink" or "drive" capability

APPLICATIONS:

- Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor
- Over-current, over-voltage, over-temperature protectors
- Dual-tracking power supply with RCA-CA3085
- Wide-frequency-range oscillator ■ Analog timer
- Level detector ■ Alarm systems ■ Voltage follower
- Ramp-voltage generator ■ High-power comparator
- Ground-fault interrupter (GFI) circuits

The CA3094 is a differential-input power-control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional-control output signal up to 100 mA. This signal is sufficient to directly drive high-current thyristors, relays, dc loads, or power transistors. The CA3094 has the generic characteristics of the RCA-CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100 mA.

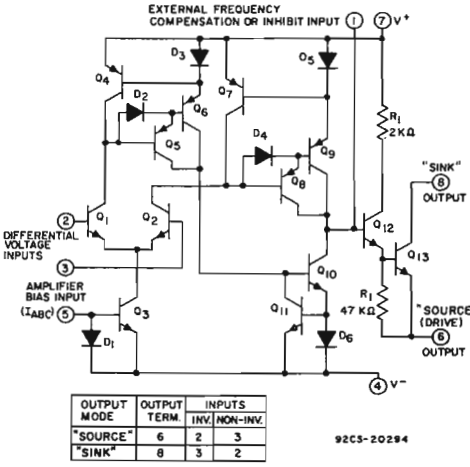
The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100 μA, a one-millivolt change at the input will change the output from 0 to 100 mA (typical).

The CA3094 is intended for operation up to 24 volts and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24 volts is a primary design requirement (see Figs.27,28 and 29 in Applications Section). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

Application Note ICAN-6668 describes the rudiments of Operational Transconductance Amplifiers (OTA's).

These types are available in 8-lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8-lead dual-in-line plastic package "MINI-DIP" ("E" suffix), and in chip form ("H" suffix).

APPLICATION NOTE ICAN-6048 GIVES DETAILED APPLICATION INFORMATION FOR THE CA3094, CA3094A, AND CA3094B.



OUTPUT MODE	OUTPUT TERM.	INPUTS	
		INV.	NON-INV.
"SOURCE"	6	2	3
"SINK"	8	3	2

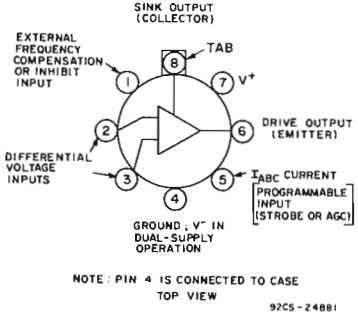
92CS-20294

Fig. 1—Schematic diagram of CA3094.

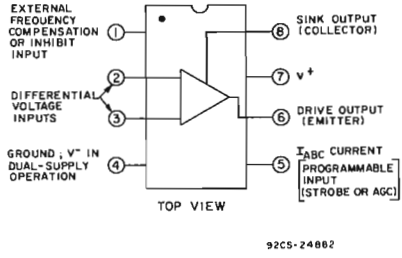
MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3094	CA3094A	CA3094B	
DC SUPPLY VOLTAGE:				
Dual Supply	± 12 V	± 18 V	± 22 V	V
Single Supply	24 V	36 V	44 V	V
DC DIFFERENTIAL INPUT VOLTAGE (Terminals 2 and 3)	± 5*			V
DC COMMON-MODE INPUT VOLTAGE	Term. 4 ⩽ Term. 2 & 3 ⩽ Term. 7			
PEAK INPUT SIGNAL CURRENT (Terminals 2 and 3)	± 1			mA
PEAK AMPLIFIER BIAS CURRENT (Terminal 5)	2			mA
OUTPUT CURRENT:				
Peak	300			mA
Average	100			mA
DEVICE DISSIPATION:				
Up to T_A = 55°C:				
Without heat sink	630			mW
With heat sink	1.6			W
Above T_A = 55°C:				
Without heat sink derate linearly	6.67			mW/°C
With heat sink derate linearly	16.7			mW/°C
THERMAL RESISTANCE (Junction to Air)	140			°C/W
AMBIENT TEMPERATURE RANGE:				
Operating	−55 to +125			°C
Storage	−65 to +150			°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 300			°C

*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.



TO-5 Style Package



Plastic Package

FUNCTIONAL DIAGRAMS

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
		Test Circuit Fig. No.	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Char. Curves Fig. No.	Min.	Typ.	Max.	
INPUT PARAMETERS								
Input Offset Voltage	V_{IO}	17	T_A = 25°C	2	–	0.4	5	mV
			T_A = 0 to 70°C		–	–	7	mV
Input-Offset-Voltage Change	$\lvert\Delta V_{IO}\rvert$		Change in V_{IO} Between I_{ABC} = 100 μA and I_{ABC} = 5 μA		–	1	8	mV
Input Offset Current	I_{IO}	18	T_A = 25°C	3	–	0.02	0.2	μA
			T_A = 0 to 70°C		–	–	0.3	μA
Input Bias Current	I_I	19	T_A = 25°C	4	–	0.2	0.50	μA
			T_A = 0 to 70°C		–	–	0.70	μA
Device Dissipation	P_D	18	I_{out} = 0	5, 6	8	10	12	mW
Common-Mode Rejection Ratio	C_{MRR}	20			70	110	–	dB
Common-Mode Input–Voltage Range	V_{ICR}	20	V^+ = 30 V $\frac{\text{High}}{\text{Low}}$	7	27	28.8	–	V
					1.0	0.5	–	V
			V^+ = 15 V, V^- = 15 V	7	+12	+13.8	–	V
					–14	–14.5	–	V
Unity Gain-Bandwidth			I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA		–	30	–	MHz
Open-Loop Bandwidth At –3 dB Point	BW_{OL}		I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA	12	–	4	–	kHz
Total Harmonic Distortion (Class A Operation)	THD		P_D = 220 mW		–	0.4	–	%
			P_D = 600 mW		–	1.4	–	
Amplifier Bias Voltage (Terminal (No.5 to Terminal No.4)	V_{ABC}				–	0.68	–	V
Input Offset Voltage Temperature Coefficient	$\Delta V_{IO}/\Delta T$				–	4	–	μV/°C
Power-Supply Rejection	$\Delta V_{IO}/\Delta V$	17			–	15	150	μV/V
1/F Noise Voltage	E_N	21	f = 10 Hz, I_{ABC} = 50 μA	8	–	18	–	$\eta V/\sqrt{Hz}$
1/F Noise Current	I_N	21	f = 10 Hz, I_{ABC} = 50 μA	9	–	1.8	–	$pA/\sqrt{Hz}$
Differential Input Resistance	R_I		I_{ABC} = 20 μA		0.50	1	–	MΩ
Differential Input Capacitance	C_I		f = 1 MHz, V^+ = 30 V		–	2.6	–	pF

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
		Test Circuit Fig. No.	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Char. Curves Fig. No.	Min.	Typ.	Max.	
OUTPUT PARAMETERS (Differential Input Voltage = 1V)								
Peak Output Voltage: (Terminal No. 6)			V^+ = 30 V					
With Q13 "ON"	V^+_{OM}		R_L = 2 kΩ to ground		26	27	–	V
With Q13 "OFF"	V^-_{OM}				–	0.01	0.05	V
Peak Output Voltage: (Terminal No. 6)			V^+ = +15 V, V^- = -15 V				0.5	
Positive	V^+_{OM}		R_L = 2 kΩ to −15 V		+11	+12	–	V
Negative	V^-_{OM}				–	−14.99	−14.95	V
Peak Output Voltage: (Terminal No. 8)			V^+ = 30 V					
With Q13 "ON"	V^+_{OM}		R_L = 2 kΩ to 30 V		29.95	29.99	–	V
With Q13 "OFF"	V^-_{OM}				–	0.040	–	V
Peak Output Voltage: (Terminal No. 8)			V^+ = 15 V, V^- = – 15 V					
Positive	V^+_{OM}		R_L = 2 kΩ to + 15 V		+14.95	+14.99	–	V
Negative	V^-_{OM}				–	14.96	–	V
Collector-to-Emitter Saturation Voltage (Terminal No. 8)	$V_{CE(sat)}$		V^+ = 30 V I_C = 50 mA Terminal No.6 grounded	10	–	0.17	0.80	V
Output Leakage Current (Terminal No. 6 to Terminal No. 4)			V^+ = 30 V		–	2	10	μA
Composite Small-Signal Current Transfer Ratio (Beta) (Q_{12} and Q_{13})	h_{fe}		V^+ = 30 V V_{CE} = 5 V I_C = 50 mA	11	16,000	100,000	–	
Output Capacitance: Terminal No. 6	C_O		f = 1 MHz All Remaining Terminals Tied to Terminal No. 4		–	5.5	–	pF
Terminal No. 8					–	17	–	pF
TRANSFER PARAMETERS								
Voltage Gain	A	22	V^+ = 30 V I_{ABC} = 100 μA ΔV_{out} = 20 V R_L = 2 kΩ	12	20,000 86	100,000 100	– –	V/V dB
Forward Transconductance To Terminal No. 1	g_m			13	1650	2200	2750	μmhos
Slew Rate: Open Loop: Positive Slope		23	I_{ABC} = 500 μA R_L = 2 kΩ	14	–	500	–	V/μs
Negative Slope					–	50	–	V/μs
Unity Gain (Non-Inverting, Compensated)		24	I_{ABC} = 500 μA R_L = 2 kΩ	15	–	0.7	–	V/μs

Typical Characteristics Curves

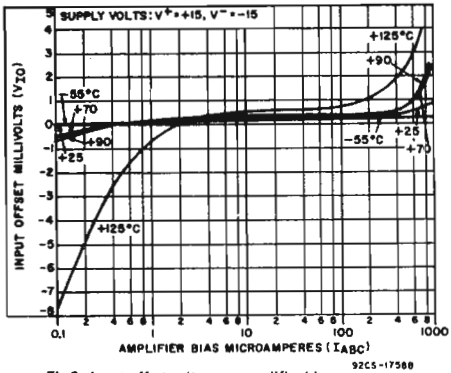


Fig.2—Input offset voltage vs. amplifier bias current (I_{ABC}, terminal No. 5).

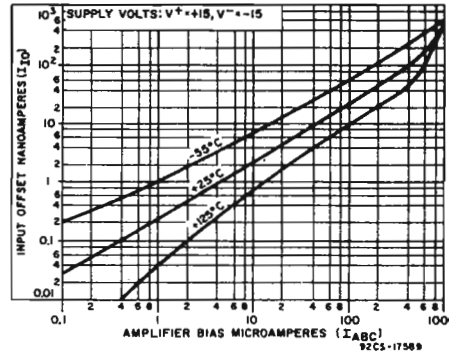


Fig.3—Input offset current vs. amplifier bias current (I_{ABC}, terminal No. 5).

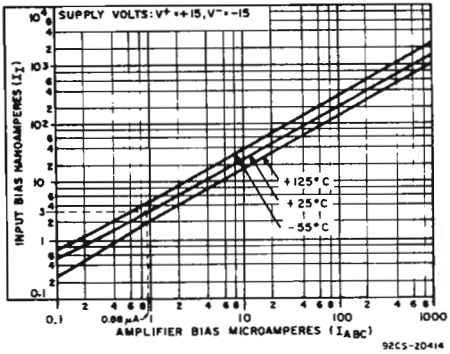


Fig.4—Input bias current vs. amplifier bias current (I_{ABC}, terminal No. 5).

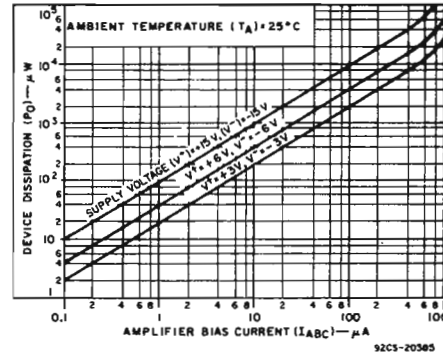


Fig.5—Device dissipation vs. amplifier bias current (I_{ABC}, terminal No. 5).

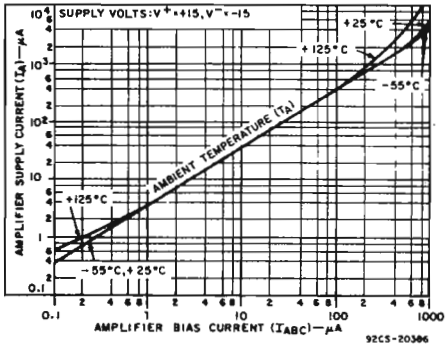


Fig.6—Amplifier supply current vs. amplifier bias current (I_{ABC}, terminal No. 5).

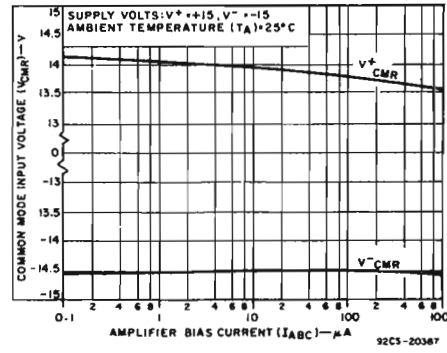


Fig.7—Common mode input voltage vs. amplifier bias current (I_{ABC}, terminal No. 5).

Typical Characteristics Curves

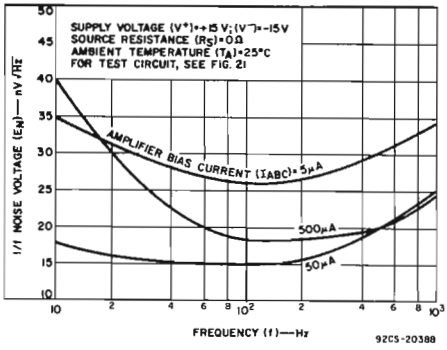


Fig.8—1/F Noise voltage vs. frequency.

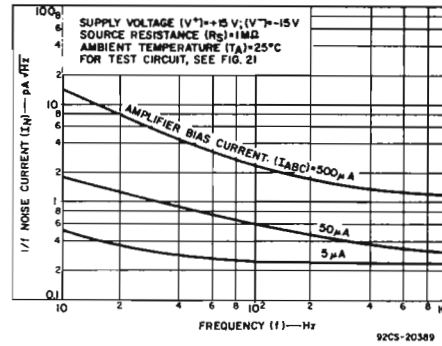


Fig.9—1/F Noise current vs. frequency.

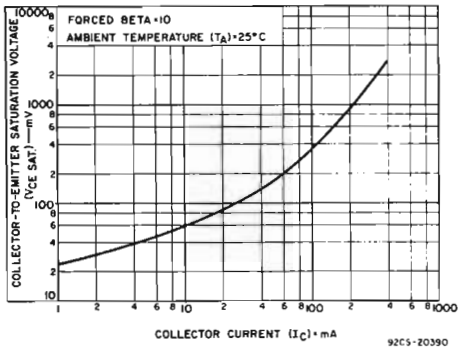


Fig.10—Collector-emitter saturation voltage vs. collector current of output transistor Q_{13}.

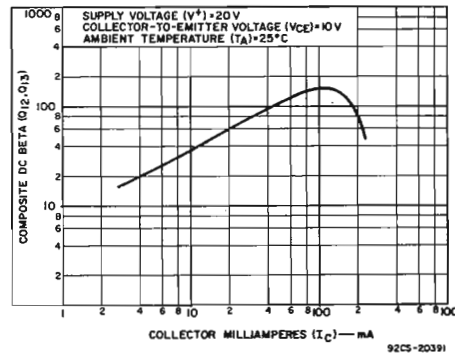


Fig.11—Composite dc beta vs. collector current of Darlington-connected output transistors Q_{12}, Q_{13}.

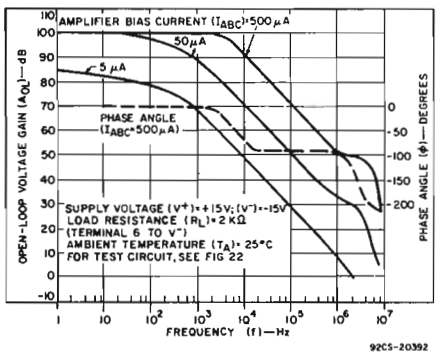


Fig.12—Open-loop voltage gain vs. frequency

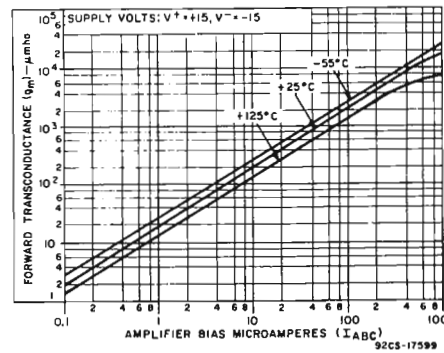


Fig.13—Forward transconductance vs. amplifier bias current.

Typical Characteristics Curves

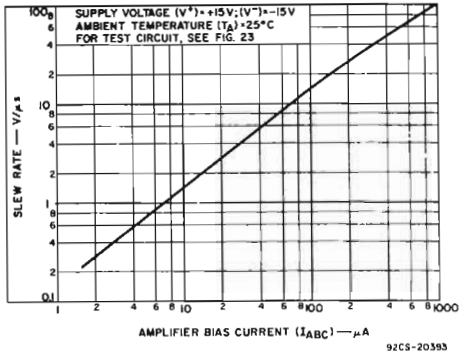


Fig. 14—Slew rate vs. amplifier bias current.

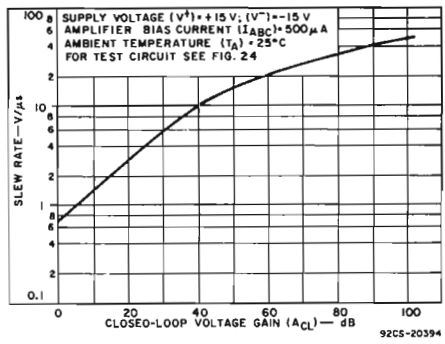


Fig. 15—Slew rate vs. closed-loop voltage gain.

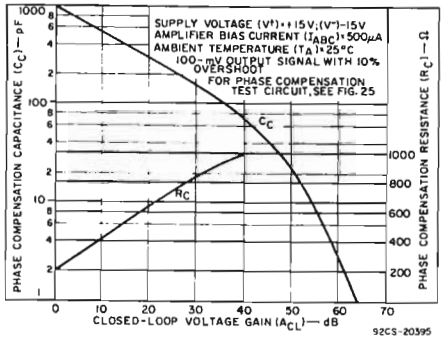


Fig. 16—Phase compensation capacitance and resistance vs. closed-loop voltage gain.

OPERATING CONSIDERATIONS

The "Sink" Output (terminal No. 8) and the "Drive" Output (terminal No. 6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between terminal No. 6 and terminal No. 4 (V^- or ground), it is important to connect a current-limiting resistor between terminal 8 and terminal No. 7 (V^+) to protect transistor Q_{13} under shorted load conditions. Similarly, if a load is connected between terminal No. 8 and terminal No. 7, the current-limiting resistor should be connected between terminal 6 and terminal No. 4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100-ohm current-limiting resistor be inserted between terminal No. 7 and the V^+ supply.

TEST CIRCUITS

1/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Fig. 21. This circuit is a 30-dB, non-inverting amplifier with emitter-follower output and phase compensation from terminal No. 2 to ground. Source resistors (Rs) are set to 0.Ω or 1 MΩ for ^{E} noise and ^{I} noise measurements, respectively. These measurements are made at frequencies of 10 Hz, 100 Hz, and 1 kHz with a 1-Hz measurement bandwidth. Typical values for 1/f noise at 10 Hz and 50 μA I_{ABC} are $E_n = 18\ nV/\sqrt{Hz}$ and $I_N = 1.8\ pA/\sqrt{Hz}$.

Test Circuits

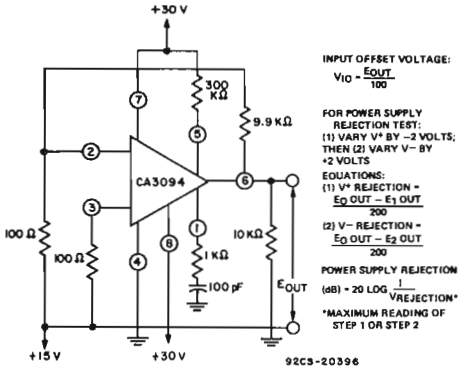


Fig.17—Input offset voltage and power-supply rejection test circuit.

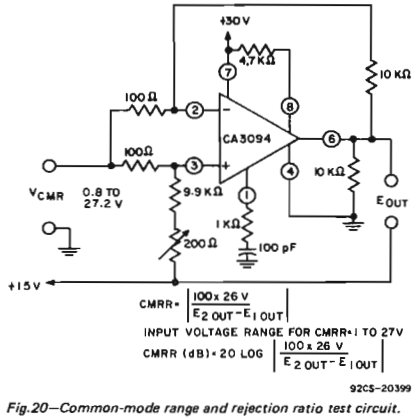


Fig.20—Common-mode range and rejection ratio test circuit.

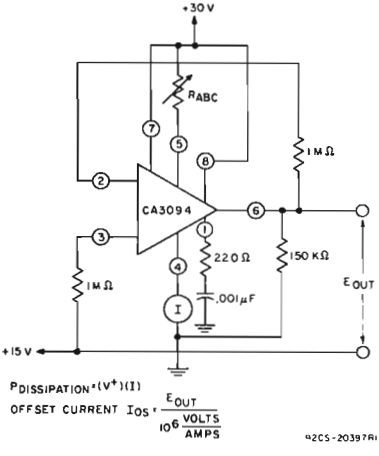


Fig.18—Input offset current test circuit.

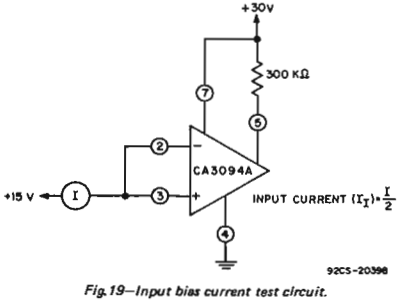
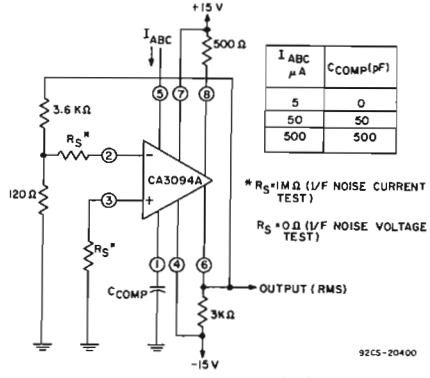
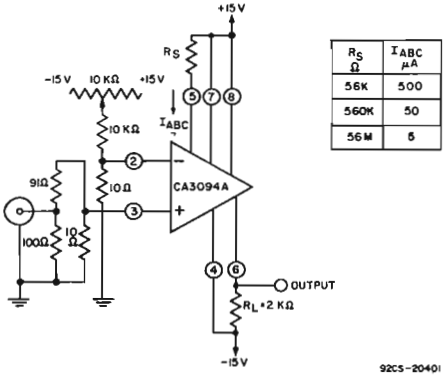


Fig.19—Input bias current test circuit.



IABC μA	CCOMP (pF)
5	0
50	50
500	500

Fig.21—1/F noise test circuit.



RS Ω	IABC μA
56K	500
560K	50
56M	5

Fig.22—Open-loop gain vs. frequency test circuit.

Test Circuits (cont'd)

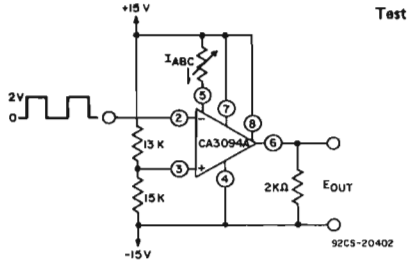


Fig.23—Open-loop slew rate vs. I_{ABC} test circuit.

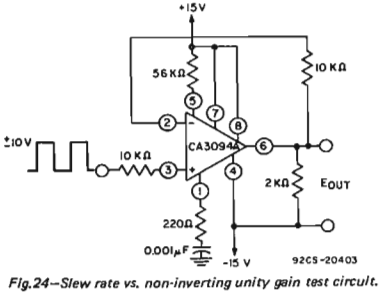
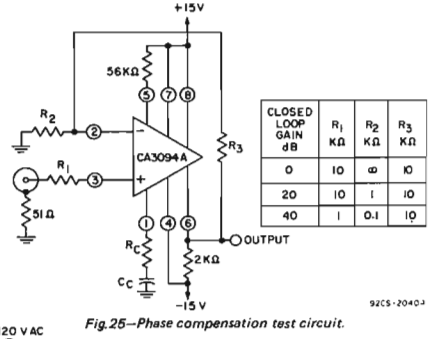
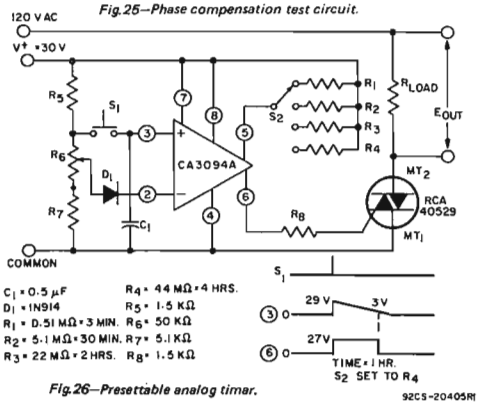


Fig.24—Slew rate vs. non-inverting unity gain test circuit.



CLOSED LOOP GAIN dB	R_1 KΩ	R_2 KΩ	R_3 KΩ
0	10	∞	10
20	10	1	10
40	1	0.1	10

Fig.25—Phase compensation test circuit.



C_1 = 0.5 μF
D_1 = 1N914
R_1 = 0.51 MΩ ± 3 MIN.
R_2 = 5.1 MΩ ± 30 MIN.
R_3 = 22 MΩ ± 2 HRS.
R_4 = 44 MΩ ± 4 HRS.
R_5 = 1.5 KΩ
R_6 = 50 KΩ
R_7 = 5.1 KΩ
R_8 = 1.5 KΩ

Fig.26—Presettable analog timer.

TYPICAL APPLICATIONS

For Additional Application Information, refer to Application Note ICAN-6048 "Some Applications of a Programmable Power/Switch Amplifier IC".

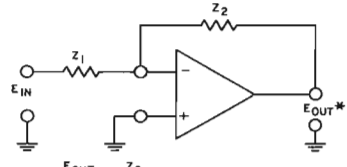
Design Considerations

The selection of the optimum amplifier bias current (I_{ABC}) depends on —

1. The Desired Sensitivity — the higher the I_{ABC}, the higher the sensitivity — i.e., a greater-drive current capability at the output for a specific voltage change at the input
2. Required Input Resistance — the lower the I_{ABC}, the higher the input resistance

If the desired sensitivity and required input resistance are not known and are to be experimentally determined, or the anticipated equipment design is sufficently flexible to tolerate a wide range of these parameters, it is recommended that the equipment designer begin his calculations with an I_{ABC} of 100 μA, since the CA3094 is characterized at this value of amplifier bias current.

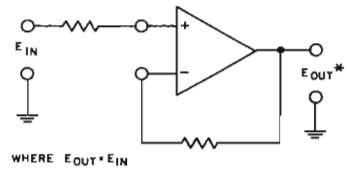
The CA3094 is extremely versatile and can be used in a wide variety of applications:



WHERE $\frac{E_{OUT}}{E_{IN}} = f\left(\frac{Z_2}{Z_1}\right)$ DEPENDS ON THE CHARACTERISTICS OF Z_1 AND Z_2

(a).

Fig. (a) As an inverting op-amp.



WHERE $E_{OUT} = E_{IN}$

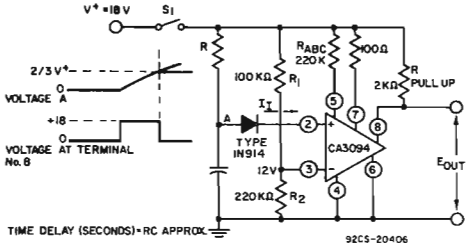
*IN SINGLE-ENDED OUTPUT OPERATION, THE CA3094 MAY REQUIRE A PULL UP OR PULL DOWN RESISTOR

(b)

92CS-20383

Fig. (b) In a non-inverting mode as a follower.

Typical Applications (cont'd)



Problem: To calculate the maximum value of R required to switch a 100-mA output current comparator

Given: $I_{ABC} = 5\ \mu A$, $R_{ABC} = 3.6\ M\Omega \approx \frac{18\ V}{5\ \mu A}$

$I_I = 500$ nA @ $I_{ABC} = 100\ \mu A$ (from Fig. 4)

$I_I = 5\ \mu A$ can be determined by drawing a line on Fig. 4 through $I_{ABC} = 100\ \mu A$ and $I_B = 500$ nA parallel to the typical $T_A = 25^oC$ curve.

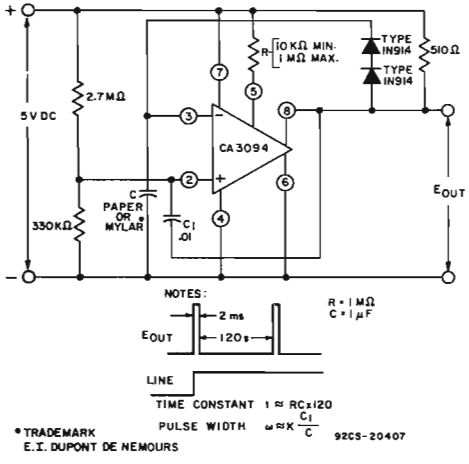
Then: $I_I = 33$ nA @ $I_{ABC} = 5\ \mu A$

$$R_{max} = \frac{18 - 12 \text{ volts}}{33\ nA} = 180\ M\Omega\ @\ T_A = 25^oC$$

$R_{max} = 180\ M\Omega \times 2/3^* = 120\ M\Omega\ @\ T_A = -55^oC$

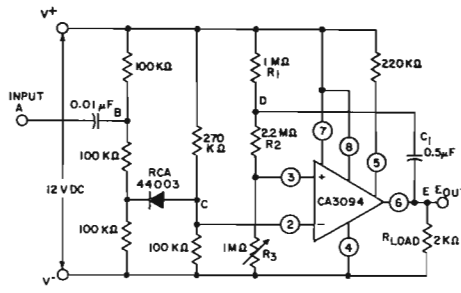
*Ratio of I_I at $T_A = +25^oC$ to I_I at $T_A = -55^oC$ for any given value of I_{ABC}.

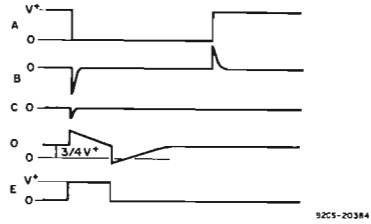
Fig.27—RC timer.



*TRADEMARK E.I. DUPONT DE NEMOURS

Fig.28—Free-running pulse generator.





On a negative-going transient at input (A), a negative pulse at C will turn "on" the CA3094, and the output (E) will go from a low to a high level.

At the end of the time constant determined by C_1, R_1, R_2, R_3, the CA3094 will return to the "off" state and the output will be pulled low by R_{LOAD}. This condition will be independent of the interval when input A returns to a high level.

Fig.29—RC timer triggered by external negative pulse.

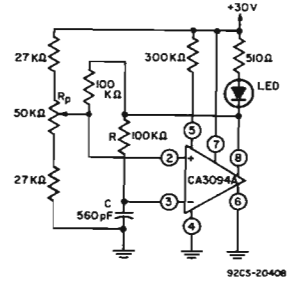


Fig.30—Single-supply astable multivibrator.

Typical Applications (cont'd)

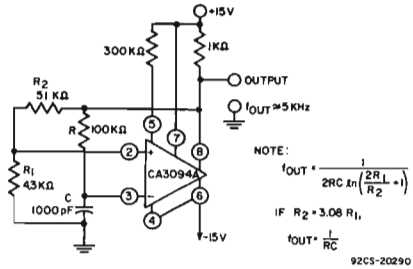
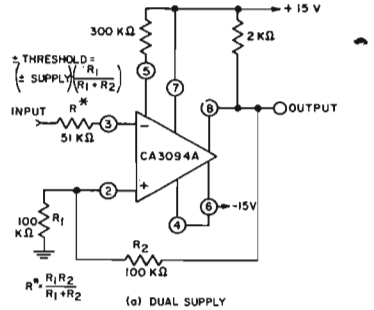


Fig.31—Op-amp astable multivibrator (dual-supply).



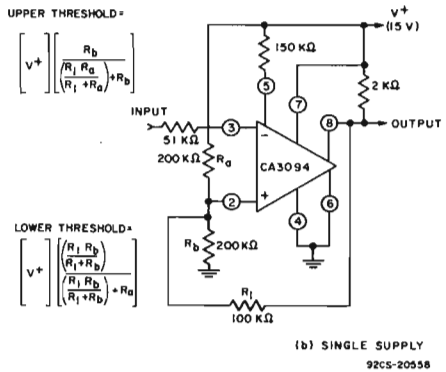


Fig.32—Comparator/threshold detector.

Typical Applications (cont'd)

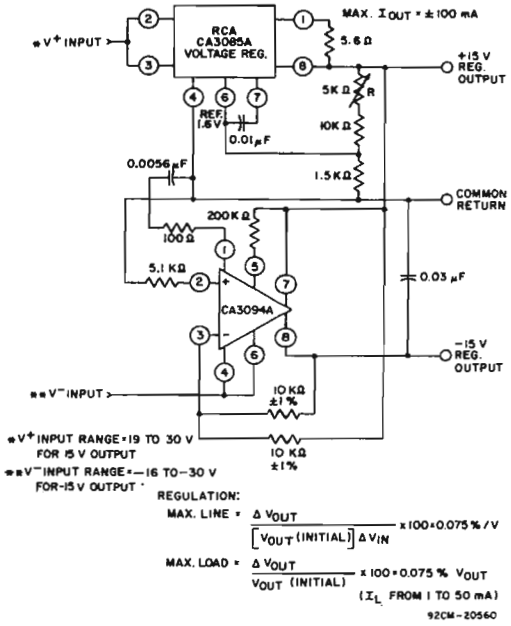


Fig.33—Dual tracking voltage regulator.

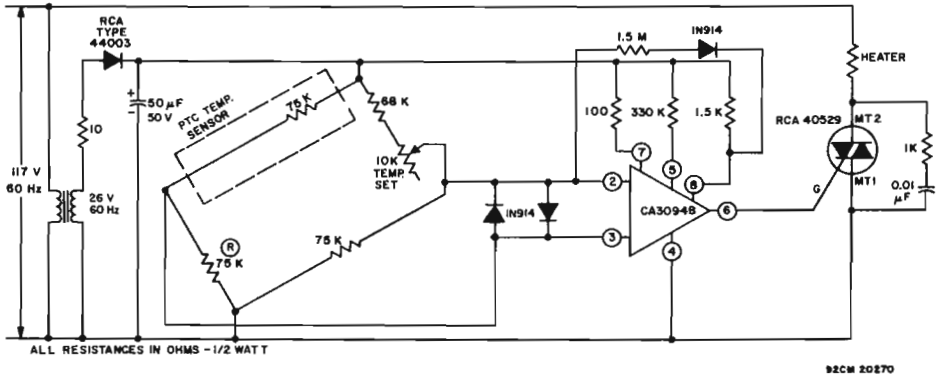
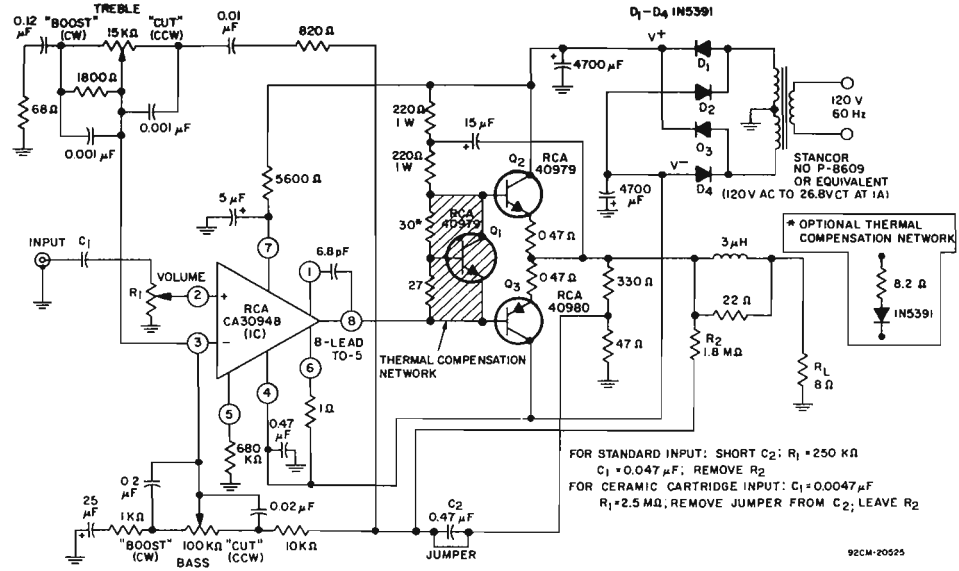


Fig.34—Temperature controller.



TYPICAL PERFORMANCE DATA — For 12-W Audio Amplifier Circuit

Power Output (8Ω load, Tone Control set at "Flat")		
Music (at 5% THD, regulated supply)	15	W
Continuous (at 0.2% IMD, 60 Hz & 2 kHz mixed in a 4:1 ratio, unregulated supply) See Fig. 8 In ICAN-6048	12	W
Total Harmonic Distoration		
At 1 W, unregulated supply	0.05	%
At 12 W, unregulated supply	0.57	%
Voltage Gain	40	dB
Hum and Noise (Below continuous Power Output)	83	dB
Input Resistance	250	kΩ
Tone Control Range	See Fig. 9 In ICAN-6048	

Fig.35— 12-watt amplifier circuit featuring a true-complementary output stage with CA3094 in driver stage.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3095E

16-Lead Dual-In-Line Plastic Package

Super-Beta Transistor Array

Differential Cascode Amplifier Plus 3 Independent Transistors

Applications

Differential Cascode Amplifier:

- Super-beta pre-amplifier for op-amp
- High-impedance dc meter amplifier
- Low-noise video amplifier
- Piezoelectric transducer amplifier
- Long-interval timer
- Long-duration one-shot multivibrator
- Comparator with high-input impedance
- Long-time-constant integrator
- Photocell amplifier
- Low-noise amplifier—for operation from high-source impedances

Independent Transistors:

- General use in signal processing systems in dc through vhf range

RCA-CA3095E* is a monolithic array of transistors connected as a super-beta differential cascode amplifier with three independent n-p-n transistors. (Refer to Fig. 1 for following description.)

The differential cascode amplifier incorporates two cascode amplifiers consisting of transistors Q1, Q3 and Q2, Q4, respectively, plus a voltage-limiting circuit, consisting of diodes D1, D2 and p-n-p transistor Q5. Two of these transistors, Q1 and Q2, are super-beta types that have an $h_{FE} > 1000$ and are capable of operating over a wide current range of 1 μA to 2 mA. Each of these types comprises the input section of its respective cascode amplifier. The output section of each cascode amplifier employs a conventional n-p-n transistor, Q3, Q4, respectively. The output signal is obtained at the collectors of these transistors. See Operating Considerations on page 8 for bias considerations of the differential cascode amplifier.

The exceptionally high-beta characteristics of Q1 and Q2, plus the large signal-voltage swing capability of Q3 and Q4, make the composite differential cascode amplifier an excellent choice for a broad range of small-signal, high-input-impedance amplifier applications including low-noise video amplifiers. This amplifier is also recommended for use in long-interval timers, oscillators, and long-duration one-shot applications.

The independent transistors, Q6, Q7 and Q8, are high-voltage silicon n-p-n conventional types for general use in signal processing systems in the frequency range from dc through vhf. Separate terminals for each of these transistors permit maximum flexibility in circuit design.

The CA3095E is supplied in a 16-lead dual-in-line plastic package and operates over the ambient temperature range of −55°C to +125°C

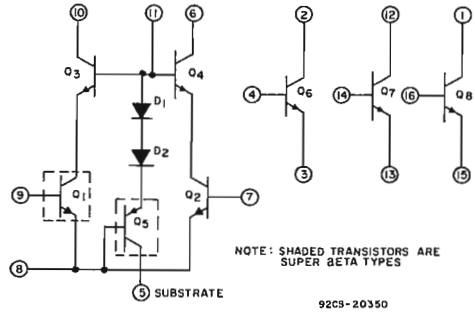
* Formerly developmental type TA6269X.

Features

- Two super-beta n-p-n transistors — $h_{FE} > 1000$
- Voltage-limiting circuitry (D1, D2, Q5)
- Operation possible at I_{IB} down to < 1 nA
- Matched pair (Q1 and Q2) —
  V_{IO} = 5 mV max. at I_C = 100 μA dc
  I_{IO} = 20 nA max. at I_C = 100 μA dc
- Wide current range — < 1 μA to 2 mA

Independent Transistors:

- h_{FE} = 300 typ. for each transistor
- Wide current range — < 1 μA to 10 mA
- Matched general-purpose transistors
- High voltage — V_{CBO} = 45 V max.



MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25\ ^\circ C$

Power Dissipation:		
Any One Transistor	300	mW
Total Package—		
Up to 25 °C	750	mW
Above 25 °C ..... derate linearly	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−55 to +150	°C
Lead Temperature (During Soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C
Voltage and Current Ratings Apply for Each Specified Transistor:		
Super-Beta Transistors (Q1, Q2)—		
Collector-to-Base Voltage (V_{CBO})	6	V
Emitter-to-Base Voltage (V_{EBO})	6	V
Collector-to-Substrate Voltage (V_{CIO})*	45	V
Collector Current (I_C)	50	mA
Base Current (I_B)	20	mA
Conventional N-P-N Transistors (Q3, Q4, Q6, Q7, Q8)—		
Collector-to-Base Voltage (V_{CBO})	45	V
Collector-to-Emitter Voltage (V_{CEO})	35	V
Emitter-to-Base Voltage (V_{EBO})	6	V
Collector-to-Substrate Voltage (V_{CIO})*	45	V
Collector Current (I_C)	50	mA
Base Current (I_B)	20	mA
Conventional P-N-P Transistor (Q5)—		
Collector-to-Base Voltage (V_{CBO})	−45	V
Collector-to-Emitter Voltage (V_{CEO})	−35	V
Limiting Circuit Current ($I_{Pin\ 11}$)	20	mA

* The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

STATIC CHARACTERISTICS

Characteristics	Symbol	Test Conditions $T_A = 25\ ^\circ C$		Limits Min.	Limits Typ.	Limits Max.	Units
Characteristics Apply for Each Super-Beta Cascode Amplifier Transistor Pair (Q1, Q3) and (Q2, Q4), Unless Indicated Otherwise							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A$, $I_E = 0$ See Note 1		6	–	–	V
Emitter-to-Base Breakdown Voltage (Applies only to Q1 & Q2)	$V_{(BR)EBO}$	$I_E = 100\ \mu A$, $I_C = 0$ Term. 9 to 8 or Term. 7 to 8		6	8	--	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 100\ \mu A$, $I_B = I_E = 0$		45	–	–	V
Collector Cutoff Current	I_{CER}	V_{6-8} or $V_{10-8} = 10$ V, $I_{11} = 100\ \mu A$ $R_{BE} = 100\ M\Omega$		–	–	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{10-8} = 5$ V or $V_{5-8} = 5$ V	$I_C = 1$ mA	–	1500	--	
			$I_C = 100\ \mu A$	1000	2000	5000	
			$I_C = 10\ \mu A$	–	1500	–	
Base-to-Emitter Voltage (Applies only to Q1 & Q2)	V_{BE}	$I_C = 100\ \mu A$, V_{6-8} or $V_{10-8} = 5$ V		0.50	0.59	0.68	V
Saturation Voltage	V_{sat}	I_6 or $I_{10} = 1$ mA, $I_{11} = 100\ \mu A$, I_7 or $I_9 = 100\ \mu A$		–	0.22	0.7	V
For Cascode Amplifiers as a Differential Matched Pair							
Magnitude of Input-Offset Voltage	$\lvert I_{IO} \rvert$	$I_C = 100\ \mu A$ $V_{6-8} = V_{10-8} = 5$ V		–	1	5	mV
Magnitude of Input-Offset Current	$\lvert I_{IO} \rvert$			–	4	20	nA
Magnitude of Input-Offset Voltage Drift (Temp. Coeff.)	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$			–	3.3	--	μV/°C
Magnitude of Input-Offset Current Drift (Temp. Coeff.)	$\frac{\lvert \Delta I_{IO} \rvert}{\Delta T}$			–	0.05	–	nA/°C

Note 1: Terminal No. 9 to terminals 10 and 11 connected or terminal No. 7 to terminals 6 and 11 connected.

STATIC CHARACTERISTICS (Cont'd)

Characteristics	Symbol	Test Conditions $T_A = 25\ ^\circ C$		Limits Min.	Typ.	Max.	Units
For Each Conventional n-p-n Transistor (Q3, Q4, Q6, Q7, Q8)							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A$, $I_E = 0$		45	95	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$		35	50	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 100\ \mu A$, $I_C = 0$		6	8	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 100\ \mu A$, $I_B = I_E = 0$		45	95	–	V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$		–	–	100	nA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$		–	–	10	nA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 5$ V	$I_C = 10$ mA	–	210	–	
			$I_C = 1$ mA	150	300	500	
			$I_C = 10\ \mu A$	–	180	–	
Base-to-Emitter Voltage	V_{BE}	$I_C = 1$ mA, $V_{CE} = 5$ V		0.60	0.69	0.78	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10$ mA, $I_B = 1$ mA		–	0.22	0.7	V

Dynamic Characteristics

Characteristics	Symbol	Test Conditions $T_A = 25\ ^\circ C$	Limits Min.	Typ.	Max.	Units
Characteristics Apply for Each Super-Beta Cascode Amplifier Transistor Pair (Q1, Q3), Unless Indicated Otherwise						
Gain-Bandwidth Product	f_T	$I_C = 100\ \mu A$, $V_{6-8} = V_{10-8} = 5$ V,	–	78	–	MHz
Noise Voltage (Referred to Input) For Differential Amplifier Operation	E_N	$I_C = 50\ \mu A$, f = 10 Hz	–	13	–	$nV/\sqrt{Hz}$
Noise Current (Referred to Input) For Differential Amplifier Operation	I_N	$I_C = 5\ \mu A$, f = 10 Hz	–	0.12	–	$pA/\sqrt{Hz}$
Collector-to-Base Capacitance	C_{CB}	$V_{6-7} = V_{10-9} = 5$ V, $I_E = 0$	–	0.3		pF
Collector-to-Substrate Capacitance	C_{CIO}	$V_{6-5} = V_{10-5} = 5$ V, $I_B = 0$	–	3.0	–	pF
For Each Conventional Transistor (Q3 through Q8)						
Gain-Bandwidth Product	f_T	$I_C = 100\ \mu A$, $V_{CE} = 5$ V	–	100	–	MHz
		$I_C = 3$ mA, $V_{CE} = 5$ V	–	320	–	
Noise Voltage (Referred to Input)	E_N	$I_C = 100\ \mu A$, $V_{CE} = 5$ V, f = 10 Hz	–	5	–	$nV/\sqrt{Hz}$
Noise Current (Referred to Input)	I_N	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, f = 10 Hz	–	0.8	–	$pA/\sqrt{Hz}$
Collector-to-Base Capacitance	C_{CB}	$V_{CB} = 5$ V, $I_E = 0$	–	0.4	–	pF
Collector-to-Substrate Capacitance	C_{CIO}	$V_{CI} = 5$ V, $I_B = 0$	–	2	–	pF

* Curve plotted for I_{CEO} characteristic.

Test Circuits for Measurement of Super-Beta Cascode Amplifier Characteristics

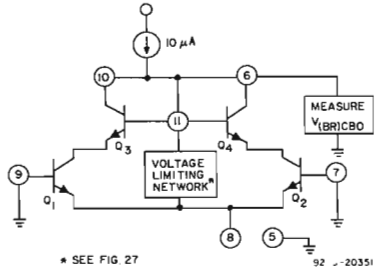


Fig.2–$V_{(BR)CBO}$ test circuit.

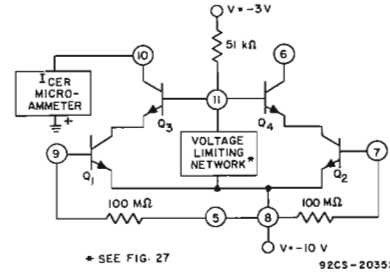


Fig.3–I_{CER} test circuit

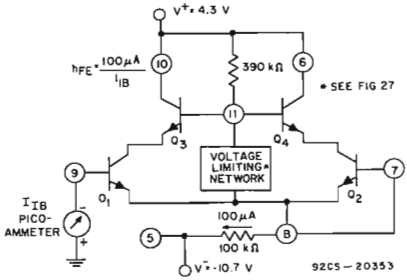


Fig.4–DC Beta (h_{FE}) test circuit.

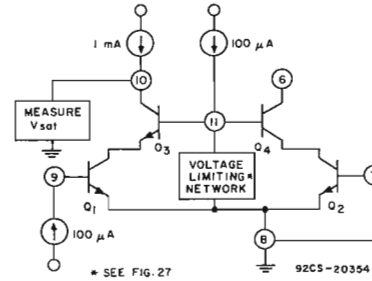


Fig.5–V_{sat} test circuit for super-beta cascode pairs.

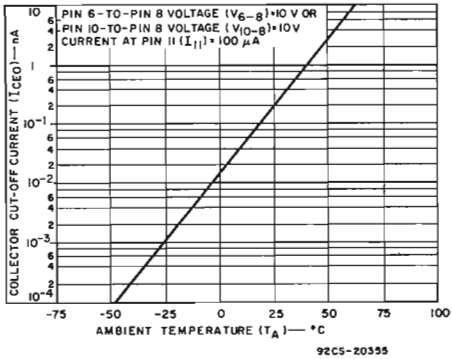


Fig.6–Collector cut-off current vs ambient temperature for super-beta cascode pairs.

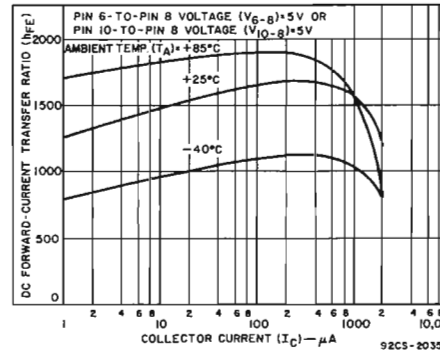


Fig.7–h_{FE} vs. I_C for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

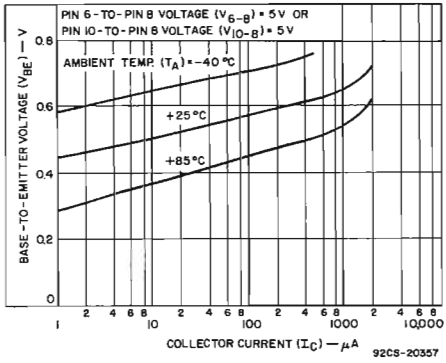


Fig.8—V_{BE} vs. I_C for each super-beta transistor (Q1 and Q2).

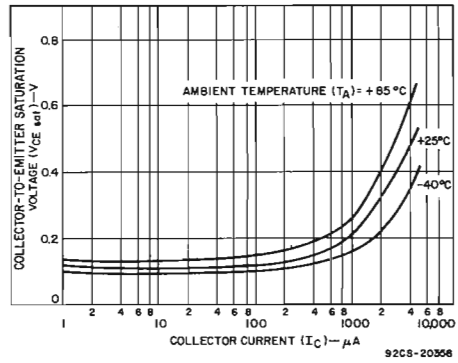


Fig.9—$V_{CE(sat)}$ vs. I_C for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

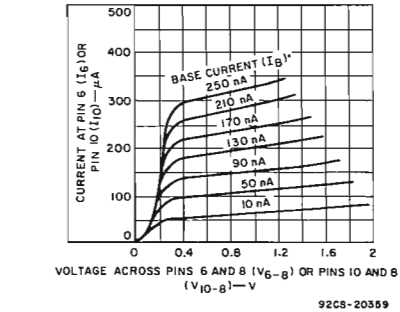


Fig.10—I-V characteristics for the super-beta cascode pairs.

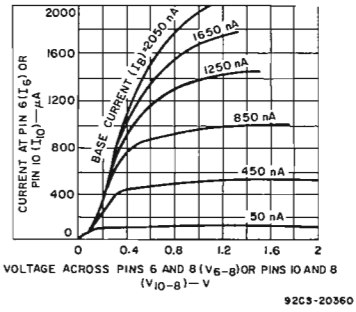


Fig.11—I-V characteristics for the super-beta cascode pairs.

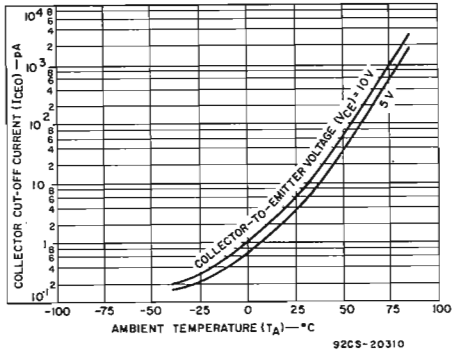


Fig.12—Collector cutoff current vs ambient temperature for the conventional transistors (V_{CE} = 5 V, 10 V).

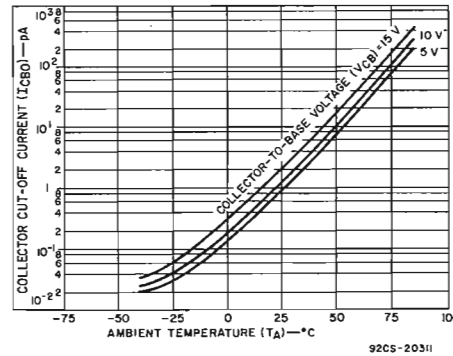


Fig.13—Collector cutoff current vs ambient temperature for the conventional transistors (V_{CB} = 5 V, 10 V, 15 V).

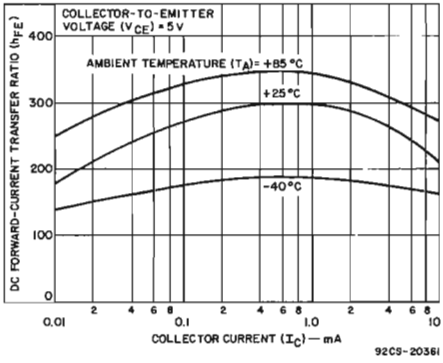


Fig.14—h_{FE} vs. I_C for each conventional transistor (Q6, Q7, Q8).

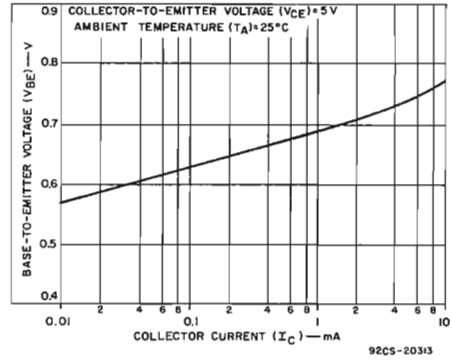


Fig.15—V_{BE} as a function of collector current for the conventional transistors.

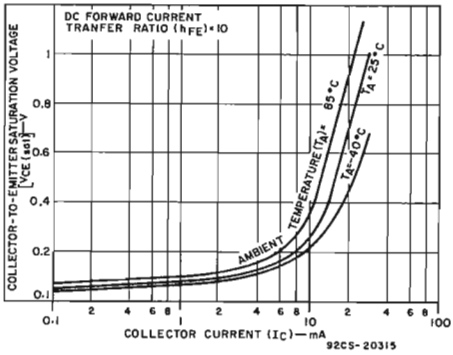


Fig.16—$V_{CE(sat)}$ as a function of collector current for the conventional transistors.

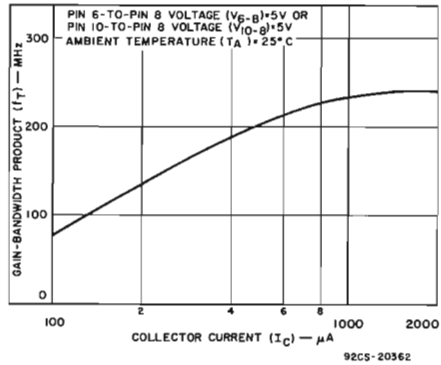


Fig.17—Gain bandwidth product vs collector current for the super-beta cascode pairs.

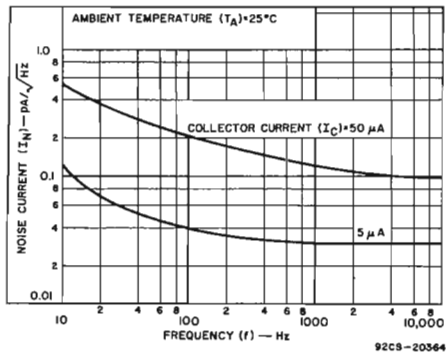


Fig.18—I_N vs. f for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

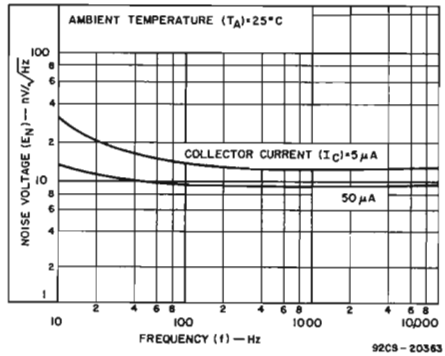


Fig.19—E_N vs. f for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

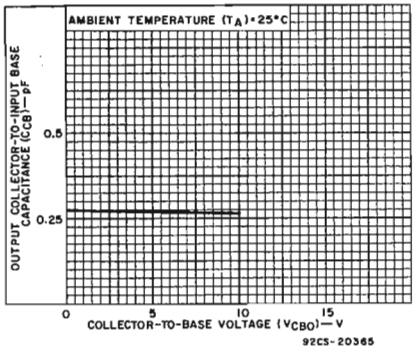


Fig.20–C_{CB} vs. V_{CBO} for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

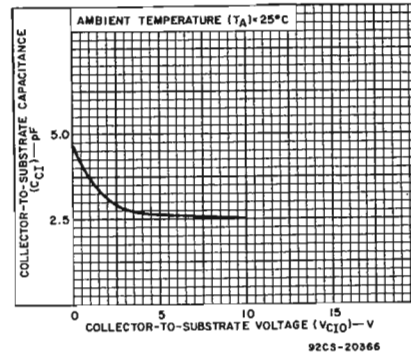


Fig.21–C_{CI} vs. V_{CIO} for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

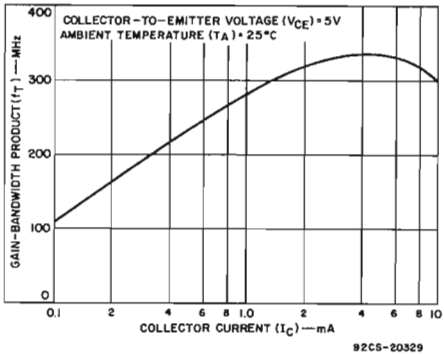


Fig.22–Gain bandwidth product vs collector current for the conventional transistors.

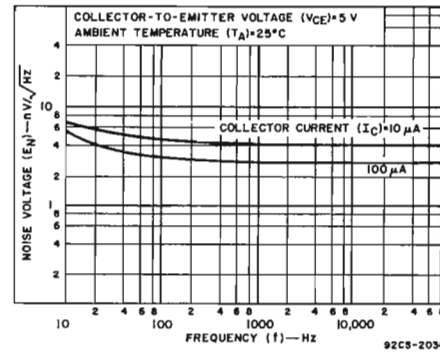


Fig.23–Noise voltage vs frequency for the conventional transistors.

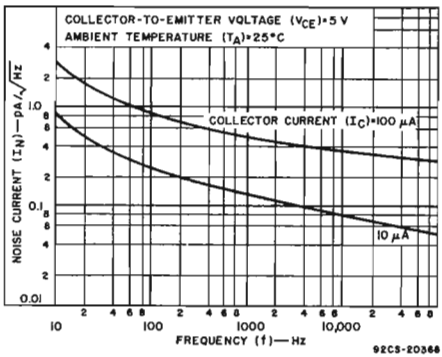


Fig.24–I_N vs. f for each conventional transistor (Q6, Q7, Q8).

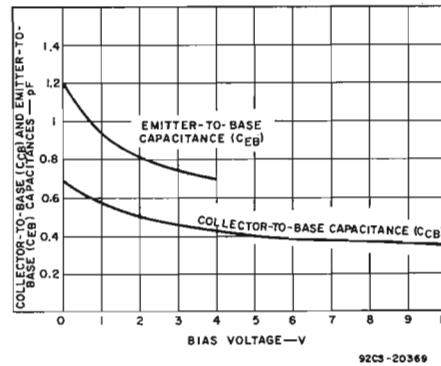


Fig.25–Collector-to-base and emitter-to-base capacitances vs bias voltage for the conventional transistors.

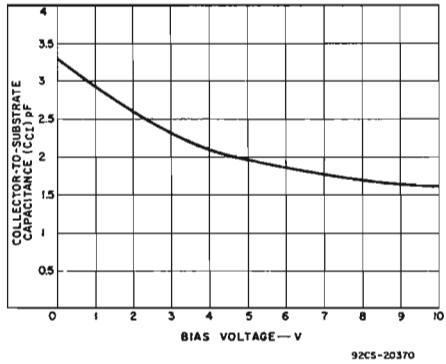


Fig.26—Collector-to-substrate capacitance vs bias voltage for the conventional transistors.

TYPICAL APPLICATIONS

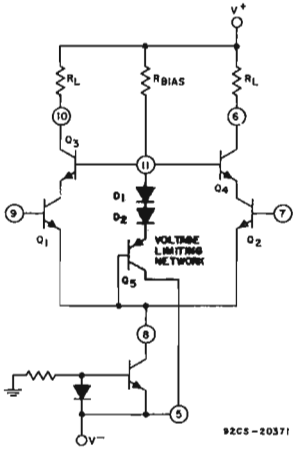


Fig.27—Bias arrangement for operation of the super-beta differential cascode amplifier.

Operating Considerations

Operation Considerations for the Super-Beta Differential Cascode Amplifier

An internal voltage-limiting network (diodes D1, D2 and p-n-p transistor Q5) incorporated in the differential cascode amplifier, assures that the applied collector-to-emitter voltage of each super-beta unit is maintained below two volts. Fig. 27 shows a typical bias arrangement of the super-beta differential cascode amplifier.

Bias current for this network must be supplied by an external source. This bias current can be obtained by simply connecting a resistor from Pin 11 to the positive supply of the differential amplifier. The return path for most of the bias current is through the substrate, Pin 5, rather than through the common emitter, Pin 8. This arrangement provides superior common-mode and power-supply rejection. As a general rule-of-thumb, the current supplied into Pin 11 should be approximately 0.04 to 0.1 times the value of the quiescent current of Pin 8.

TYPICAL APPLICATIONS (Cont'd)

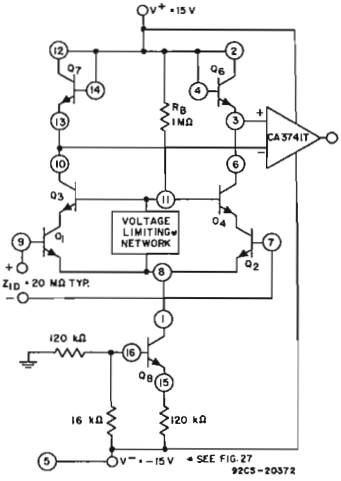


Fig.28—Super-beta Op-Amp with diode drive network.

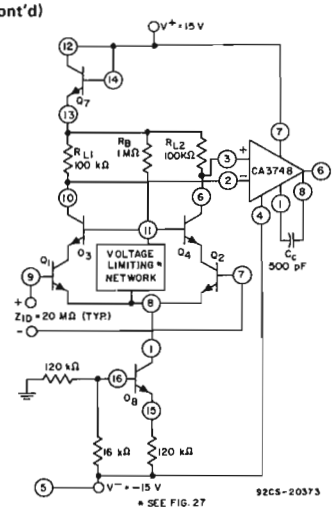


Fig.29—Super-beta Op-Amp with resistor drive network.

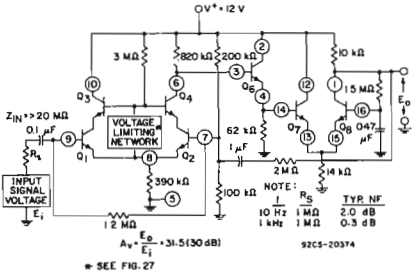


Fig.30—High-input-impedance, low-noise amplifier circuit.

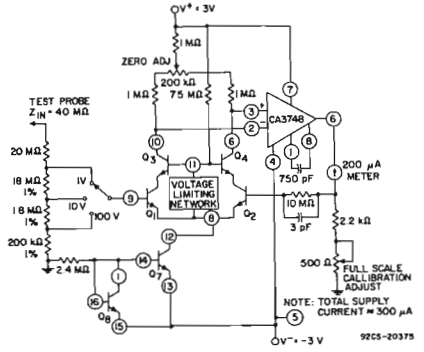


Fig.31—Typical high-input-impedance dc voltmeter circuit.

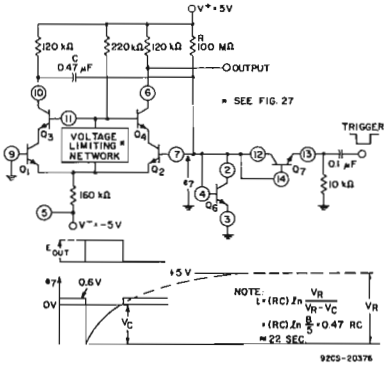


Fig.32—Long-delay monostable multivibrator circuit.

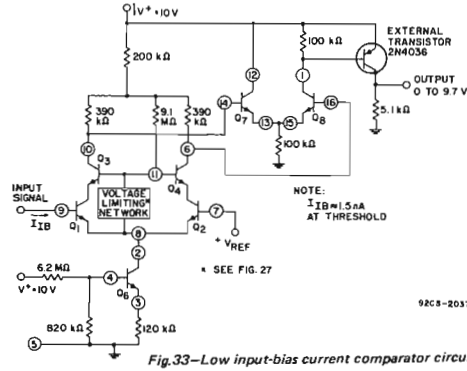


Fig.33—Low input-bias current comparator circuit.

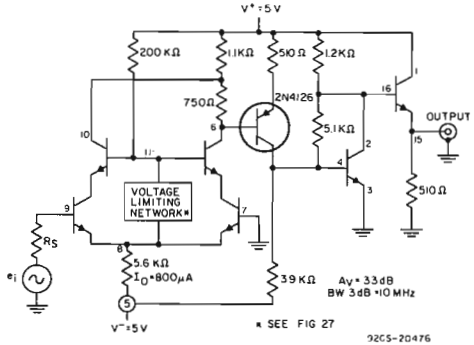


Fig.34—CA3095E wideband amplifier.

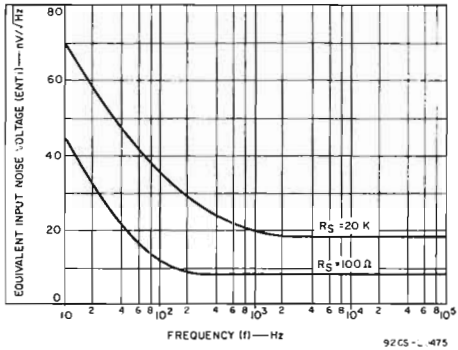


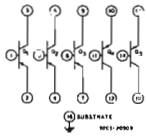
Fig.35—Equivalent input noise voltage vs. frequency for circuit of figure 34.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA3096AE
CA3096E



Schematic Diagram

H-1622

N-P-N/P-N-P Transistor-Array IC

Features:

- Matched General-Purpose Transistors (CA3096AE Only)
- Input Offset Voltage ±5 mV
- Input Offset Current:
  p-n-p Pair ±250 nA max. @ I_C = −100 μA
  n-p-n Pair ±0.6 μA max. @ I_C = 1 mA
- High h_{FE}
  n-p-n transistor: 150 min. @ I_C = 1 mA
  p-n-p transistor: 40 min. @ I_C = 100 μA
- High Breakdown Voltages:
  n-p-n transistor: $V_{(BR)CEO}$ = 35 V min; $V_{(BR)CBO}$ = 45 V min.
  p-n-p transistor: $V_{(BR)CEO}$ = 40 V min; $V_{(BR)CBO}$ = 40 V min.
- Separate Substrate Connection
- Low Noise Figure:
  n-p-n transistor: 2.2 dB typ. at 1 kHz
  p-n-p transistor: 3 dB typ. at 1 kHz

RCA-CA3096E● and CA3096AE● are general-purpose high-voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096AE and CA3096E are identical, except that the CA3096AE specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and $V_{CE(SAT)}$ (see Table I).

CA3096E and CA3096AE are supplied in 16-lead dual-in-line plastic packages.

Applications:

- Differential Amplifiers
- DC Amplifiers
- Sense Amplifiers
- Level Shifters
- Timers
- Lamp and Relay Drivers
- Thyristor Firing Circuits
- Temperature-Compensated Amplifiers
- Operational Amplifiers

● Formerly RCA Developmental No. TA6270.

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

		Each n-p-n Transistor	Each p-n-p Transistor	
Collector-to-Emitter Voltage	V_{CEO}	35	−40	V
Collector-to-Base Voltage	V_{CBO}	45	−40	V
Collector-to-Substrate Voltage	V_{CIO}	45	−45	V
Emitter-to-Base Voltage	V_{EBO}	6	−40	V
Collector Current	I_C	50	−10	mA
Dissipation P_D:				
Up to T_A = 55 °C:				
Device (Total)		750		mW
Each Transistor		200		mW
Above T_A = 55 °C		Derate Linearly 6.67		mW/°C

Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering)		
At distance 1/16 ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

TABLE I—CA3096AE AND CA3096E ESSENTIAL DIFFERENCES*

RCA TYPE	I_{CBO} (nA)		I_{CEO} (nA)		$V_{CE(SAT)}$ (V)		$\lvert V_{IO}\rvert$ (mV)		$\lvert I_{IO}\rvert$ (μA)	
	n-p-n	p-n-p	n-p-n	p-n-p	n-p-n	p-n-p	n-p-n	p-n-p	n-p-n	p-n-p
CA3096AE	40	−40	100	−100	0.7	0.4	5	5	0.6	0.25
CA3096E	100	−100	1000	−1000	1.0	0.7	—	—	—	—

* Maximum values.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$ (For Equipment Design)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	CA3096AE, CA3096E LIMITS			UNITS
			Min.	Typ.	Max.	
For Each n-p-n Transistor:						
Collector-Cutoff Current (CA3096AE)	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	0.0013	40	nA
Collector-Cutoff Current (CA3096AE)	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	0.0055	100	nA
Collector-Cutoff Current (CA3096E)	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	0.0013	100	nA
Collector-Cutoff Current (CA3096E)	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	0.0055	1	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	35	50	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	45	100	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 10 μA, I_B = I_E = 0	45	100	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	6	8	–	V
Emitter-to-Base Zener Voltage	V_Z	I_Z = 10 μA	6	7.9	9.8	V
Collector-to-Emitter Saturation Voltage (CA3096AE)	$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA	–	0.24	0.5	V
Collector-to-Emitter Saturation Voltage (CA3096E)	$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA	–	0.24	0.7	V
Base-to-Emitter Voltage	V_{BE}	I_C = 1 mA, V_{CE} = 5 V	0.6	0.69	0.78	V
DC Forward-Current Transfer Ratio	h_{FE}		150	390	500	
Magnitude of Temperature Coefficient: V_{BE} (for each transistor)	$\lvert\Delta V_{BE}/\Delta T\rvert$	I_C = 1 mA, V_{CE} = 5 V	–	−1.9	–	mV/°C
For Each p-n-p Transistor:						
Collector-Cutoff Current (CA3096AE)	I_{CBO}	V_{CB} = −10 V, I_E = 0	–	−0.055	40	nA
Collector-Cutoff Current (CA3096AE)	I_{CEO}	V_{CE} = −10 V, I_B = 0	–	−0.12	100	nA
Collector-Cutoff-Current (CA3096E)	I_{CEO}	V_{CE} = −10 V, I_B = 0	–	−0.12	1	μA
Collector-Cutoff-Current (CA3096E)	I_{CBO}	V_{CB} = −10 V, I_E = 0	–	−0.055	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = −100 μA, I_B = 0	−40	−75	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = −10 μA, I_E = 0	−40	−80	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = −10 μA, I_C = 0	−40	−100	–	V
Emitter-to-Base Zener Voltage	V_Z	I_Z = 10 μA	10	16	–	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	I_{EI} = 10 μA, I_B = I_C = 0	−40	−100	–	V
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = −1 mA, I_B = −100 μA	–	−0.16	−0.4	V
Base-to-Emitter Voltage	V_{BE}	I_C = −100 μA, V_{CE} = −5 V	−0.5	−0.6	−0.7	V
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −100 μA, V_{CE} = −5 V	40	85	200	
		I_C = −1 mA, V_{CE} = −5 V	20	47	150	
Magnitude of Temperature Coefficient: V_{BE} (for each transistor)	$\lvert\Delta V_{BE}/\Delta T\rvert$	I_C = −100 μA, V_{CE} = −5 V	–	−2.2	–	mV/°C
For Transistors Q1 and Q2 (As a Differential Amplifier): CA3096AE ONLY						
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 5 V, I_C = 1 mA	–	0.3	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		–	0.07	0.6	μA
Absolute Input Offset Voltage Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$		–	1.1		μV/°C
For Transistors Q4 and Q5 (As a Differential Amplifier): CA3096AE ONLY						
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = −5 V, I_C = −100 μA, R_S = 0	–	0.15	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		–	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$		–	0.54	–	μV/°C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$
Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each n-p-n Transistor				
Noise Figure (low frequency)	NF	f = 1 kHz, V_{CE} = 5 V, I_C = 1 mA, R_S = 1 kΩ	2.2	dB
Low-Frequency, Input Resistance	R_i	f = 1.0 kHz, V_{CE} = 5 V, I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance	R_o		80	kΩ
Admittance Characteristics:				
Forward Transfer Admittance	Y_{fe} g_{fe} / b_{fe}	f = 1 MHz, V_{CE} = 5 V, I_C = 1 mA	7.5 −j13	mmho
Input Admittance	Y_{ie} g_{ie} / b_{ie}		2.2 j3.1	mmho
Output Admittance	Y_{oe} g_{oe} / b_{oe}		0.76 j2.4	mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5 V, I_C = 1.0 mA V_{CE} = 5 V, I_C = 5 mA	280 335	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V	0.75	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V	0.46	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 3 V	3.2	pF
For Each p-n-p Transistor				
Noise Figure (low frequency)	NF	f = 1 kHz, I_C = 100 μA, R_S = 1 kΩ	3	dB
Low-Frequency Input Resistance	R_i	f = 1 kHz, V_{CE} = 5 V, I_C = 100 μA	27	kΩ
Low-Frequency Output Resistance	R_o		680	kΩ
Gain-Bandwidth Product	f_T	V_{CE} = 5 V, I_C = 100 μA	6.8	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = −3 V	0.85	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = −3 V	2.25	pF
Base-to-Substrate Capacitance	C_{BI}	V_{BI} = 3 V	3.05	pF

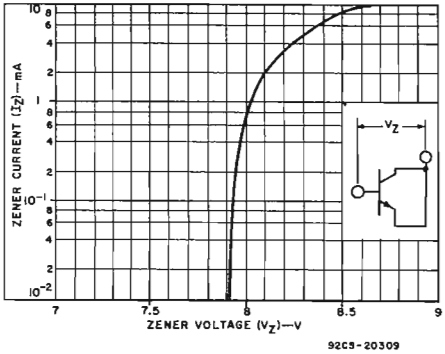


Fig.1—Base-to-emitter zener characteristic (n-p-n).

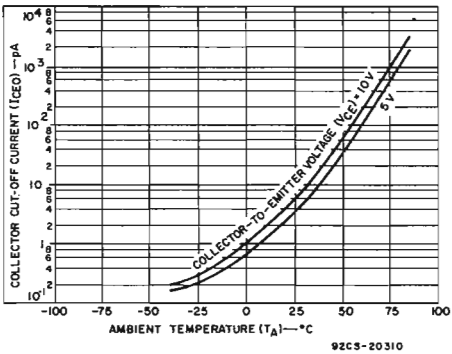


Fig.2—Collector cut-off current (I_{CEO}) as a function of temperature (n-p-n).

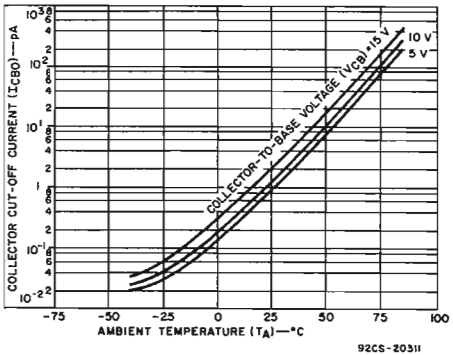


Fig.3—Collector cut-off current (I_{CBO}) as a function of temperature (n-p-n).

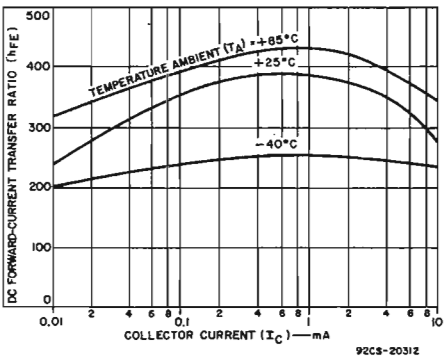


Fig.4—Transistor (n-p-n) h_{FE} as a function of collector current.

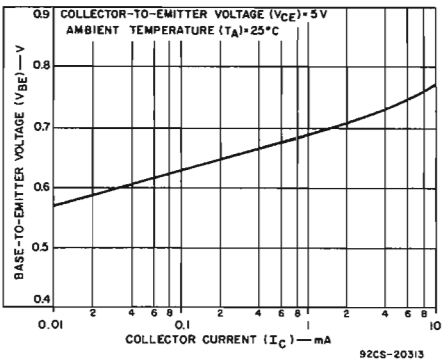


Fig.5—V_{BE} (n-p-n) as a function of collector current.

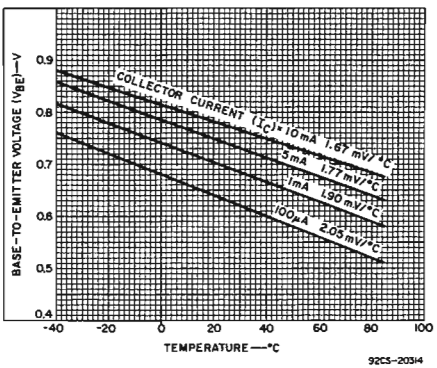


Fig.6—V_{BE} (n-p-n) as a function of temperature.

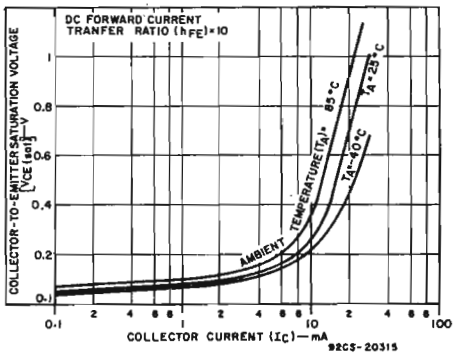


Fig.7—$V_{CE(SAT)}$(n-p-n) as a function of collector current.

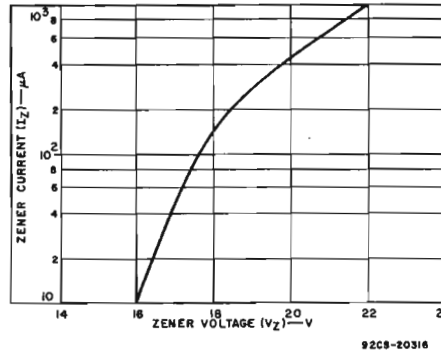


Fig.8—Base-to-emitter zener characteristic (p-n-p).

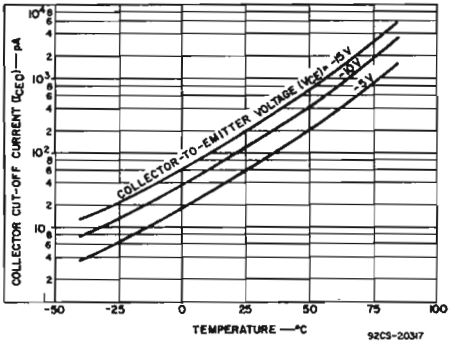


Fig.9—Collector cut-off current (I_{CEO}) as a function of temperature (p-n-p).

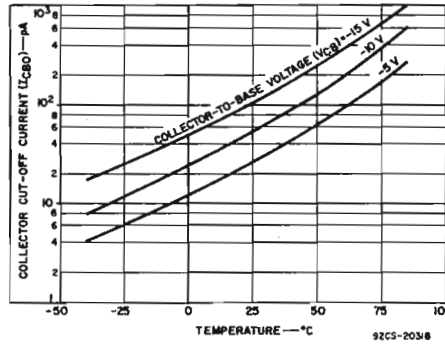


Fig.10—Collector cut-off current (I_{CBO}) as a function of temperature (p-n-p).

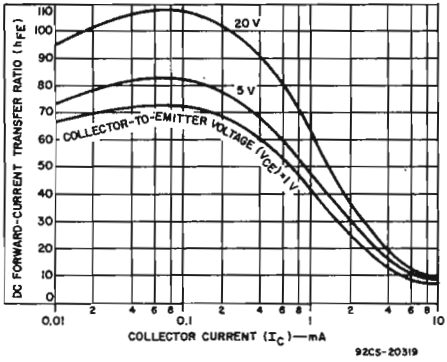


Fig.11—Transistor (p-n-p) h_{FE} as a function of collector current.

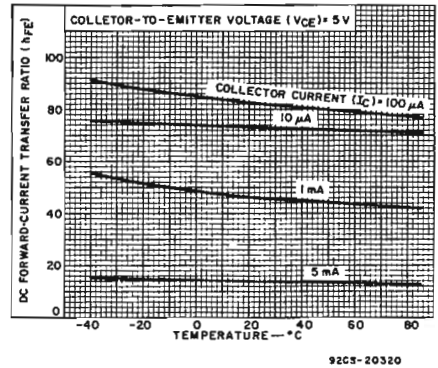


Fig.12—Transistor (p-n-p) h_{FE} as a function of temperature.

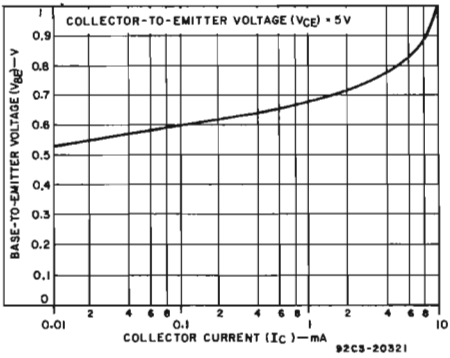


Fig.13—V_{BE} (p-n-p) as a function of collector current.

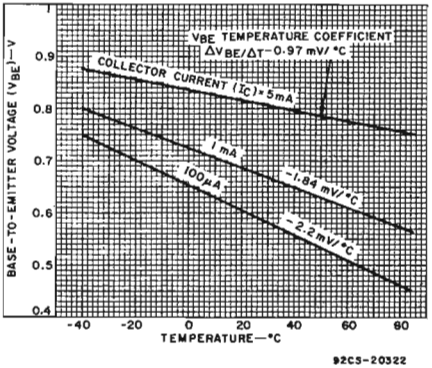


Fig.14—V_{BE} (p-n-p) as a function of temperature.

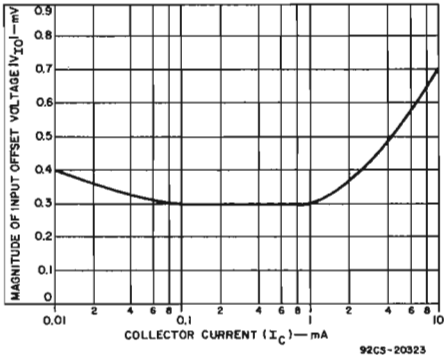


Fig.15—Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for n-p-n transistor Q_1—Q_2.

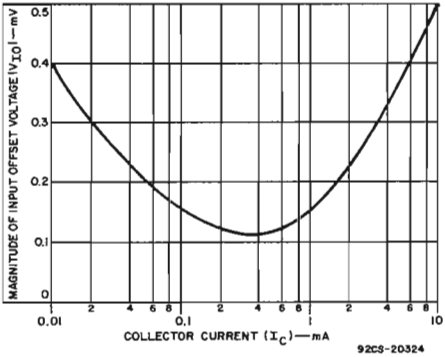


Fig.16—Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for p-n-p transistors Q_4—Q_5.

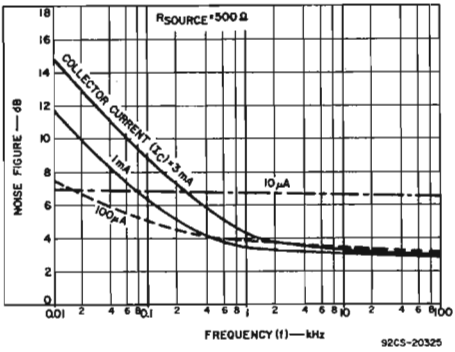


Fig.17—Noise figure as a function of frequency for n-p-n transistors.

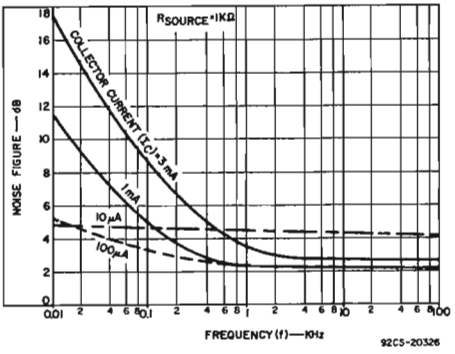


Fig.18—Noise figure as a function of frequency for n-p-n transistors.

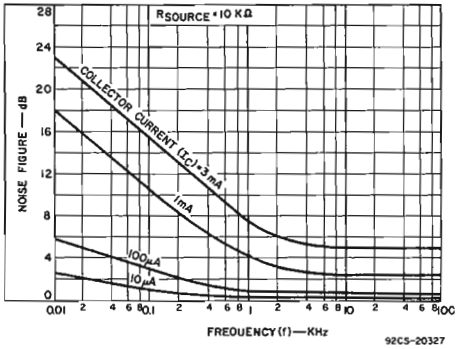


Fig.19—Noise as a function of frequency for n-p-n transistors.

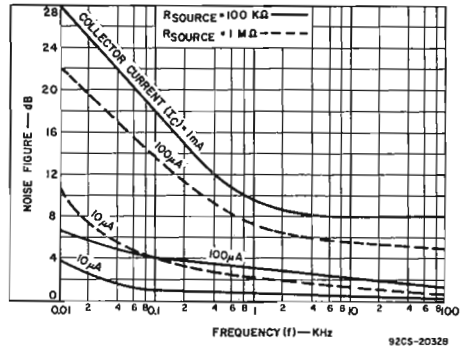


Fig.20—Noise figure as a function of frequency for n-p-n transistors.

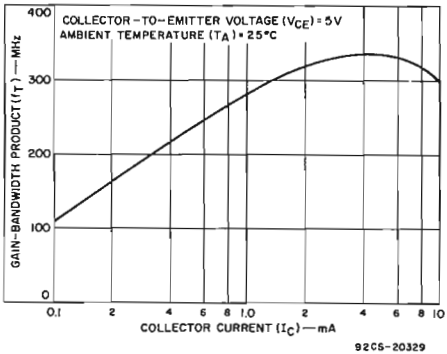


Fig.22—Capacitance as a function of bias voltage (n-p-n).

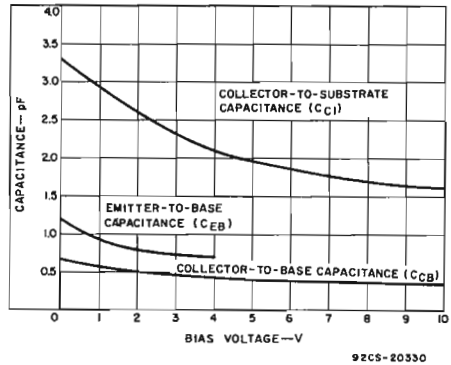


Fig.21—Gain-bandwidth product as a function of collector current (n-p-n).

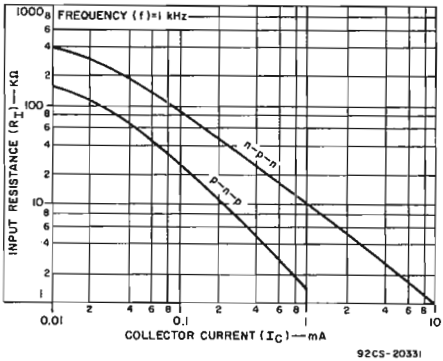


Fig.23—Input resistance as a function of collector current.

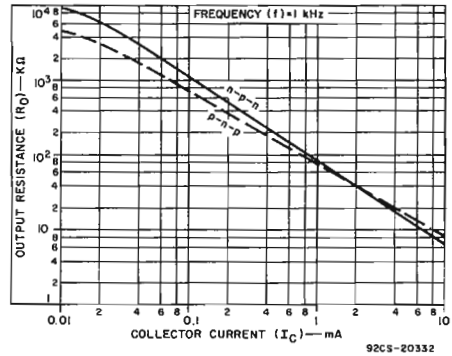


Fig.24—Output resistance as a function of collector current.

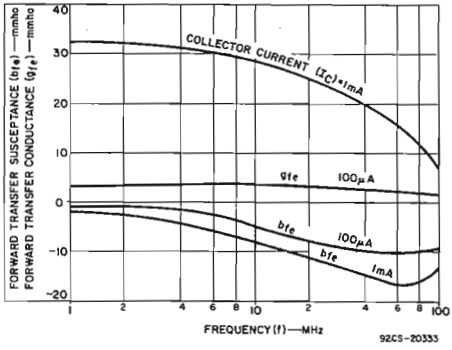


Fig.25—Forward transconductance as a function of frequency.

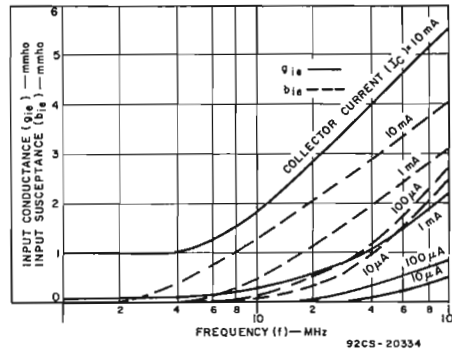


Fig.26—Input admittance as a function of frequency.

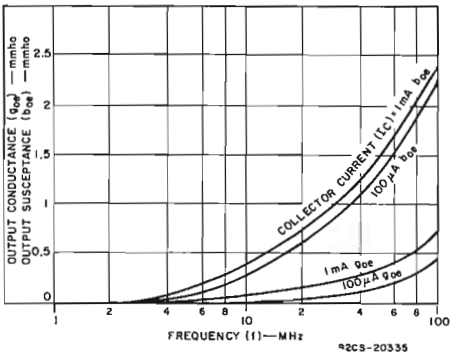


Fig.27—Output admittance as a function of frequency.

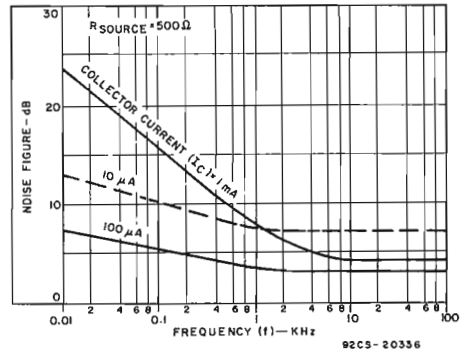


Fig.28—Noise figure as a function of frequency (p-n-p).

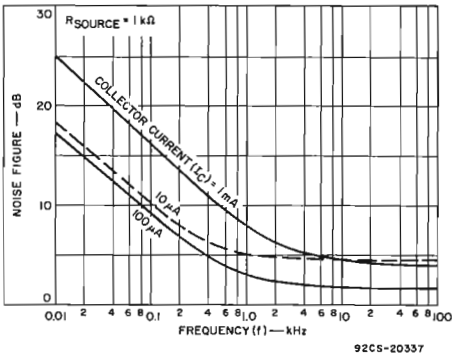


Fig.29—Noise figure as a function of frequency (p-n-p).

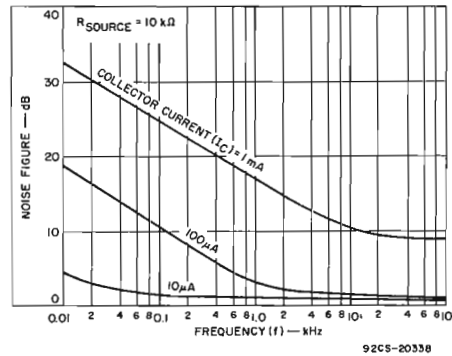


Fig.30—Noise figure as a function of frequency (p-n-p).

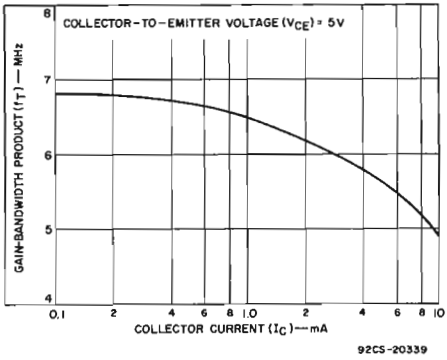


Fig.31—Gain-bandwidth product as a function of collector current (p-n-p).

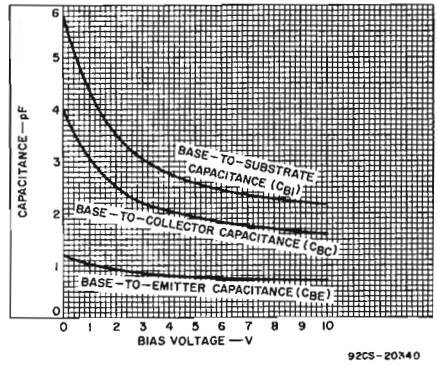


Fig.32—Capacitance as a function of bias voltage (p-n-p).

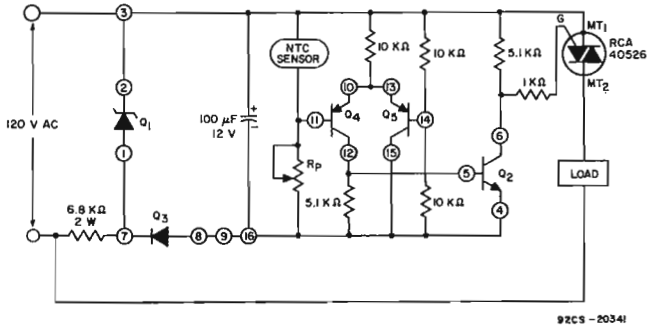


Fig.33—Line-operated level switch using CA3096AE or CA3096E.

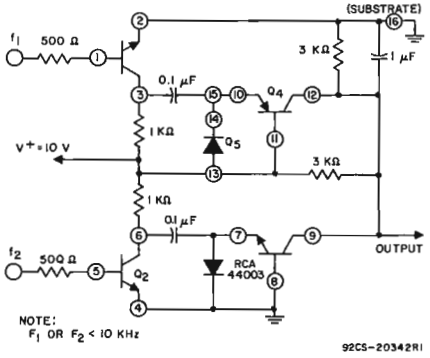


Fig.34a—Frequency comparator using CA3096E.

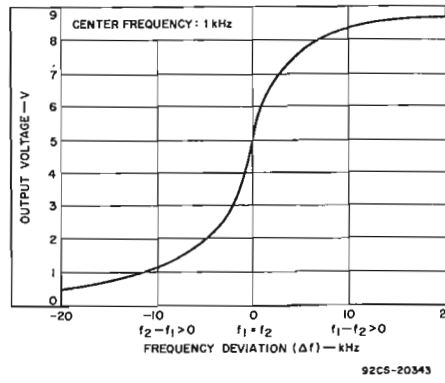
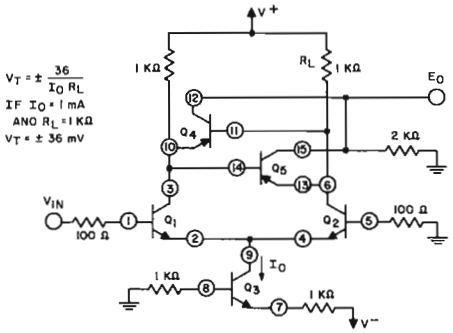


Fig.34b—Frequency comparator characteristics.



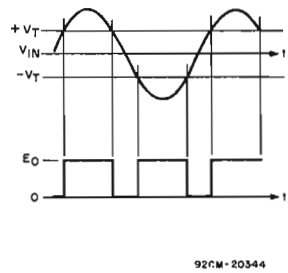


Fig.35—CA3096AE small-signal zero-voltage detector having noise immunity.

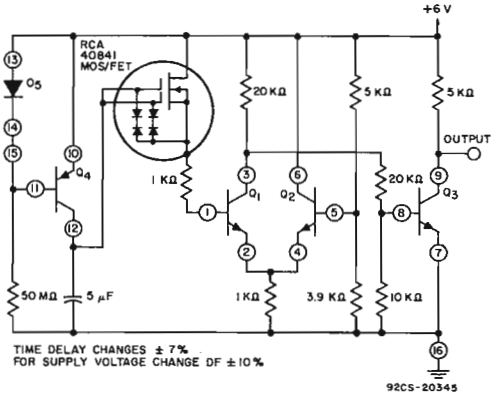


Fig.36a—One-minute timer using CA3096AE and a MOS/FET.

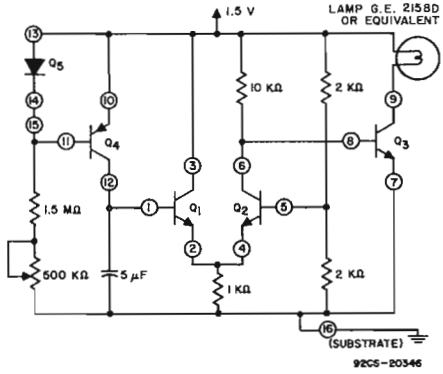
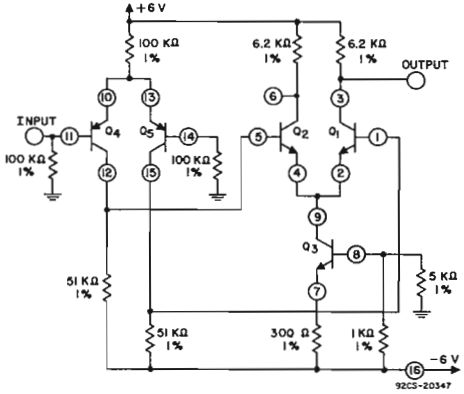


Fig.36b—Ten-second timer operated from 1.5-volt supply using CA3096E.



Features:

1. Can be operated with either dual supply or single supply.
2. Wide-input common-mode range +5 V to −5 V
3. Low bias current: <1 μA.

Fig.37a—Cascade of differential amplifiers using CA3096AE.

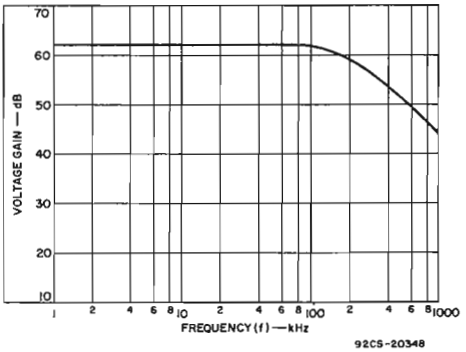


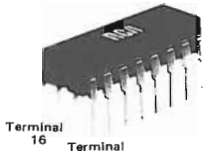
Fig.37b—Gain-frequency characteristics.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3097E



16-Lead Dual-In-Line Plastic Package

Thyristor/Transistor Array

For Military, Commercial, and Industrial Applications

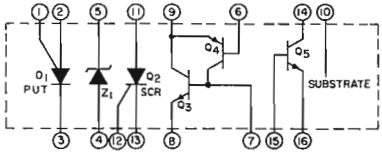
Includes:

- Uncommitted n-p-n Transistor
- Sensitive-Gate Silicon Controlled Rectifier
- Programmable Unijunction Transistor (PUT)
- p-n-p/n-p-n Transistor Pair
- Zener Diode
- Separate Substrate Connection

RCA-CA3097E* Thyristor/Transistor Array is a monolithic integrated circuit that enables circuit designers to further integrate control systems. The CA3097E consists of five independent and completely isolated elements on one chip: an n-p-n transistor, a p-n-p/n-p-n transistor pair, a zener diode, a programmable unijunction transistor (PUT), and a sensitive-gate silicon controlled rectifier (SCR).

The CA3097 is supplied in either the 16-lead dual-in-line plastic package ("E" suffix) or the chip version ("H" suffix), and operates over the full military-temperature range of −55 to +125°C.

*Formerly Dev. No. TA6281



92CS-21935

Fig. 1 — Schematic diagram of CA3097E.

Features:

- Complete isolation between elements
- n-p-n transistor — V_{CEO} = 30 V (min.) I_C = 100 mA (max.)
- p-n-p/n-p-n transistor pair — beta ≥ 8000 (typ.) @ I_C = 10 mA, individual p-n-p, n-p-n, or transistor pair operation
- Programmable unijunction transistor (PUT) — peak-point current = 15 nA (typ.) at R_G = 1 MΩ; V_{AK} = ±30 V
- (PUT) Extremely long RC time constants with low value of external capacitor
- Sensitive-gate silicon controlled rectifier (SCR) — 150 mA forward current (max.)
- Zener-diode impedance (Z_Z) = 15Ω (typ.) at 10 mA

Applications:

- Timers
- Light dimmers/motor controls
- Oscillators
- "One-shot" multivibrators
- Voltage regulators
- Comparators, Schmitt triggers
- Constant-current sources
- Amplifiers
- Logic circuits
- SCR triggering
- Pulse Circuits

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

Isolation Voltage, any terminal to substrate*	+50 V
Dissipation, Total Package:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/^oC
Ambient Temperature Range:	
Operating	−55 to +125^oC
Storage	−65 to +150^oC
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 ^oC
Each n-p-n Transistor (Q3,Q5)	
The following ratings apply with terminals 6 & 9 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	30 V
Collector-to-Base Voltage (V_{CBO})	50 V
Emitter-to-Base Voltage (V_{EBO})	5 V
Collector Current (I_C)	100 mA
Base Current (I_B)	20 mA
Dissipation (P_D)	500 mW
p-n-p Transistor (Q4)	
The following ratings apply with terminals 7 & 8 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	−40 V
Collector-to-Base Voltage (V_{CBO})	−50 V
Emitter-to-Base Voltage (V_{EBO})	−40 V
Collector Current (I_C)	−10 mA
Base Current (I_B)	−3 mA
Dissipation (P_D)	200 mW
p-n-p/n-p-n Transistor Pair (Q3,Q4)	
Dissipation (P_D)	500 mW
Programmable Unijunction Transistor, PUT (Q1)	
Gate-to-Cathode Positive Voltage (V_{GK})	30 V
Gate-to-Cathode Negative Voltage (V_{GKR})	5 V
Gate-to-Anode Negative Voltage (V_{GA})	30 V
Anode-to-Cathode Voltage (V_{AK})	±30 V
DC Anode Current	150 mA
Peak Anode Non-Recurrent Forward (On-State) Current (10 μs pulse)	2 A
Total Average Dissipation	300 mW
Silicon Controlled Rectifier, SCR (Q2)	
Repetitive Peak Reverse Voltage (V_{RRXM}), R_{GK} = 1 KΩ	30 V
Repetitive Peak Off-State Voltage (V_{DRXM}), R_{GK} = 1 kΩ	30 V
DC On-State Current (I_{TDC})	150 mA
Peak Surge (Non-Repetitive) On-State Current (10 μs pulse)	2 A
Forward Peak Gate Current (I_{GFM})	20 mA
Peak Gate-to-Cathode Reverse Voltage (V_{GRM})	5 V
Total Average Dissipation	300 mW
Zener Diode, (Z1)	
DC Current (I_Z)	25 mA
Dissipation (P_D)	250 mW

* One or more of the terminals of each element of the CA3097E is isolated from the substrate by a junction diode. In order to maintain electrical isolation between elements, the substrate terminal must be connected to a voltage which is no more positive than that of any other terminal. To avoid undesirable coupling between elements, the substrate terminal (terminal 10) should be maintained at either dc or signal (ac) ground.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
n-p-n TRANSISTORS Q3, Q5 (TERMINALS 6 and 9 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = 100μA, I_B = 0		30	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0		50	–	–	V
COLLECTOR-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0		50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = 100μA, I_C = 0		5	7.5	10	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE(SAT)}$	I_C = 50mA, I_B = 5mA	5	–	–	0.65	V
		I_C = 10mA, I_B = 1 mA		–	0.10	–	
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE(SAT)}$	I_C = 10mA, I_B = 1mA	2	–	0.76	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.73	0.85	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = 3V, I_C = 10mA	4	100	130	–	
		V_{CE} = 3V, I_C = 50mA		80	120	–	
p-n-p TRANSISTOR Q4 (TERMINALS 7 and 8 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = -10 V, I_E = 0		–	–	–1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = -10 V, I_B = 0		–	–	–10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = -100μA, I_B = 0		–40	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = -10μA, I_E = 0		–50	–	–	V
EMITTER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)EIO}$	I_{EI} = 10μA, I_B = 0, I_E = 0		–50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = –10μA, I_C = 0		–40	–	–	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE(SAT)}$	I_C = -1mA, I_B = -100μA	6	–	–	–0.33	V
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE(SAT)}$	I_C = -1mA, I_B = –100μA-	7	–	–0.7	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = -3 V, I_C = –100μA	8	–0.5	–0.6	–0.7	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = – 3 V, I_C = –100μA	9	30	60	–	
		V_{CE} = –3 V, I_C = –1 mA		40	–	–	
n-p-n/p-n-p TRANSISTOR PAIR Q3, Q4							
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} (n-p-n) = 3V, I_C = 10mA	10	–	8000	–	
		V_{CE} (n-p-n) = 3V, I_C = 50mA	10	–	6500	–	

ELECTRICAL CHARACTERISTICS (Cont'd.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT), Q1							
OFFSET VOLTAGE	V_T*	V_S = 10V, R_G = 10kΩ	11,22[a]	0.2	–	0.7	V
		V_S = 10V, R_G = 1MΩ		0.2	–	0.7	
ANODE-TO-CATHODE ON-STATE VOLTAGE	V_F	I_F = 50mA	12	–	0.90	1.5	V
		I_F = 100mA		–	1	–	
PEAK OUTPUT VOLTAGE	V_{OM}	C = 0.22μF Anode Supply Voltage = 20V	13,23	–	10	–	V
PEAK-POINT CURRENT	I_P	V_S = 10V, R_G = 10kΩ	14,22[a]	–	0.55	1	μA
		V_S = 10V, R_G = 1MΩ	–	–	0.015	0.15	
VALLEY-POINT CURRENT	I_V	V_S = 10V, R_G = 10kΩ	17,15	4	40	–	μA
		V_S = 10V, R_G = 1MΩ	16	–	–	25	
GATE REVERSE CURRENT	I_{GAO}	V_S = 30V	22[c]	–	0.02	–	nA
GATE REVERSE CURRENT	I_{GKS}	Anode-To-Cathode Short, V_S = 30V	22[d]	–	0.2	–	nA
OUTPUT PULSE RISETIME	t_r	Anode-Supply Voltage = 20V C = 0.22 μF	23	–	60	–	ns
SILICON CONTROLLED RECTIFIER (SCR), Q2							
PEAK OFF-STATE CURRENT: FORWARD	I_{DXM}	V_{DRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	μA
REVERSE	I_{RXM}	V_{RRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	
FORWARD DC VOLTAGE DROP	V_T	I_T = 50 mA	18	–	0.90	1.5	V
GATE-TO-SOURCE TRIGGER CURRENT	I_{GS}	T_A = 25°C	26	–	33	100	μA
		T_A = −55°C	26	–	50	–	
DC GATE-TRIGGER VOLTAGE	V_{GT}	V_L = 10V, R_L = 100Ω	19	–	0.55	0.75	V
HOLDING CURRENT	I_{HO}	R_{GK} = 1kΩ	20,24	–	1.2	–	mA
CRITICAL RATE-OF-RISE OF OFF-STATE VOLTAGE	dv/dt	EXPONENTIAL RISE, R_{GK} = 1kΩ, V_{DRXM} = 30V	25	–	150	–	V/μs
GATE-CONTROLLED TURN-ON TIME	t_{gt}	See Fig. 33	33	–	50	–	ns
CIRCUIT-COMMUTATED TURN-OFF TIME	t_q	See Fig. 33	33	–	10	–	μs
ZENER DIODE, Z1							
ZENER VOLTAGE	V_Z	I_Z = 10mA	21	7.2	8	8.8	V
ZENER IMPEDANCE	Z_Z	I_Z = 10mA, f = 1kHz		–	15	25	Ω
ZENER VOLTAGE TEMPERATURE COEFFICIENT	$(\Delta V_Z/V_Z)/\Delta T$	I_Z = 10mA		–	+0.05	–	%/°C
	$\Delta V_Z/\Delta T$			–	+4	–	mV/°C
ZENER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)ZIO}$	I_Z = 100μA TERM. 5 TO SUBSTRATE		50	80	– –	V

* $V_T = V_P - V_S$ (Fig. 22)

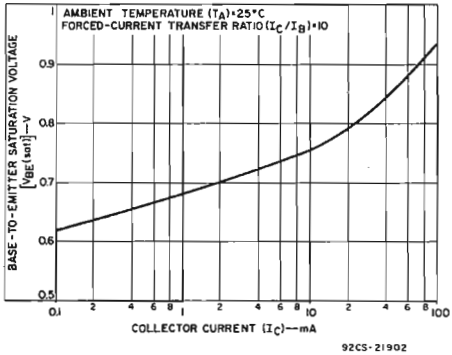


Fig.2 – Base-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

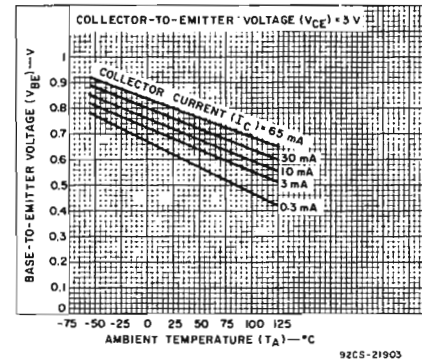


Fig.3 – Base-to-emitter voltage vs. ambient temperature for n-p-n transistors Q3 & Q5.

TYPICAL CHARACTERISTICS

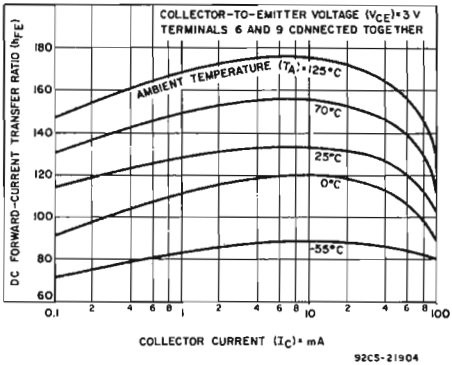


Fig.4 – DC forward-current transfer ratio vs. collector current for n-p-n transistors Q3 & Q5.

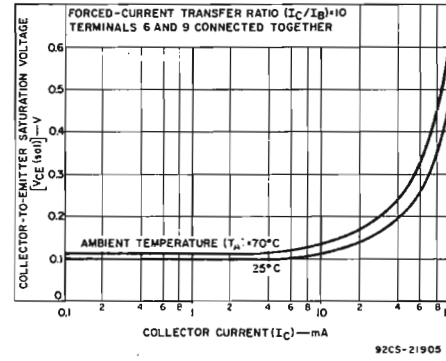


Fig.5 – Collector-to-emitter saturation voltage vs. collector for n-pn- transistors Q3 & Q5.

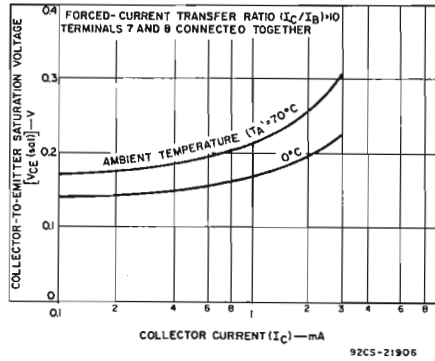


Fig.6 – Collector-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

TYPICAL CHARACTERISTICS (CONT'D)

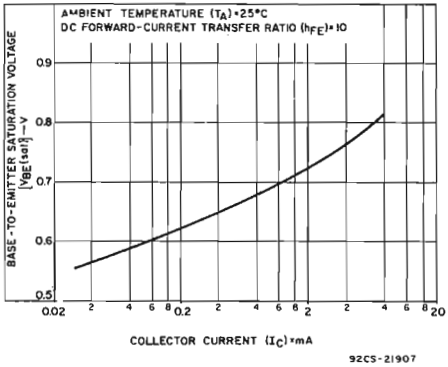


Fig.7 – Base-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

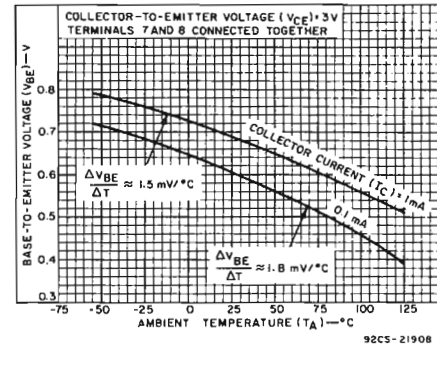


Fig.8 – Base-to-emitter voltage vs. ambient temperature for p-n-p transistor Q4.

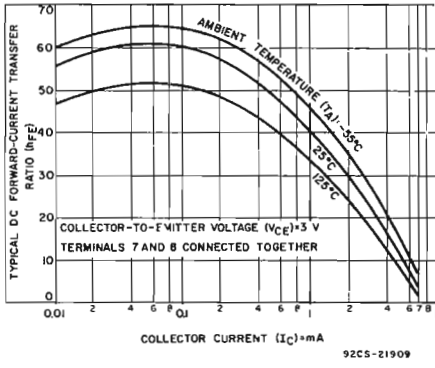


Fig.9 – DC forward-current transfer ratio vs. collector current for p-n-p transistor Q4.

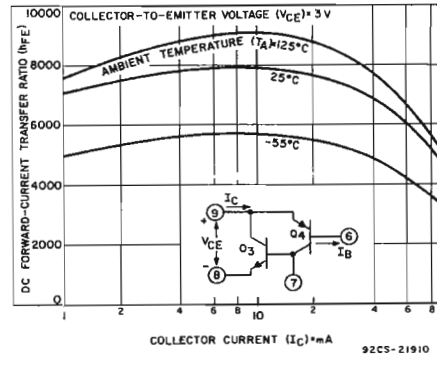


Fig.10 – DC forward-current transfer ratio vs. collector current for transistor pair Q3, Q4.

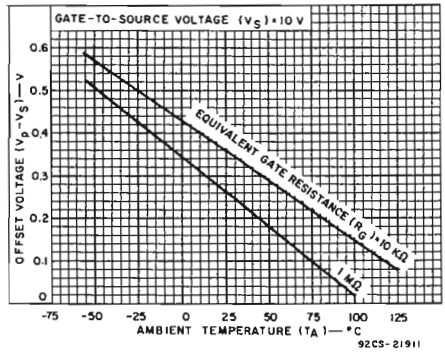


Fig.11 – Offset voltage vs. ambient temperature for Q1 (PUT).

TYPICAL CHARACTERISTICS (CONT'D)

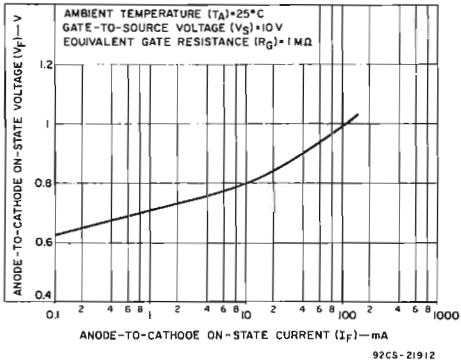


Fig.12 – Anode-to-cathode on-state voltage vs. anode-to-cathode on-state current for Q1 (PUT).

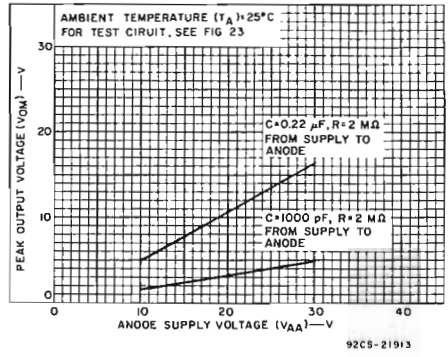


Fig.13 – Peak output voltage vs. anode supply voltage for Q1 (PUT).

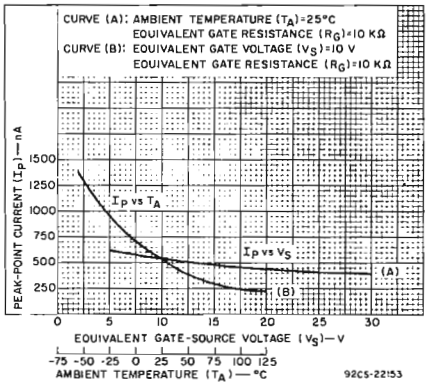


Fig.14 – Peak-point current vs. gate-source voltage and ambient temperature for Q1 (PUT).

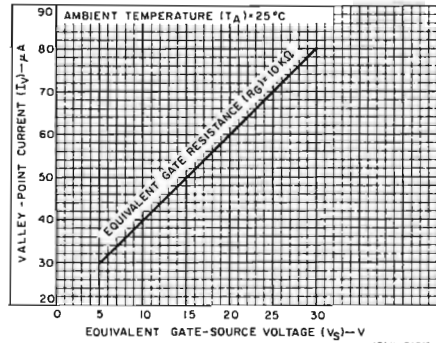


Fig.15 – Velley-point current vs. gate-source voltage for Q1 (PUT).

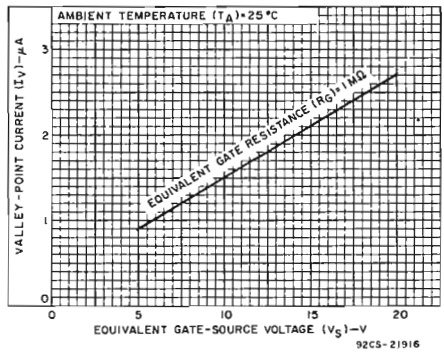


Fig.16 – Valley-point current vs. gate-source voltage for Q1 (PUT).

TYPICAL CHARACTERISTICS (CONT'D)

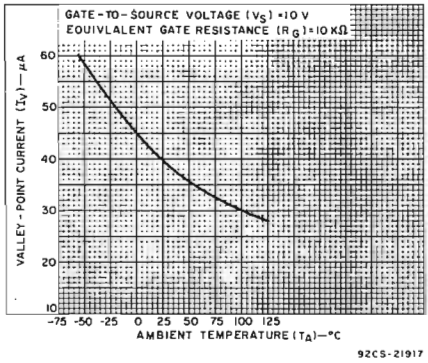


Fig.17 — Valley-point current vs. ambient temperature for Q1 (PUT).

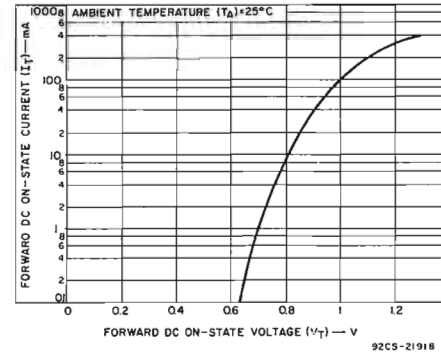


Fig.18 — Forward DC on-state current vs. on-state voltage for Q2 (SCR).

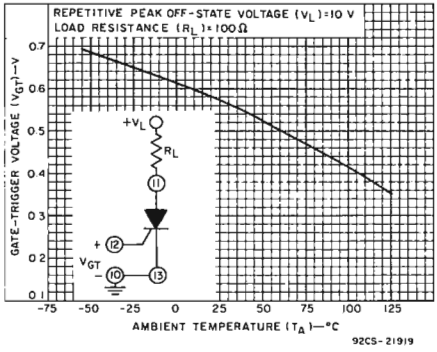


Fig.19 — Gate-trigger voltage vs. ambient temperature for Q2 (SCR).

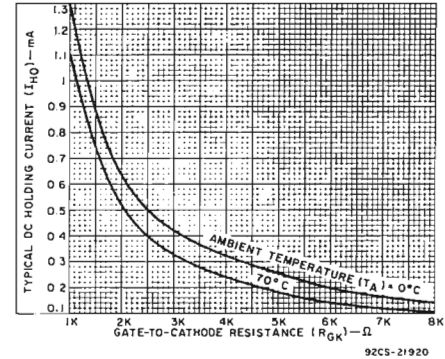


Fig.20 — Typical DC holding current vs. gate-to-cathode resistance for Q2 (SCR).

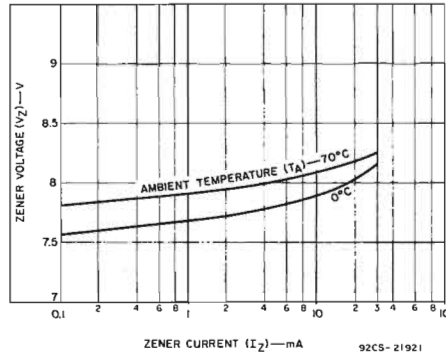


Fig.21 — Zener voltage vs. zener current for Z1.

OPERATING CONSIDERATIONS FOR CA3097E

1. Composite p-n-p/n-p-n Transistors Q3, Q4 (See Fig. 3)

To use Q3 as an individual n-p-n transistor, join terminals no. 6 and no. 9 to disable p-n-p transistor Q4.

The appropriate terminal connections are then:

Collector..... terminal 9
Base ..... terminal 7
Emitter..... terminal 8

To use Q4 as an individual p-n-p transistor, join terminals no. 7 and no. 8 to disable n-p-n transistor Q3.

The appropriate terminal connections are then:

Collector..... terminal 7
Base ..... terminal 6
Emitter..... terminal 9

To use Q3 and Q4 as a composite use terminals 6, 7, 8, and 9 as required.

2. Programmable Unijunction Transistor Q1 (PUT)

The programmable unijunction transistor is essentially an anode-gate SCR. The volt-ampere characteristic of the device is shown in Fig. 22. When an equivalent Thevenin source (V_S, R_G), as shown in Fig. 22, is applied to the gate terminal the device will be "off" if the anode-voltage is negative with respect to the gate voltage. Under this condition, any current flow is exclusively leakage current. When the anode voltage becomes more positive than the gate voltage by an increment equal to the threshold voltage (V_T = 0.4 V typ.), the device can turn "on" only if the current available at the anode terminal is greater than the specified peak-point current. The PUT will then switch through its negative-resistance region to the "on" state (low anode-to-gate voltage). It should be noted that I_P is not the maximum current allowed through the device, but is the current required at the peak of the V-I curve. I_P is typically a very low value of current.

After the PUT has switched to its low-impedance state, the device will remain "on" if the anode-current (I_A) exceeds the valley-point current (I_V). If $I_A < I_V$, the PUT will switch back to its high-impedance "off" state. Thus, the PUT can be made to "latch" or recover, depending on I_V. Since I_V is a function of the "on"-state gate current (which depends on R_G and V_S) a choice of R_G and/or V_S will determine the operating mode, i.e., "off" state→"on" state or "off" state → "on" state → "off" state. The value of I_V increases directly as a function of V_G and inversely with R_G. The PUT in the CA3097E has a low I_P.....I_P = 15 nA at V_S = 10 V, R_G = 1 MΩ. This low value of I_P indicates that an extremely large value of anode-supply resistor, e.g. 60 MΩ (typ.), can be used in timing circuits requiring long RC time constants. This becomes important when considering the size of the external

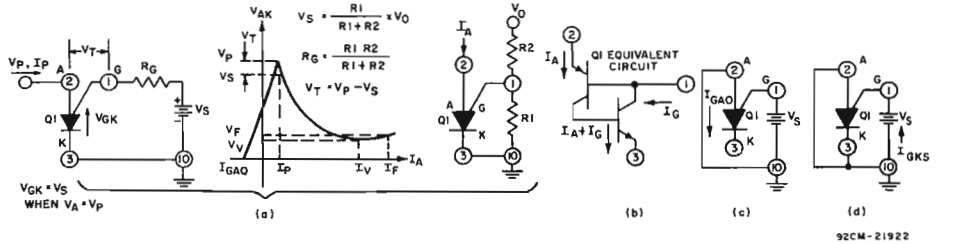


Fig. 22 – General anode characteristics for Q1 (PUT).

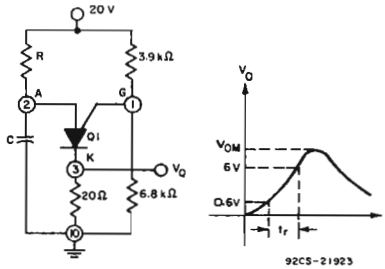


Fig. 23 – Output pulse characteristics for Q1 (PUT).

OPERATING CONSIDERATIONS (CONT'D)

timing capacitor to be used. Consequently, the use of the PUT in the CA3097E is advantageous since it has a lower I_P than most discrete PUT's.

Temperature Compensation of Switching Point

As described previously, the PUT will switch to its low-impedance state when its anode voltage is approximately a diode-drop above the gate voltage. Since the anode-to-gate threshold voltage vs. temperature characteristic is similar to that of a typical silicon-diode junction, a compensating series diode such as used in the circuit of Fig. 29 (Z1 connected as forward-biased diode) considerably reduces the effect of temperature on the switching point.

Bypassing Anode Current

If the PUT gate equivalent source is such that $I_A > I_V$, the PUT will remain "on". A method for turning the PUT off is by shunting current away from the anode until $I_A < I_V$. An example of this technique is the oscillator circuit of Fig. 29. Q3 transistor is turned "on" after the PUT fires and shunts current away from the anode, thereby forcing $I_A < I_V$. The PUT then turns "off" allowing C_T to recharge through R_T, to repeat the cycle.

Protecting The PUT Against Discharge Current Of The Capacitor

A current-limiting resistor in series with the PUT is normally required to dissipate capacitive discharge energy (see Figs. 23 and 29).

Silicon Controlled Rectifier, Q2 (SCR)

The SCR should be used with a 1 kΩ (or less) resistor connected between the cathode and gate terminals if the SCR is to be subjected to its maximum forward and reverse voltage ratings (V_{DXM} and V_{RXM}). Selecting a value for R_{GK} of 1 kΩ (or lower) increases the capability of the device to withstand greater dv/dt and increases the noise immunity of the SCR against false triggering at the gate. Practical considerations such as available current drive from the triggering devices (e.g., a PUT) will determine the lowest value of R_{GK} at which the SCR will fire with a $V_{GK} \approx 0.55$ V. With a value of 500Ω for R_{GK}, the trigger source must be capable of supplying 1.1 mA. R_{GK} should be non-inductive within the frequency band of the noise transients normally encountered in a particular application.

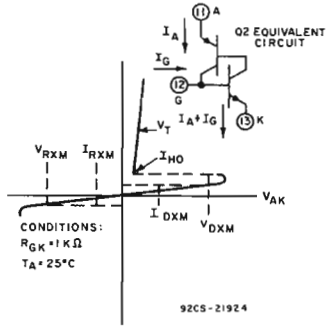


Fig. 24 – Principle voltage-current characteristics for Q2 (SCR).

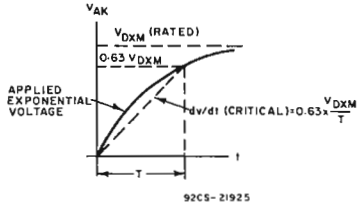


Fig. 25 – Definition of critical rate of rise of off-state voltage for Q2 (SCR).

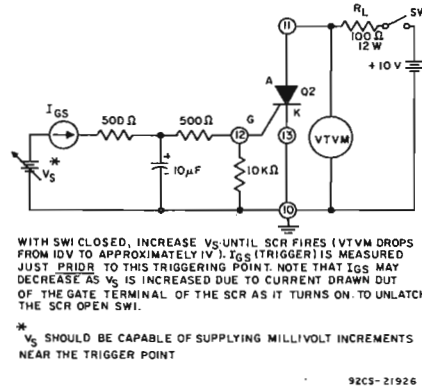
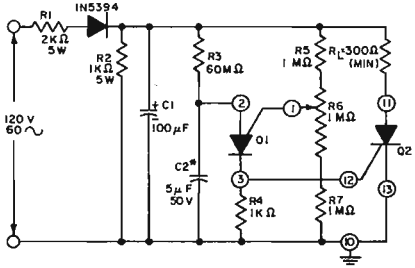


Fig. 26 – Test circuit for determining I_{GS} in Q2 (SCR).

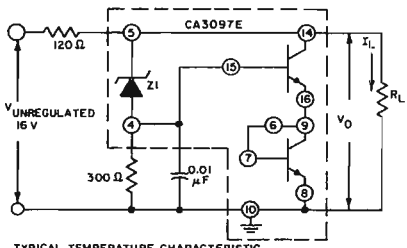
APPLICATIONS CIRCUITS



TIMING PERIOD ≈ 200 SEC. WITH 1 MΩ POT CENTERED
TIMING CYCLE BEGINS WHEN AC IS APPLIED
* SPRAGUE TYPE 4308, 5 μF AT 50 V
SPRAGUE TYPE 6308, 5μF AT 50 V
OR EQUIVALENT

92CS-21927

Fig. 27 — AC line-operated one-shot timer.



TYPICAL TEMPERATURE CHARACTERISTIC

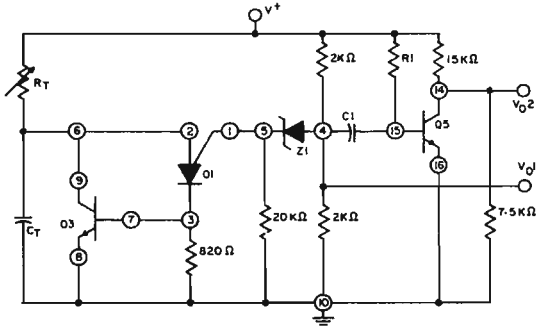
@ R_L = 330Ω $\frac{\Delta V_O/V_O}{\Delta T}$ × 100 = ±0.01 %/°C

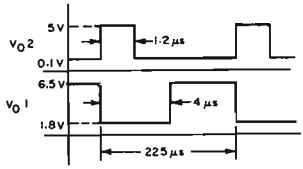
92CS-21928

TYP. LOAD REGULATION @ I_L = 0 TO 40 mA, ($\Delta V_O/V_O$) × 100 = −3 % (NO LOAD TO FULL LOAD)

TYP. LINE REGULATION @ R_L = 330Ω, $\frac{\Delta V_O/V_O}{\Delta V_{UNREG.}}$ × 100 = ±0.55%/V

Fig. 28 — Temperature-compensated shunt regulator.





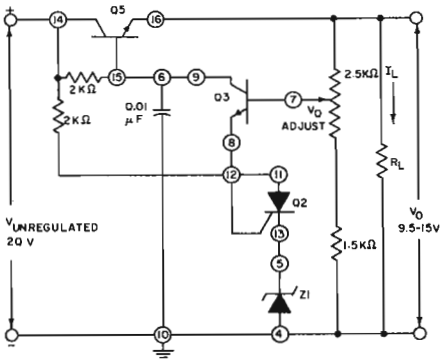
PULSE RATE ADJUSTED BY VARYING R_T OR C_T.
OUTPUT PULSE WIDTH ADJUSTED BY R_1C_1 DIFFERENTIATING TIME CONSTANT

TYPICAL OPERATION FOR:
V^+ = 15 V, C_T = 0.1 μF, R_T = 4.3KΩ
C_1 = 82 pF, R_1 = 60KΩ

92CM-21929

Fig. 29 — Pulse generator.

APPLICATIONS CIRCUITS



TYPICAL LOAD REGULATION @ V_O = 12 V, I_L = 0 TO 40 mA

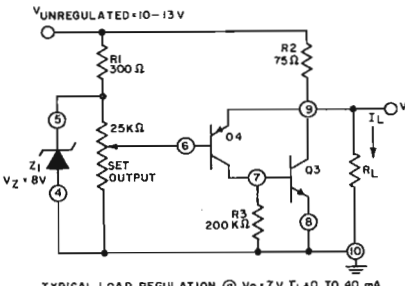
$$\frac{\Delta V_O}{V_O} \times 100 = \pm 0.4\ \%$$ (NO LOAD TO FULL LOAD)

TYPICAL LINE REGULATION @ V_O = 12 V

$$\frac{\Delta V_O / V_O}{\Delta V_{UNREG.}} \times 100 = \pm 0.45\ \%/V$$

92CS-21930

Fig. 30 – Series voltage regulator.



TYPICAL LOAD REGULATION @ V_O = 7 V, I_L = 0 TO 40 mA

$$\frac{\Delta V_O}{V_O} \times 100 = -1.1\ \%$$

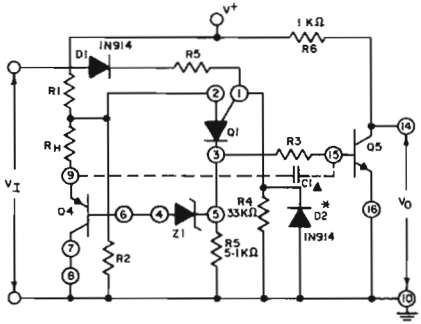
TYPICAL LINE REGULATION @ V_O = 7 V, I_L = 20 mA

$$\frac{\Delta V_O}{V_O} = \pm 0.85\ \%/VOLT$$

$$\Delta V_{UNREGULATED}$$

92CS-21931

Fig. 31 – 5 to 7.5 V shunt regulator.



▲ OPTIONAL SPEED-UP CAPACITOR

* REQUIRED IF V_I SWINGS BELOW GROUND

TYPICAL OPERATING CONDITIONS:

FREQUENCY IN = 0-10 KHz

SUPPLY VOLTAGE (V^+) = 15 V

R1, R2, R_H = 5.1 KΩ

R3 = 6.2 KΩ, R_S = 300 Ω

CI = 820 pF

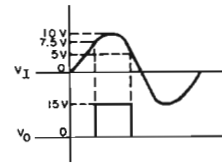
$V_{TH}U$ = 7.5 V, $V_{TH}L$ = 5 V

HYSTERESIS VOLTAGE = 2.5 V

UPPER THRESHOLD VOLTAGE $(V_{TH}U) \approx V^+ \frac{R2}{R1+R2}$

LOWER THRESHOLD VOLTAGE $(V_{TH}L) \approx \frac{(V^+)\left(\frac{R2\,R_H}{R2+R_H}\right)}{\frac{R2\,R_H}{R2+R_H} + R1}$

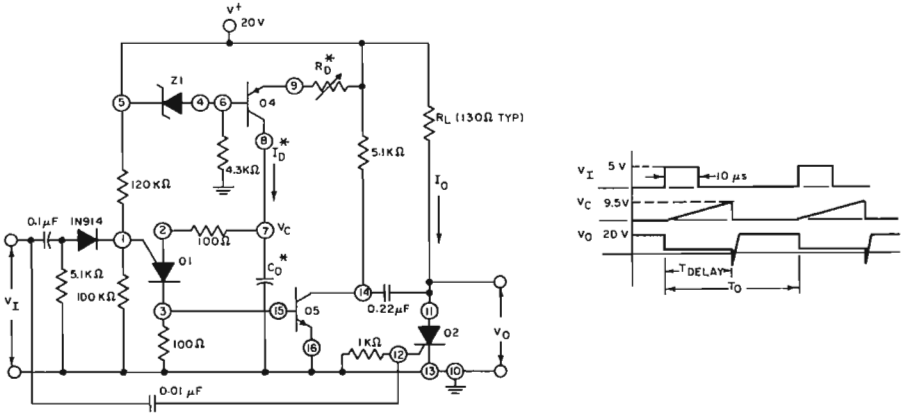
HYSTERESIS VOLTAGE = $V_{TH}U - V_{TH}L$



92CM-21932

Fig. 32 – Schmitt trigger.

APPLICATIONS CIRCUITS (CONT'D)

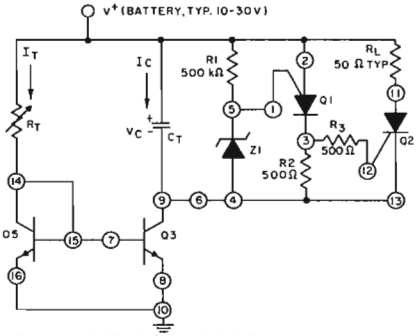


*MONOSTABLE DELAY TIME SET BY ADJUSTMENT OF I_D (VARY R_D) OR BY C_D. I_D MUST BE GREATER THAN I_V OF Q1 (PUT) FOR MONOSTABLE OPERATION.

Q2 (SCR) SWITCHING TIMES:
GATE-CONTROLLED TURN-ON TIME (t_{gt}) = 50 ns (TYP)
CIRCUIT-COMMUTATED TURN-OFF TIME (t_q) = 10 μs (TYP)

92CM-21933

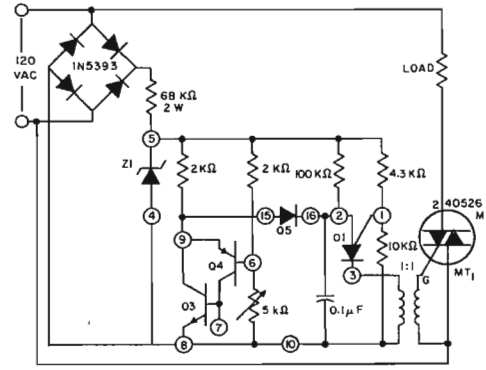
Fig. 33 — Monostable multivibrator with variable delay.



T_{OFF} = TIMING PERIOD (NO LOAD CURRENT)
PUT FIRES WHEN $V_C \approx 8$ V
$V_C = \frac{I_C (T_{OFF})}{C_T}$, $I_C \approx I_T$ (Q3, Q5 MATCHED)
I_T SET BY ADJUSTING R_T, $I_T \approx \frac{V^+ - 0.7}{R_T}$
T_{ON} = CAPACITOR DISCHARGE TIME THROUGH LOAD. LOAD TURNS OFF WHEN SCR ANODE CURRENT FALLS BELOW HOLDING CURRENT (I_{HO}). TYPICAL I_{HO} = 1.2 mA
EXAMPLE: FOR TIMING PERIOD OF 8.3 MIN
C_T = 1000 μF, I_T = 16 μA
$R_T = \frac{V^+ - 0.7}{I_T}$ (FOR V^+ = 16 V, $R_T \approx$ 1 MΩ)

92CS-21934

Fig.34 — Low-current-drain battery-operated long interval astable timer.



NOTE: SHORT TERMINAL 15 TO 14 WHEN USING Q5 AS A DIODE

92CS-22178

Fig.35 — Phase control circuit.

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA3099E

14-Lead Dual-in-Line
Plastic Package H-1517

Programmable Comparator - - With Memory

Features:

- Programmable operating current
- Micro-power standby dissipation
- Directly controls current up to 150 mA
- Low input on/off current of less than 1 nA for programmable bias current of 1 μA
- Built-in hysteresis: 10 mV max.
- Programmable hysteresis: 10 mV to V+
- Dual reference input
- High sensor range: 100 Ω to 100 MΩ
- Stable predictable switching levels
- Temperature-compensated reference voltage

Applications:

- Control of relays, heaters, LED's, lamps, photo-sensitive devices, thyristors, solenoids, etc.
- Signal reconditioning
- Phase and frequency modulators
- On/off motor switching
- Schmitt triggers, level detectors
- Time delays
- Overvoltage, overcurrent, overtemperature protection
- Battery-operated equipment
- Square and triangular-wave generators

RCA-CA3099E* Programmable Comparator is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3099E can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with a maximum operating voltage of ± 8 volts. It can directly control currents up to 150 mA. It operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3099E contains the following six (6) major circuit-function features (Figure 1):

1. **Differential amplifiers and summer;** the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.

* Formerly Developmental No. TA6189.

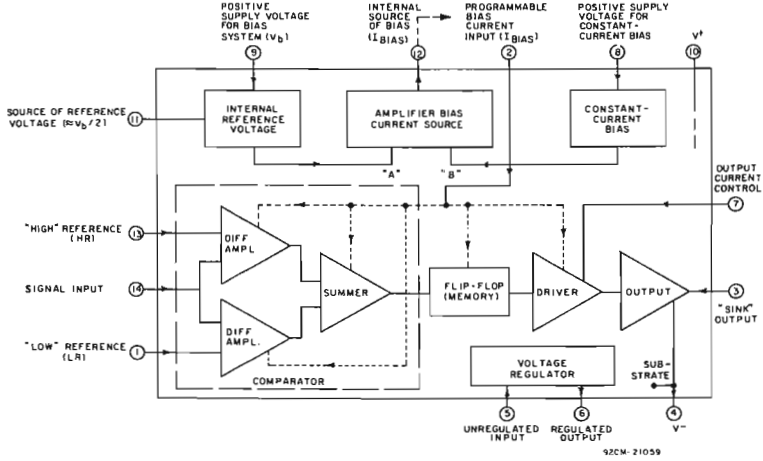


Fig. 1—Block diagram of CA3099E programmable comparator.
(See page 3 for general description of circuit operation.)

Major Circuit-Function Features (Cont'd)

2. **Flip-flop;** the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. **Driver and output stages;** these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. **Programmable operating current;** the circuit incorporates a separate terminal to permit programming the desired quiescent operating current and performance parameters.
5. **Internal sources of reference voltage and programmable bias current;** an integral circuit supplies a temperature-compensated reference voltage ($V_b/2$) which is about 1/2 of the externally applied bias voltage (V_b). Additionally, integral circuitry can optionally be used to supply an uncompensated constant-current source of bias (I_{bias}).
6. **Voltage regulator;** provides optional on-chip voltage regulation when power for the CA3099E is provided by an unregulated supply.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

Supply Voltage Between Terminals 10 and 4, 9 and 4, 8 and 4	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 14 and 1, and Terminals 13 and 14	10	V
Operating Voltage Range:		
Term. 14	0 V to V^+	
Term. 13	2.0 V to V^+	
Term. 1	0 V to V^+ minus 2.0 V	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programming Bias Current (Term. 2)	1	mA
Output Current Control (Term. 7)	15	mA
Power Dissipation:		
Up to T_A = 55°C	750	mW
Above T_A = 55°C, Derate Linearly at	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Termperature (During Soldering): At distance not less than 1/32 inch (0.79 mm) from seating plane for 10 s maximum	+265	°C

ELECTRICAL CHARACTERISTICS AT T_A = 25°C *(Unless otherwise indicated)*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C Unless Otherwise Indicated	FIG. No.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Reference Voltage	V_{REF}	Term. 9 = 12 V, Term.4 = Grd, Term.11 = Test	–	5.7	6	6.3	V
Reference Voltage Temperature Coefficient			–	–	100	–	μV/°C
Regulated Supply Voltage	V_{REG}	Term.5 1K to 12V, Term.4 = Grd, Term.6 10K to Grd	5	6	7.2	8	V
Regulated Supply Voltage Temperature Coefficient			5	–	2.9	–	mV/°C
Input Offset Voltage: "Low" Reference	V_{IO} (LR)	V_{LR} = Grd, V_{HR} = 3 V, I_{BIAS} = 100 μA	20, 6	−8	−3	2	mV
"High" Reference	V_{IO} (HR)	V_{HR} = Grd, V_{LR} = −3 V, I_{BIAS} = 100 μA	20, 7	−5	±1	5	
"Low" Reference Temp. Coefficient		−55°C to +125°C	20, 8	–	4.5	20	μV/°C
"High" Reference Temp. Coefficient		−55°C to +125°C	20, 9	–	±8.2	±20	
Min. Hysteresis Voltage	$V_{IO(HR-LR)}$	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21, 10	–	3	10	mV
Min. Hysteresis Voltage Temperature Coefficient		−55°C to +125°C	11	–	6.7	20	μV/°C
Output Saturation Voltage	$V_{CE(SAT)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,12,13	–	0.72	1.2	V
Total Supply Current: I_{TOTAL} "ON"	I_{TOTAL}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	600	710	800	μA
I_{TOTAL} "OFF"		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	420	560	750	
Input Bias Current: $I_{B(p-n-p)}$	I_{IB}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	33	200	nA
$I_{B(n-p-n)}$		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	20	60	
Output Leakage Current	$I_{CE(OFF)}$	Current from Term.3 when Q46 is "OFF"	–	–	–	10	μA
Internal Bias Current	I_{IBC}		18,19	120	200	280	
Switching Times:							
Delay	t_d	I_C = 100 μA, I_{BIAS} = 100 μA, V^+ = 5 V, V_{REG} = 2.5 V	22	–	600	–	ns
Fall	t_f		22	–	50	–	
Rise	t_r		22	–	500	–	
Storage	t_s		22	–	4.5	–	μS

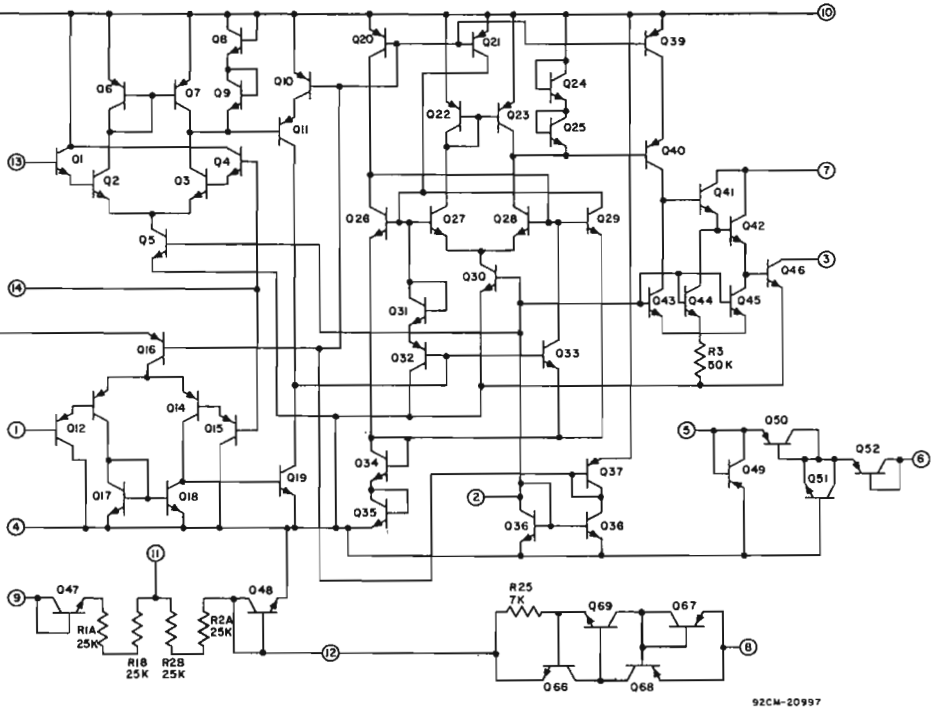


Fig.2—Schematic diagram of CA3099E.

General Description of Circuit Operation (Refer to Fig.1)

When the signal-input voltage of the CA3099E is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3099E comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2. As an alternative to externally supplied bias current, the CA3099E contains an internal source of regulated bias current accessible at terminal 12. This internal source of bias current is developed by two alternative methods; in the first method, bias voltage (V_b) applied at terminal 9 develops a source of temperature-compensated reference voltage ($\approx V_b/2$) at terminal 11 and additionally supplies a source of bias current at terminal 12 via line "A". Alternately, when a positive supply voltage is applied at terminal 8, a source of constant-current biasing is provided at terminal 12 via line "B".

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 7. The CA3099E contains an on-chip voltage regulator which may optionally be used to regulate the voltages and bias currents (exclusive of the load current at terminal 3) needed for the operation of the IC.

Fig. 2 is the schematic diagram of the CA3099E. Figs. 3 and 4 are, respectively, functional and logic diagrams of CA3099E operation.

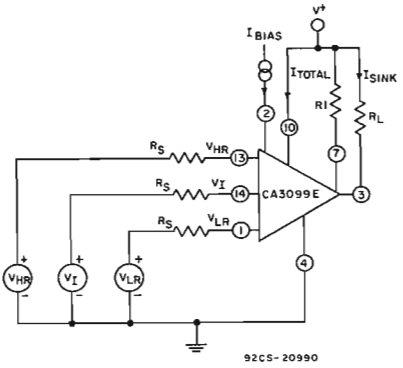


Fig. 3 — Functional diagram.

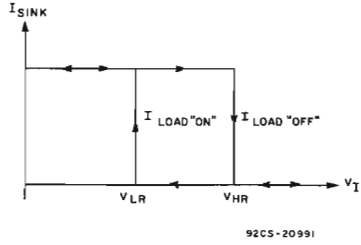


Fig. 4 — Logic diagram.

TYPICAL CHARACTERISTIC CURVES

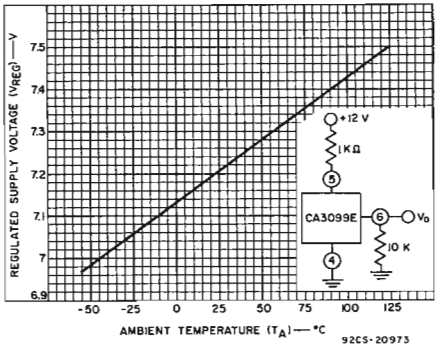


Fig. 5 — Regulated supply voltage vs. ambient temperature.

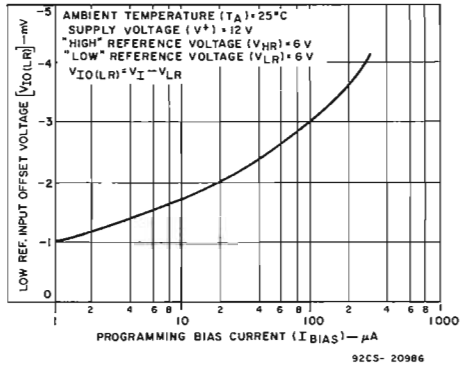


Fig. 6 — Input-offset voltage ("low" reference) vs. programming bias current.

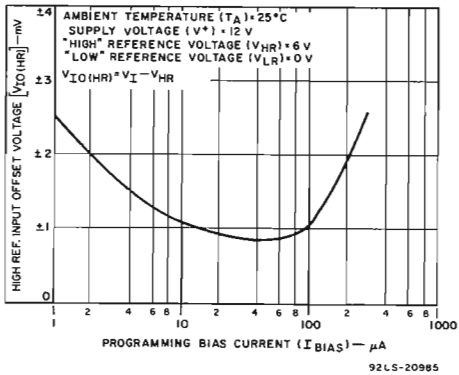


Fig. 7 — Input-offset voltage ("high" reference) vs. programming bias current.

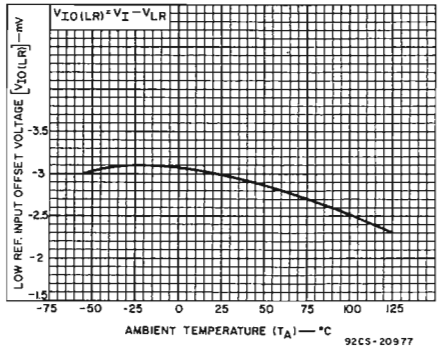


Fig. 8 — Input-offset voltage ("low" reference) vs. ambient temperature.

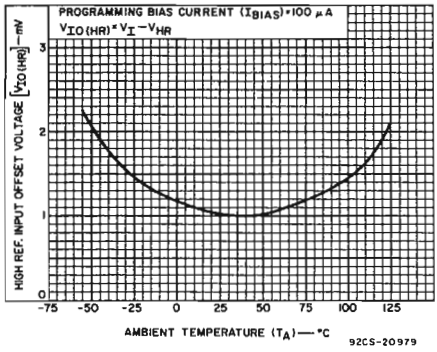


Fig. 9 — Input-offset voltage ("high" reference) vs. ambient temperature.

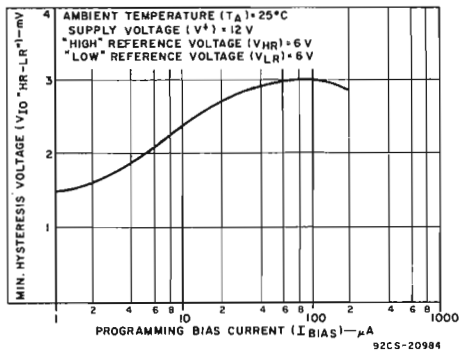


Fig. 10 — Min. hysteresis voltage vs. programming bias current.

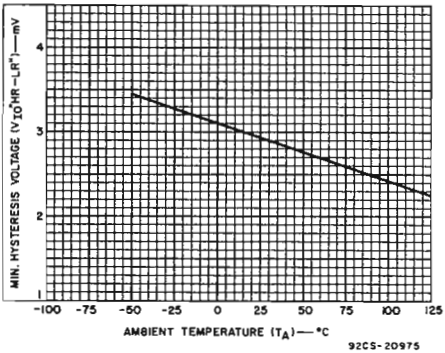


Fig. 11 — Min. hysteresis voltage vs. ambient temperature.

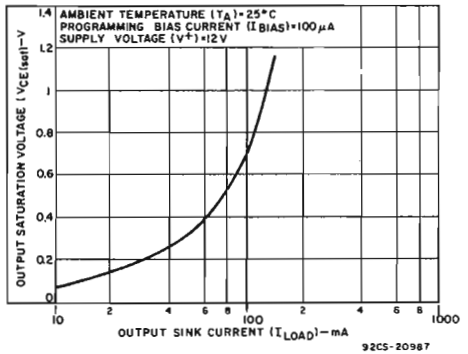


Fig. 12 — Output saturation voltage vs. output sink current.

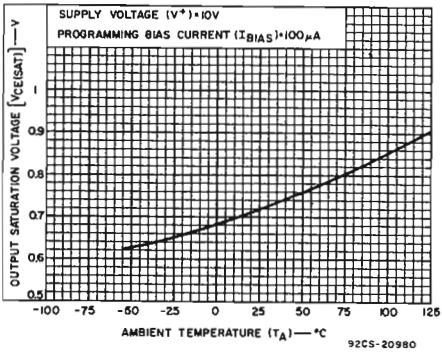


Fig. 13 — Output saturation voltage vs. ambient temperature.

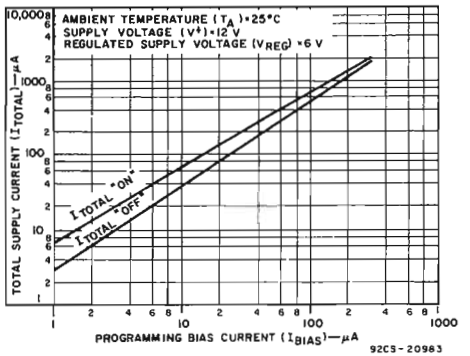


Fig. 14 — Total supply current vs. programming bias current.

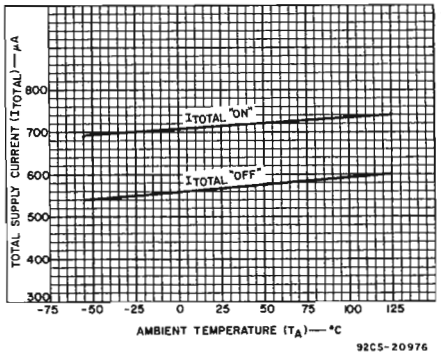


Fig. 15 – Total supply current vs. ambient temperature.

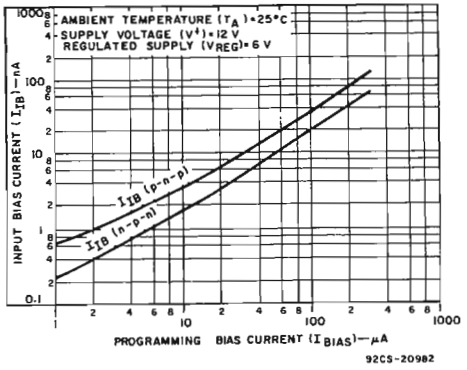


Fig. 16 – Input bias current vs. programming bias current.

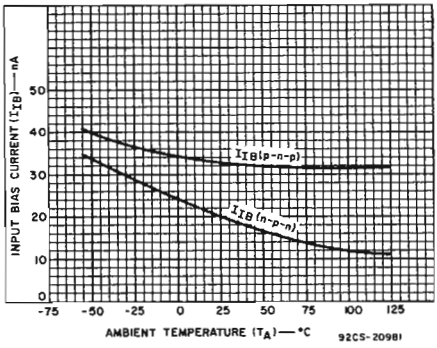


Fig. 17 – Input bias current vs. ambient temperature.

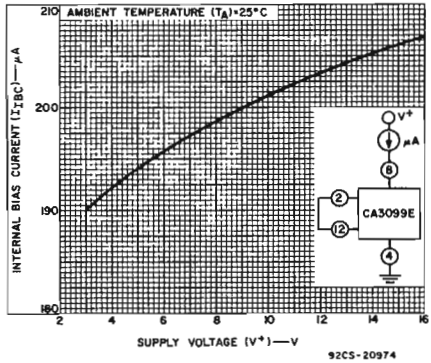


Fig. 18 – Internal bias current vs. supply voltage.

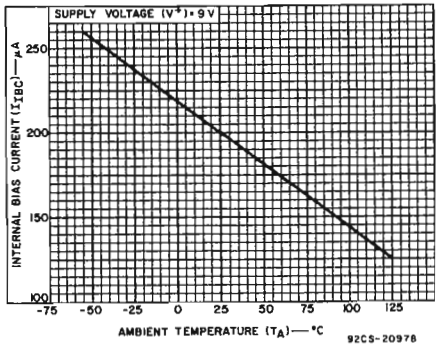


Fig. 19 – Internal bias current vs. ambient temperature.

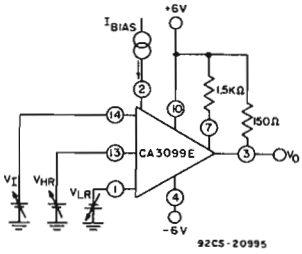


Fig. 20 – Input-offset voltage test circuit.

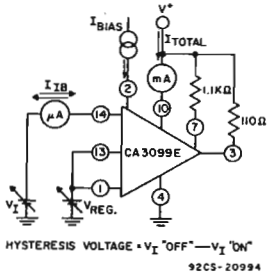
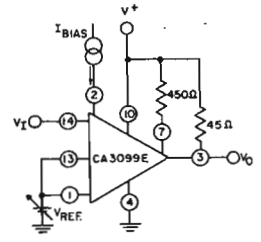


Fig. 21 – Min. hysteresis voltage, total supply current, and input bias current test circuit.



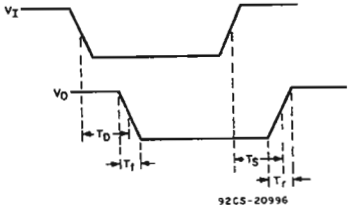


Fig. 22 – Switching time test circuit.

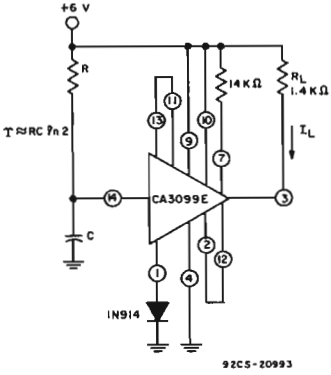


Fig. 23(b) – Time delay circuit: "sink" current interrupted after T seconds.

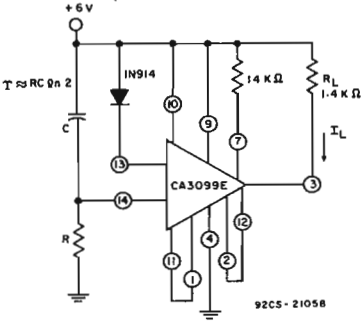
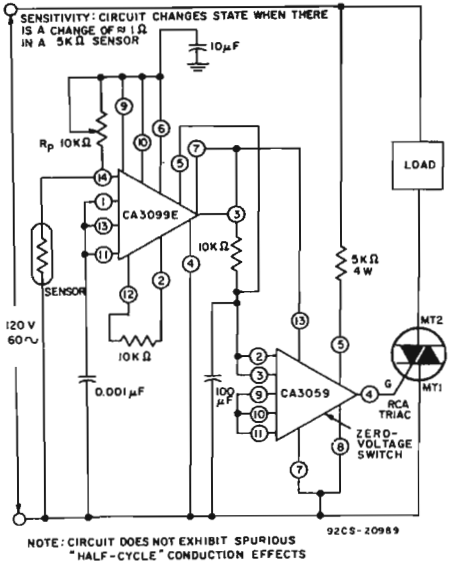


Fig. 23(a) – Time delay circuit: Terminal 3 "sinks" after T seconds.



NOTE: CIRCUIT DOES NOT EXHIBIT SPURIOUS "HALF-CYCLE" CONDUCTION EFFECTS

Fig. 24 – Sensitive temperature control.

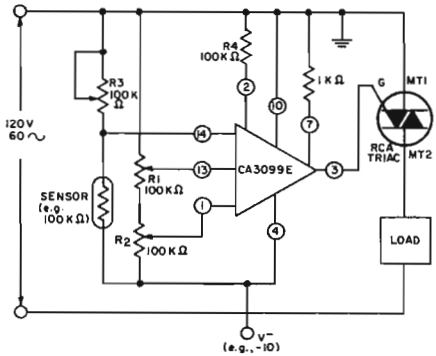


Fig. 25 – OFF/ON control of triac with programmable hysteresis.

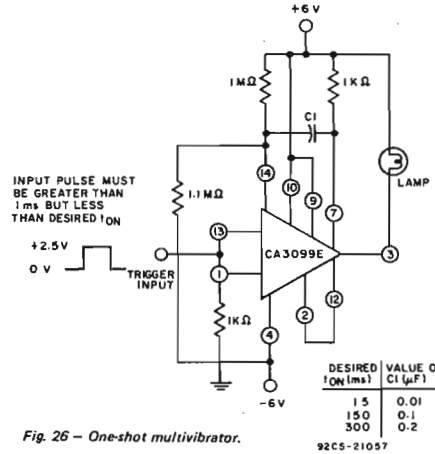


Fig. 26 – One-shot multivibrator.

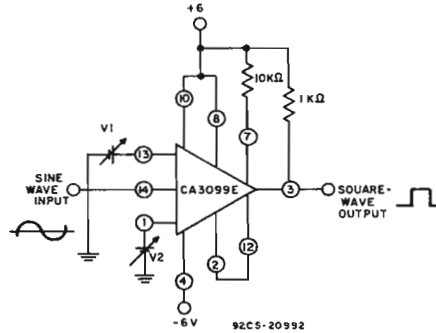


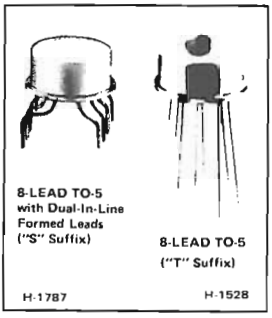
Fig. 27 – Sine-wave to square-wave converter with duty-cycle adjustment (V_1 and V_2).

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

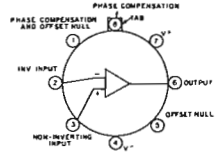
CA3100S CA3100T



Wideband Operational Amplifier

Features:

- High open-loop gain at video frequencies – 42 dB typ. at 1 MHz
- High unity-gain crossover frequency (f_T) – 38 MHz typ.
- Wide power bandwidth – V_O = 18 V p-p typ. at 1.2 MHz
- High slew rate – 70 V/μs (typ.) in 20 dB amplifier
  25 V/μs (typ.) in unity-gain amplifier
- Fast settling time – 0.6 μs typ.
- High output current – ± 15 mA min.
- LM118, 748/LM101 pin compatibility
- Single capacitor compensation
- Offset null terminals



Functional Diagram

RCA-CA3100S, CA3100T* is a large-signal wideband, high-speed operational amplifier which has a unity gain crossover frequency (f_T) of approximately 38 MHz and an open-loop, 3 dB corner frequency of approximately 110 kHz. It can operate at a total supply voltage of from 14 to 36 volts (±7 to ±18 volts when using split supplies) and can provide at least 18 V p-p and 30 mA p-p at the output when operating from ±15 volt supplies. The CA3100 can be compensated with a single external capacitor and has dc offset adjust terminals for those applications requiring offset null. (see Fig. 19).

* Formerly developmental number TA6122C.

Applications:

- Video amplifiers
- Fast peak detectors
- Meter-driver amplifiers
- High-frequency feedback amplifiers
- Video pre-drivers
- Oscillators
- Multivibrators
- Voltage-controlled osc.
- Fast comparators

The CA3100 circuit contains both bipolar and P-MOS transistors on a single monolithic chip.

The CA3100 is supplied in either the standard 8-lead TO-5 package ("T" suffix), or in the 8-lead TO-5 dual-in-line formed-lead "DIL-CAN" package ("S" suffix).

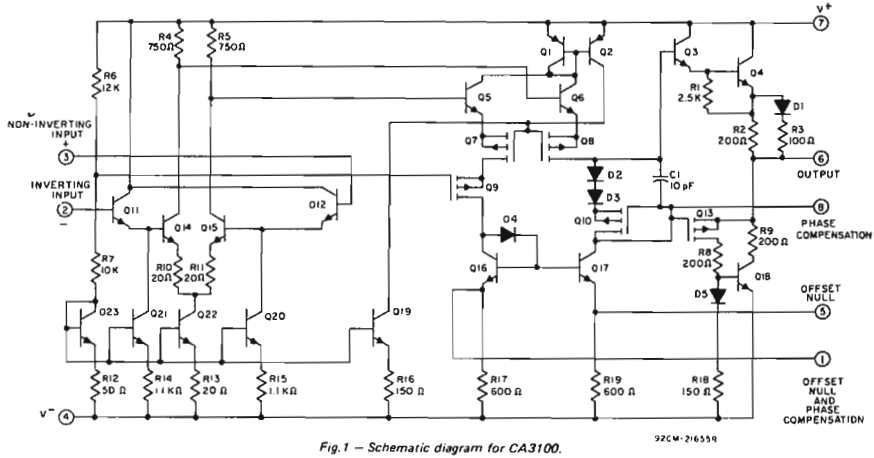


Fig. 1 – Schematic diagram for CA3100.

MAXIMUM RATINGS, *Absolute-Maximum Values at* T_A = 25°C:

SUPPLY VOLTAGE (Between V^+ and V^- terminals)	36	V
DIFFERENTIAL INPUT VOLTAGE	±12	V
INPUT VOLTAGE TO GROUND*	±15	V
OFFSET TERMINAL TO V^- TERMINAL VOLTAGE	±0.5	V
OUTPUT CURRENT	50	mA●
DEVICE DISSIPATION:		
Up to T_A = 55°C	630	mW
Above T_A = 55°C Derate Linearly at	6.67	mW/°C

AMBIENT TEMPERATURE RANGE:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	300	°C

* If supply voltage is less than ± 15 volts, the maximum input voltage to ground is equal to the supply voltage.

● CA3100S, CA3100T does not contain circuitry to protect against short circuits in the output.

TYPICAL CHARACTERISTIC CURVES

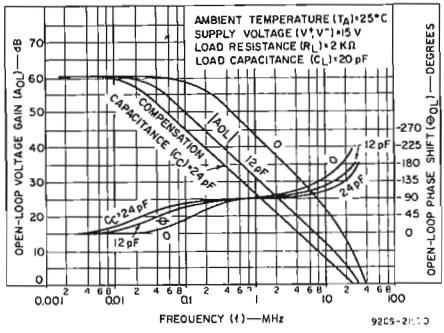


Fig.2 – Open-loop gain, open-loop phase shift vs. frequency.

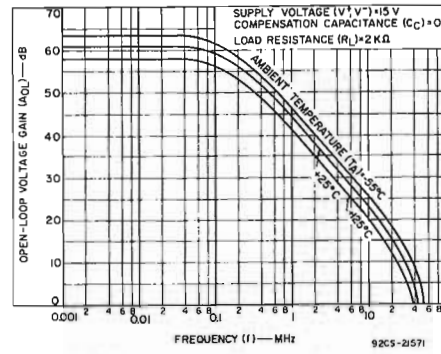


Fig.3 – Open-loop gain vs. frequency and temperature.

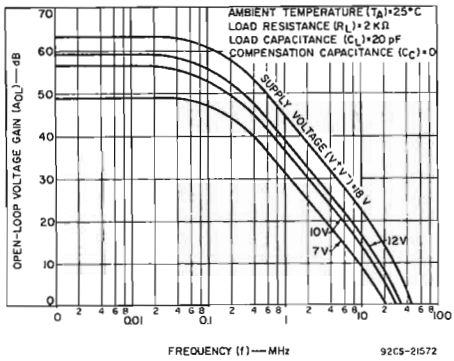


Fig.4 – Open-loop gain vs. frrquency and supply voltage.

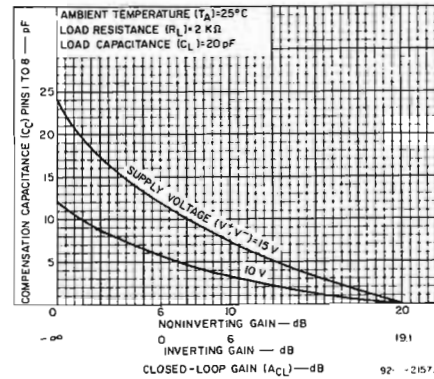


Fig.5 – Required compensation capacitance vs. closed-loop gain.

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C:*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS SUPPLY VOLTAGE (V^+,V^-)=15 V UNLESS OTHERWISE SPECIFIED	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC						
Input Offset Voltage	V_{IO}	V_O = 0 ± 0.1 V	—	±1	±5	mV
Input Bias Current	I_{IB}	V_O = 0 ± 1 V	—	0.7	2	μA
Input Offset Current	I_{IO}	V_O = 0 ± 1 V	—	±0.05	±0.4	μA
Low-Frequency Open-Loop Voltage Gain ◆	A_{OL}	V_O = ±1 V Peak, F = 1 kHz	56	61	—	dB
Common-Mode Input Voltage Range	V_{ICR}	CMRR ≥ 76 dB	±12	+14 −13	—	V
Common-Mode Rejection Ratio	CMRR	V_I Common Mode = ±12 V	76	90	—	dB
Maximum Output Voltage Positive	V_{OM}^+	Differential Input Voltage = 0 ± 0.1 V	+9	+11	—	V
Maximum Output Voltage Negative	V_{OM}^-	R_L = 2 KΩ	−9	−11	—	V
Maximum Output Current Positive	I_{OM}^+	Differential Input Voltage = 0 ± 0.1 V	+15	+30	—	mA
Maximum Output Current Negative	I_{OM}^-	R_L = 250 Ω	−15	−30	—	mA
Supply Current	I^+	V_O = 0 ± 0.1 V, R_L ≥ 10 KΩ	—	8.5	10.5	mA
Power-Supply Rejection Ratio	PSRR	ΔV^+ = ± 1 V, ΔV^- = ± 1 V	60	70	—	dB
DYNAMIC						
Unity-Gain Crossover Frequency	f_T	C_C = 0, V_O = 0.3 V (P-P)	—	38	—	MHz
1-MHz Open-Loop Voltage Gain	A_{OL}	f = 1 MHz, C_C = 0, V_O = 10 V (P-P)	36	42	—	dB
Slew Rate: 20-dB Amplifier	SR	A_V = 10, C_C = 0, V_I = 1 V (Pulse)	50	70	—	V/μs
Slew Rate: Follower Mode	SR	A_V = 1, C_C = 10 pF, V_I = 10 V (Pulse)	—	25	—	V/μs
Power Bandwidth ▲: 20-dB Amplifier	PBW	A_V = 10, C_C = 0, V_O = 18 V (P-P)	0.8	1.2	—	MHz
Power Bandwidth ▲: Follower Mode	PBW	A_V = 1, C_C = 10 pF, V_O = 18 V (P-P)	—	0.4	—	MHz
Open-Loop Differential Input Impedance	Z_I	F = 1 MHz	—	30	—	KΩ
Open-Loop Output Impedance	Z_O	F = 1 MHz	—	110	—	Ω
Wideband Noise Voltage Referred to Input	e_N(Total)	BW = 1 MHz, R_S = 1 KΩ	—	8	—	μV_{RMS}
Settling Time [To Within ±50 mV of 9 V Output Swing]	t_s	R_L = 2 KΩ, C_L = 20 pF	—	0.6	—	μs

▲ Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_O \text{ (P-P)}}$ ◆ Low-frequency dynamic characteristic

TYPICAL CHARACTERISTIC CURVES (Cont'd)

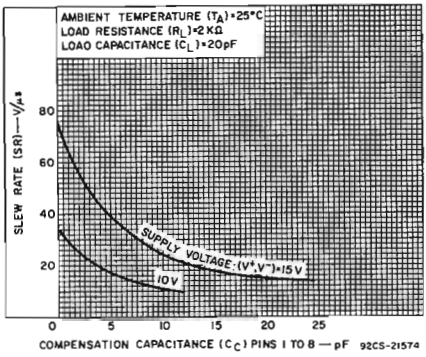


Fig.6 – Slew rate vs. compensation capacitance.

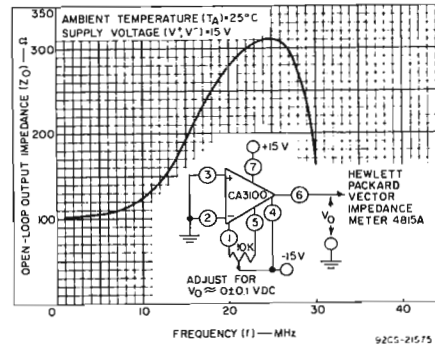


Fig.7 – Typical open-loop output impedance vs. frequency.

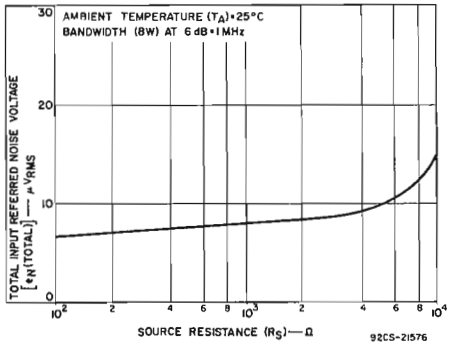


Fig.8 – Wideband input noise voltage vs. source resistance.

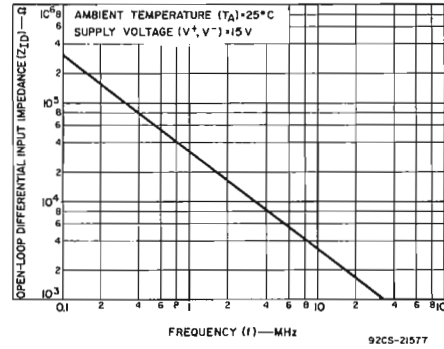


Fig.9 – Typical open-loop differential input impedance vs. frequency.

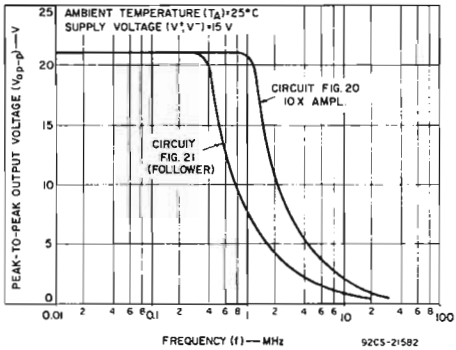


Fig.10 – Maximum output voltage swing vs. frequency.

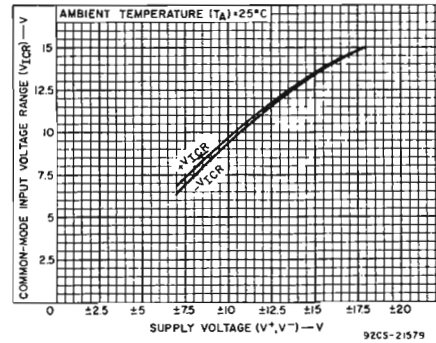


Fig.11 – Common-mode input voltage range vs. supply voltage.

TYPICAL CHARACTERISTIC CURVES (Cont'd)

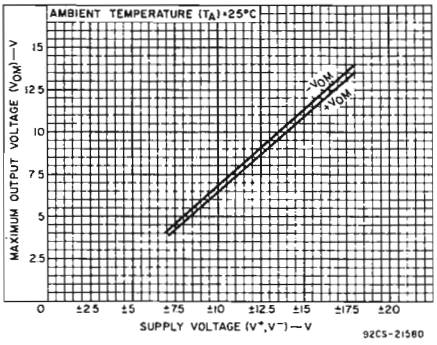


Fig.12 – Maximum output voltage vs. supply voltage.

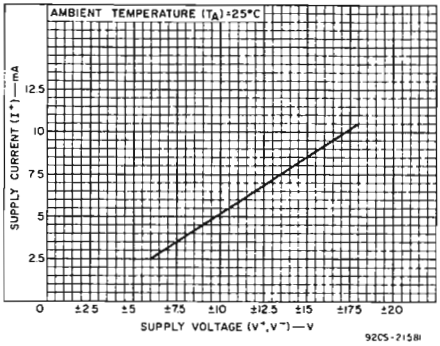


Fig.13 – Supply current vs. supply voltage.

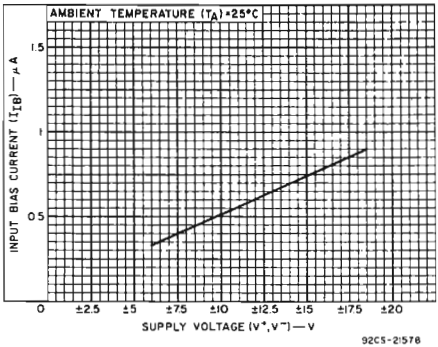


Fig.14 – Input bias current vs. supply voltage.

TYPICAL APPLICATIONS

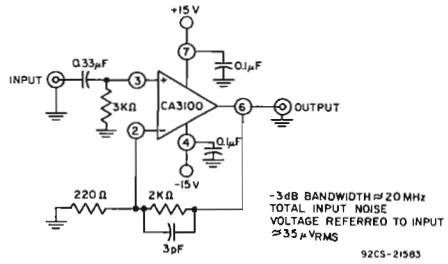


Fig.15 – 20 dB video amplifier.

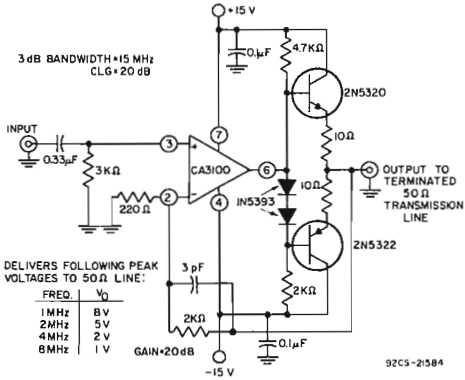


Fig.16 – 20 dB video line driver.

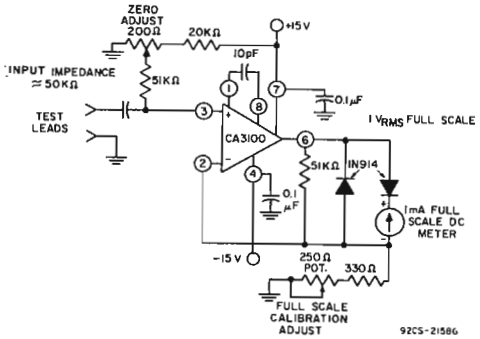


Fig.17 - 1 MHz meter-driver amplifier.

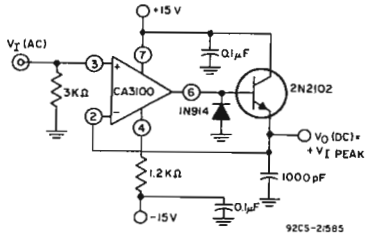


Fig.18 – Fast positive peak detector.

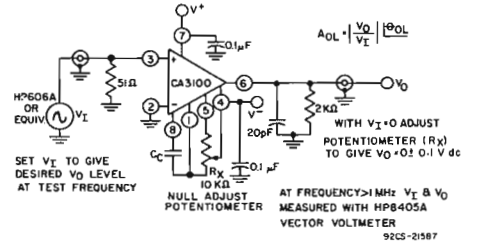


Fig.19 – Open-loop voltage gain test circuit.

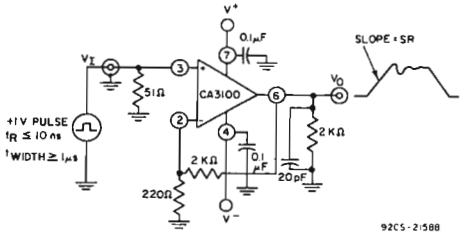


Fig.20 – Slew rate in 10X amplifier test circuit.

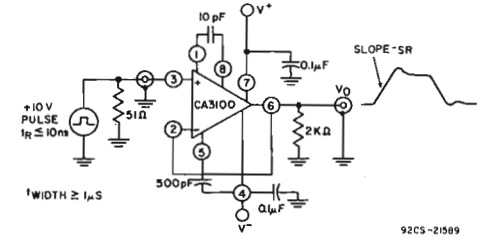


Fig.21 – Follower slew rate test circuit.

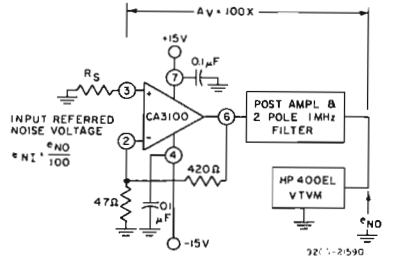


Fig.22 – Wideband input noise voltage test circuit.

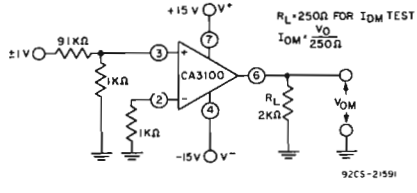


Fig.23 – Output voltage swing (V_{OM}), output current swing (I_{OM}) test circuit.

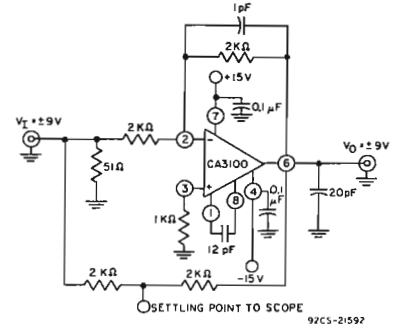


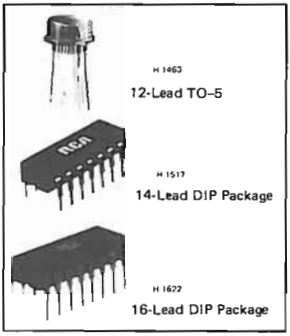
Fig.24 – Settling time test circuit.

RCA
Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3118AT CA3146AE CA3183AE
CA3118T CA3146E CA3183E



High-Voltage Transistor Arrays

Applications

- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- Lamp and relay drivers (CA3183AE, E)
- Thyristor firing (CA3183AE, E)

Features

- Matched general-purpose transistors
- V_{BE} matched ±5mV max.
- Operation from DC to 120 MHz (CA3118AT, T; CA3146AE, E)
- Low-noise figure: 3.2dB typ. at 1kHz (CA3118AT, T; CA3146AE, E)
- High I_C: 75mA max. (CA3183AE, E)

RCA-CA3118AT, CA3118T, CA3146AE, CA3146E, CA-3183AE, and CA3183E* are general-purpose high-voltage silicon n-p-n transistor arrays on a common monolithic substrate.

Types CA3118AT and CA3118T consist of four transistors with two of the transistors connected in a Darlington configuration. These types are well suited for a wide variety of applications in low-power systems in the DC through VHF range. Both types are supplied in a hermetically sealed 12-lead TO-5 type package and operate over the full military temperature range. (CA3118AT and CA3118T are high-voltage versions of the popular predecessor type CA3018.

Types CA3146AE and CA3146E consist of five transistors with two of the transistors connected to form a differentially-connected pair. These types are recommended for low-power applications in the DC through VHF range.

Types CA3183AE and CA3183E consist of five high-current transistors with independent connections for each transistor. In addition two of these transistors (Q1 and Q2) are matched at low-current (i.e. 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design.

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

For detailed application information, see companion Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated Circuit Transistor Array."

*Formerly Developmental Types Nos.

CA3118AT	– TA6091	CA3146E	– TA6181
CA3118T	– TA6182	CA3183AE	– TA6094
CA3146AE	– TA6084	CA3183E	– TA6183

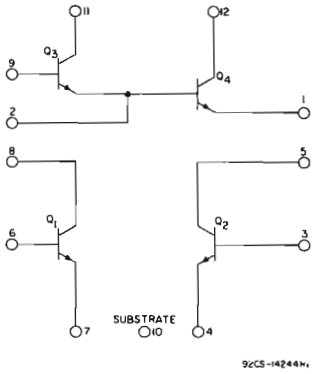
TYPE	P_T● max. mW	I_C max. mA	V_{CEO} max. V	V_{CBO} max. V	V_{CE} sat. at 10 mA typ. V	h_{FE} at 1mA, & V_{CE}=5V typ.	V_{IO} Diff. Pair at 1mA max. mV	I_{IO} Diff. Pair at 1mA max. μA	T_A Range (Operating) °C
VALUES APPLY FOR EACH TRANSISTOR									
CA3118AT	300	50	40	50	0.33	95	±5	2	
CA3118T	300	50	30	40	0.33	95	±5	2	
CA3146AE	300	50	40	50	0.33	95	±5	2	−55 – +125
CA3146E	300	50	30	40	0.33	95	±5	2	
CA3183AE	500	75	40	50	0.16	75	±5	2.5	
CA3183E	500	75	30	40	0.16	75	±5	2.5	

Caution on Total Package Power Dissipation: The maximum total package dissipation rating for the CA3118 Series circuits is 450 mW at temperatures up to +85°C, then derate linearly at 5 mW°C. The maximum total package dissipation rating for the CA3146 and CA3183 Series circuits is 750 mW at temperatures up to +55°C, then derate linearly at 6.67 mW°C.

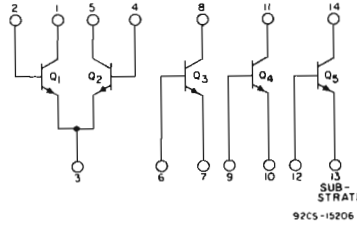
MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^oC$

Power Dissipation:		
Any one transistor –		
CA3118AT, CA3118T, CA3146AE, CA3146E	300	mW
CA3183AE, CA3183E	500	mW
Total package –		
Up to 85°C (CA3118AT, CA3118T)	450	mW
Up to 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	750	mW
Above 85°C (CA3118AT, CA3118T)	derate linearly 5	mW/°C
Above 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating –	–55 to +125	°C
Storage (all types)	–65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO}):		
CA3118AT, CA3146AE, CA3183AE	40	V
CA3118T, CA3146E, CA3183E	30	V
Collector-to-Base Voltage (V_{CBO}):		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Collector-to-Substrate Voltage (V_{CIO}): ■		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Emitter-to-Base Voltage (V_{EBO}) all types	5	V
Collector Current –		
CA3118AT, CA3118T, CA3146AE, CA3146E	50	mA
CA3183AE, CA3183E	75	mA
Base Current (I_B) – CA3183AE, CA3183E	20	mA

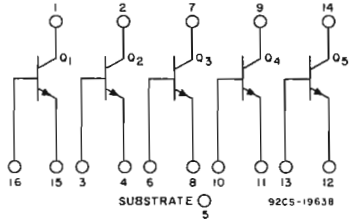
■ The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.



CA3118AT, CA3118T,



CA3146AE, CA314E



CA3183AE, CA3183E

Fig. 1 – Schematic diagrams of high-voltage arrays.

COMPARISON OF RELATED PREDECESSOR TYPE WITH TYPES IN THIS DATA BULLETIN

	DATA FILE NO.	V_{CEO} min.	V_{CBO} min.	$V_{CE\ sat.}$ typ. V	V_{BE} typ. V	I_C max. mA	C_{CB} typ. pF	C_{CI} typ. pF	C_{EB} typ. pF
				I_C=10 mA	I_C=1 mA				
CA3018	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3018A	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3118AT		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3118T		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=10 mA	I_C=1 mA				
CA3046	341	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3146AE		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3146E		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=50 mA	I_C=10 mA				
CA3083	481	15	20	0.4	0.74	100	–	–	–
CA3183AE		40	50	1.7	0.75	75	–	–	–
CA3183E		30	40	1.7	0.75	75	–	–	–

NOTE: Related predecessor types are shown in shaded areas.

STATIC ELECTRICAL CHARACTERISTICS – CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS $T_A = 25^oC$	LIMITS CA3118AT, CA3146AE Min.	CA3118AT, CA3146AE Typ.	CA3118AT, CA3146AE Max.	CA3118T, CA3146E Min.	CA3118T, CA3146E Typ.	CA3118T, CA3146E Max.	UNITS
For Each Transistor:									
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	50	72	–	40	72	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	40	56	–	30	56	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 10\mu A$, $I_B = 0$, $I_E = 0$	50	72	–	40	72	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	5	7	–	5	7	–	V
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	–	see curve	5	–	see curve	5	μA
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	–	0.002	100	–	0.002	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=5V, I_C=10mA	–	85	–	–	85	–	–
		V_{CE}=5V, I_C=1mA	30	100	–	30	100	–	–
		V_{CE}=5V, I_C=10μA	–	90	–	–	90	–	–
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$, $I_C = 1mA$	0.63	0.73	0.83	0.63	0.73	0.83	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	$I_C = 10mA$, $I_B = 1mA$	–	0.33	–	–	0.33	–	V
For transistors Q3 and Q4 (Darlington Configeration):									
Collector-Cutoff Current (CA3118AT and CA3118T only)	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	–	–	5	–	–	–	μA
DC Forward-Current Transfer Ratio (CA3118AT and CA3118T only)	h_{FE}	$V_{CE} = 5V$, $I_C = 1mA$	1500	9000	–	1500	9000	–	–
Base-to-Emitter (Q3 to Q4)	V_{BE}	V_{CE}=5V, I_E=10mA	–	1.46	–	–	1.46	–	V
		V_{CE}=5V, I_E=1mA	–	1.32	–	–	1.32	–	V
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\|\frac{\Delta V_{BE}}{\Delta T}\right\|$	$V_{CE} = 5V$, $I_E = 1mA$	–	4.4	–	–	4.4	–	mV/^{o}C
For transistors Q1 and Q2 (AS a Differential Amplifier):									
Magnitude of Input Offset Voltage $\left\|V_{BE1} - V_{BE2}\right\|$	$\|V_{IO}\|$	$V_{CE} = 5V$, $I_E = 1mA$	–	0.48	5	–	0.48	5	mV
Magnitude of h_{FE} Ratio (CA3118AT and CA3118T only)		$V_{CE} = 5V$, $I_{C1} = I_{C2} = 1mA$	0.9	1.0	1.1	0.9	1.0	1.1	–
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\|\frac{\Delta V_{BE}}{\Delta T}\right\|$	$V_{CE} = 5V$, $I_E = 1mA$	–	1.9	–	–	1.9	–	mV/^{o}C
Magnitude of V_{IO} ($V_{BE1} - V_{BE2}$) Temperature Coefficient	$\left\|\frac{\Delta V_{IO}}{\Delta T}\right\|$	$V_{CE} = 5V$, $I_{C1} = I_{C2} = 1mA$	–	1.1	–	–	1.1	–	μV/^{o}C
Magnitude of Input Offset Current $\left\|I_{IO_1} - I_{IO_2}\right\|$ (CA3146AE and CA3146E only)	I_{IO}	$V_{CE} = 5V$, $I_{C_1} = I_{C_2} = 1$ mA	–	0.3	2	–	0.3	2	μA

DYNAMIC ELECTRICAL CHARACTERISTICS — CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	CA3118AT CA3146AE			CA3118T CA3146E			UNITS
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Low Frequency Noise Figure	NF	f = 1kHz, V_{CE} = 5V, I_C = 100μA, Source resistance = 1 kΩ	–	3.25	–	–	3.25	–	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:									
Foward-Current Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	–	100	–	–	100	–	–
Short-Circuit Input Impedance	h_{ie}		–	2.7	–	–	3.5	–	kΩ
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	μmho
Open-Circuit Reverse - Voltage Transfer Ratio	h_{re}		–	1.8×10^{-4}	–	–	1.8×10^{-4}	–	–
Admittance Characteristics:									
Foward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	–	31-j1.5	–	–	31-j1.5	–	mmho
Input Admittance	Y_{ie}		–	0.35+j0.04	–	–	0.3+j0.04	–	mmho
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho
Reverse Transfer Admittance	Y_{re}			See curve			See curve		mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 3mA	300	500	–	300	500	–	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 5V, I_E = 0	–	0.70	–	–	0.70	–	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5V, I_C = 0	–	0.37	–	–	0.37	–	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 5V, I_C = 0	–	2.2	–	–	2.2	–	pF

STATIC ELECTRICAL CHARACTERISTICS — CA3183 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	LIMITS CA3183AE			LIMITS CA3183E			UNITS
			Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each Transistor:									
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=100μA, I_E=0	50	–	–	40	–	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	40	–	–	30	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI}=100μA, I_B=0, I_E = 0	50	–	–	40	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	5	–	–	5	–	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	10	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	1	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V, I_C = 10mA	40	–	–	40	–	–	–
		V_{CE} = 5V, I_C = 50mA	40	–	–	40	–	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	0.65	0.75	0.85	0.65	0.75	0.85	V
Collector-to-Emitter Saturation Voltage	*V_{CEsat}	I_C = 50mA, I_B = 5mA	–	1.7	3.0	–	1.7	3.0	V
For Transistors Q1 and Q2 (As a Differential Amplifier):									
Absolute Input Offset Voltage	$\lvert V_{IO} \rvert$	V_{CE} = 3V, I_C = 1mA	–	0.47	5	–	0.47	5	mV
Absolute Input Offset Current	$\lvert I_{IO} \rvert$		–	0.78	2.5	–	0.78	2.5	μA

* A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application.

TYPICAL STATIC CHARACTERISTICS CURVES — CA3118 and CA3146 SERIES

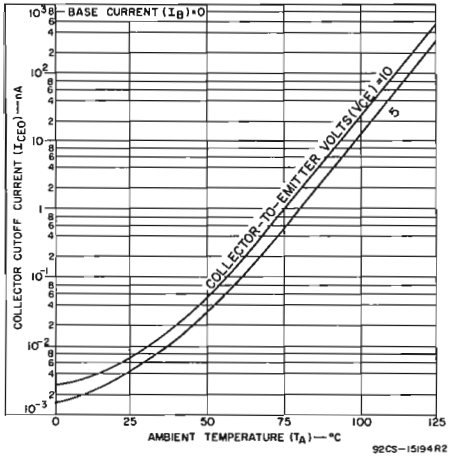


Fig. 2 – I_{CEO} vs. T_A for any transistor.

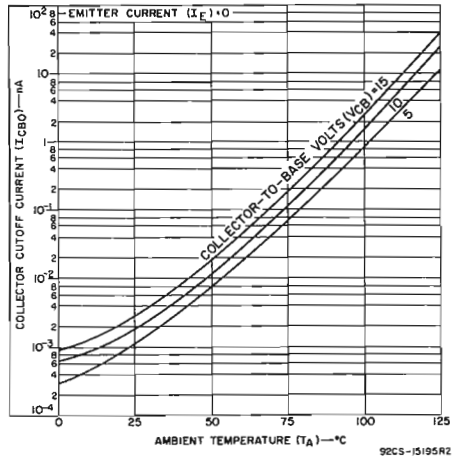


Fig. 3 – I_{CBO} vs. T_A for any transistor.

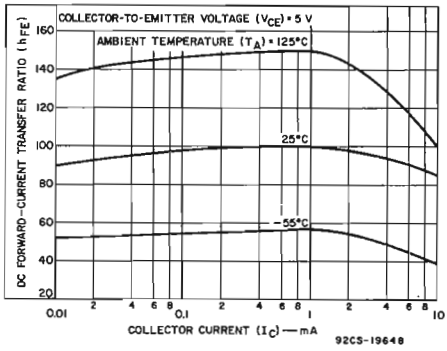


Fig. 4 – h_{FE} vs. I_C for any transistor.

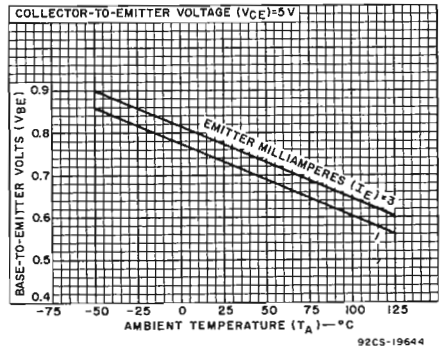


Fig. 5 – V_{BE} vs. T_A for any transistor.

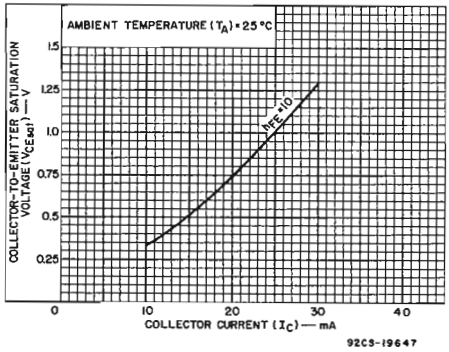


Fig. 6 – V_{CE} sat vs. I_C for any transistor.

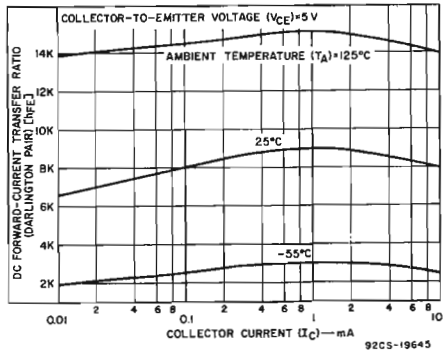


Fig. 7 – h_{FE} vs. I_C for Darlington pair (Q3 and Q4) for types CA3118AT and CA3118T.

TYPICAL STATIC CHARACTERISTICS CURVES – CA3118 and CA3146 SERIES

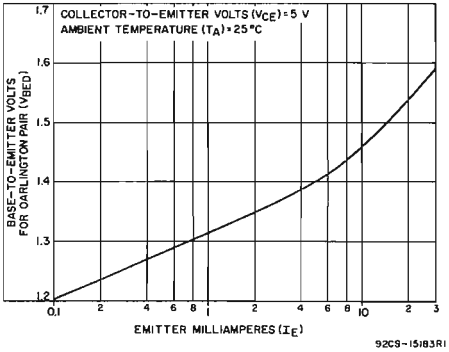


Fig. 8 – V_{BE} vs. I_E for Darlington pair (Q3 and Q4).

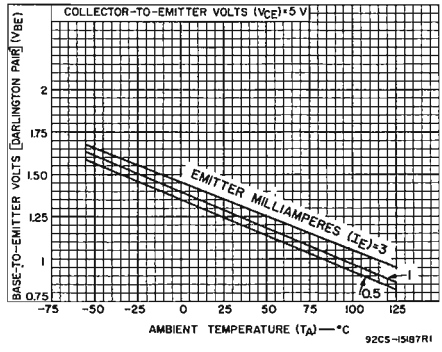


Fig. 9 – V_{BE} vs. T_A for Darlington pair (Q3 and Q4).

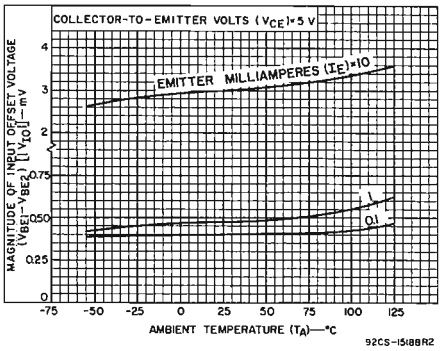


Fig. 10 – V_{IO} vs. T_A for Q1 and Q2.

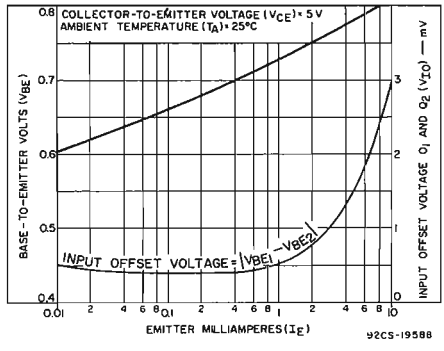


Fig. 11 – V_{BE} and V_{IO} vs. I_E for Q1 and Q2.

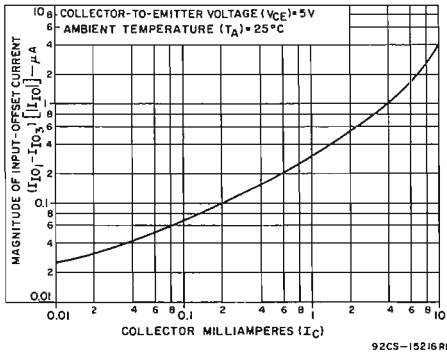


Fig. 12 – I_{IO} vs. I_C (Q1 and Q2) for types CA3146AE and CA3146E.

TYPICAL DYNAMIC CHARACTERISTICS CURVES (FOR ANY TRANSISTOR) -- CA3118, CA3146 SERIES

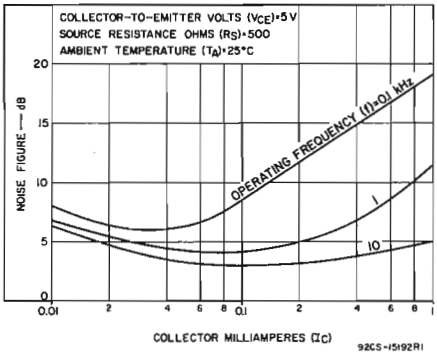


Fig. 13 – NF vs. I_C @ R_S = 500Ω.

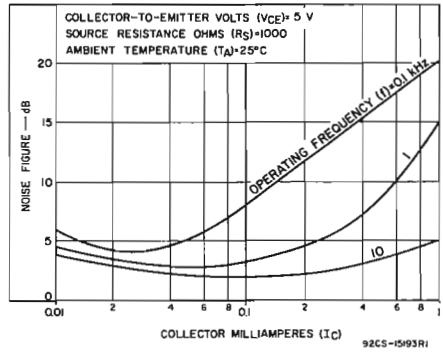


Fig. 14 – NF vs. I_C @ R_S = 1kΩ.

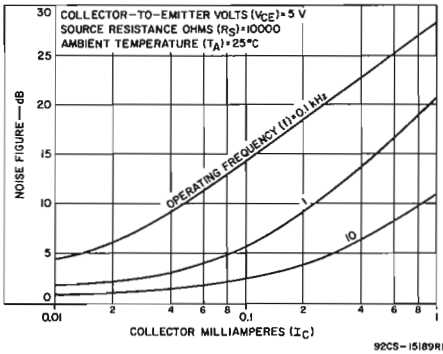


Fig. 15 – NF vs. I_C @ R_S = 10kΩ.

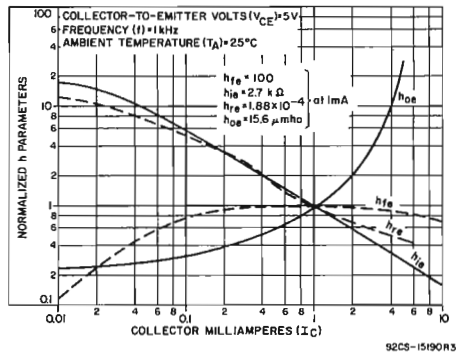


Fig. 16 – h_{fe}, h_{ie}, h_{oe}, h_{re} vs. I_C.

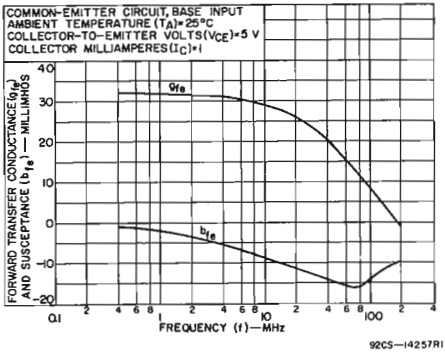


Fig. 17 – y_{fe} vs. f.

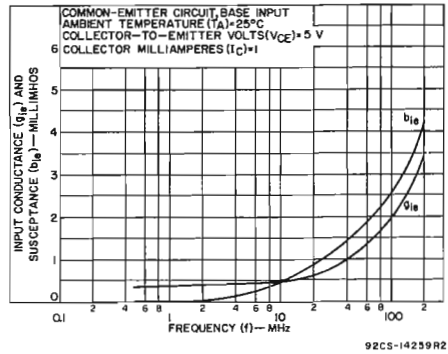


Fig. 18 – y_{ie} vs. f.

TYPICAL DYNAMIC CHARACTERISTICS CURVES (FOR ANY TRANSISTOR) – CA3118, CA3146 SERIES

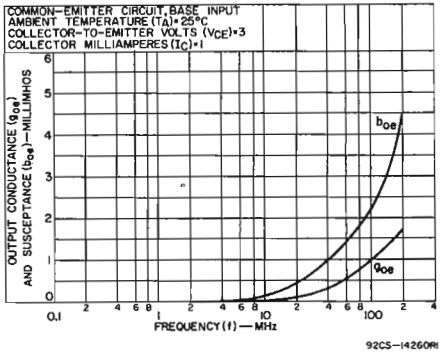


Fig. 19 – y_{oe} vs. f.

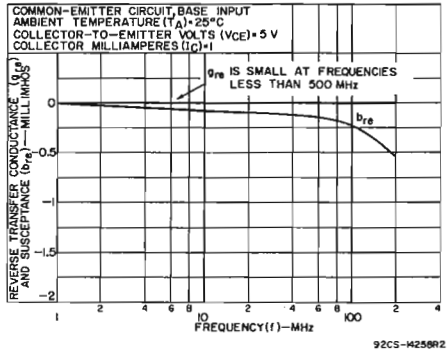


Fig. 20 – y_{re} vs. f.

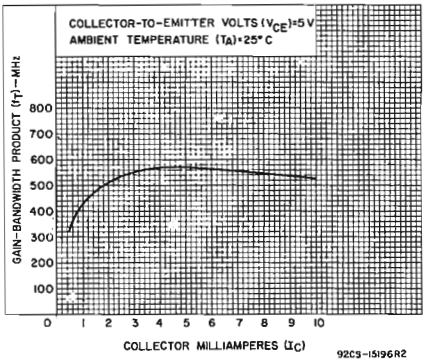


Fig. 21 – f_T vs. I_C.

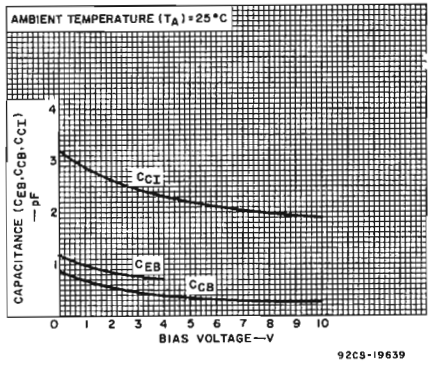


Fig. 22 – C_{EB}, C_{CB}, C_{CI} vs. bias voltage

TYPICAL STATIC CHARACTERISTICS CURVES – CA3183 SERIES

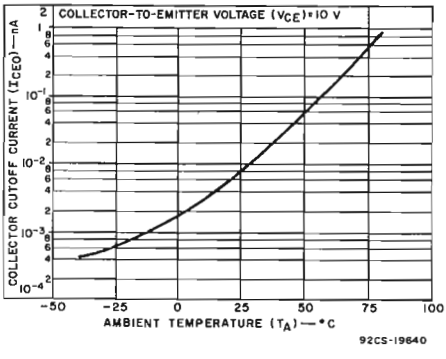


Fig. 23 – I_{CEO} vs. T_A for any transistor.

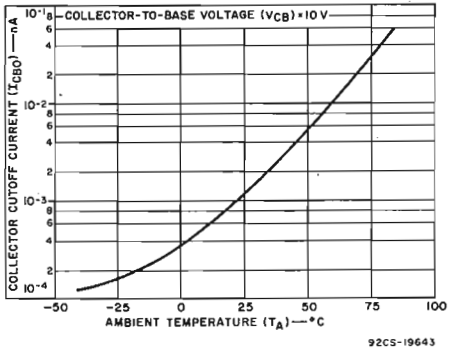


Fig. 24 – I_{CBO} vs. T_A for any transistor.

TYPICAL STATIC CHARACTERISTICS CURVES – CA3183 SERIES

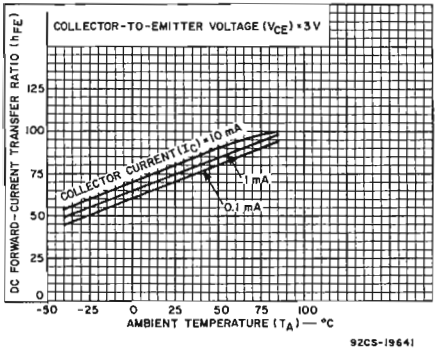


Fig. 25 – h_{FE} vs. T_A for any transistor.

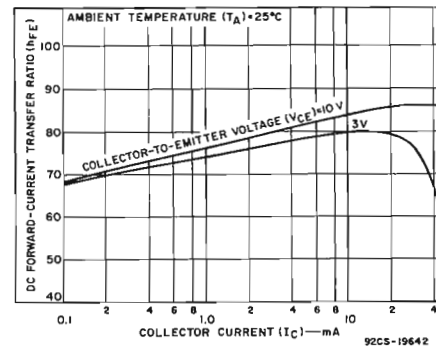


Fig. 26 – h_{FE} vs. I_C for any transistor.

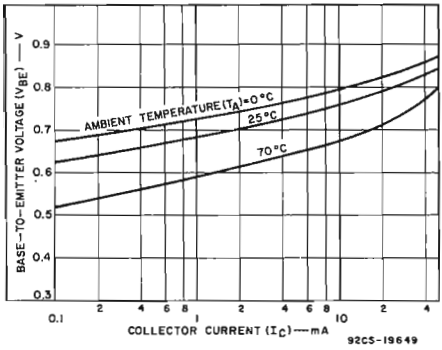


Fig. 27 – V_{BE} vs. I_C for any transistor.

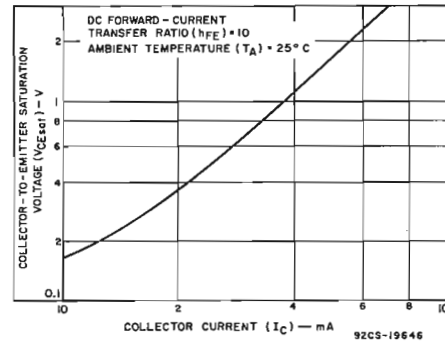


Fig. 28 – $V_{CE\ sat}$ vs. I_C for any transistor.

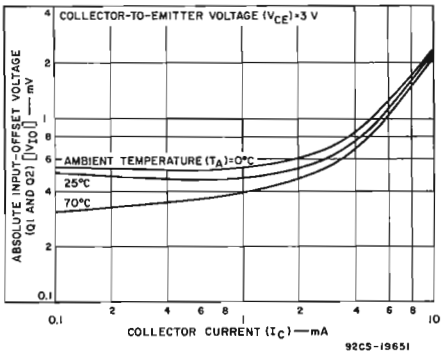


Fig. 29 – $|V_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

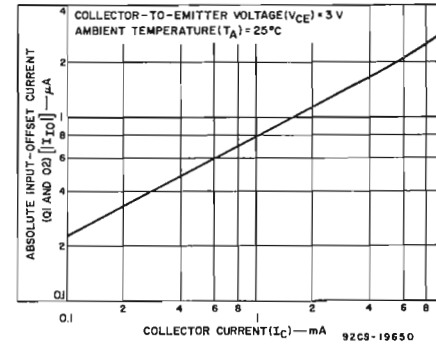


Fig. 30 – $|I_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3120E

16-Lead Dual-In-Line Plastic Package

TV Signal Processor ("Jungle" Circuit)

For Color and Monochrome Receivers

Features

- Internal impulse noise processing
- Sync separator — low impedance, dual polarity
- Strobed AGC system
- IF AGC output
- Delayed outputs for forward or reverse AGC tuners
- Automatic noise threshold and AGC detector level control
- High-impedance video input
- Low-impedance video output
- Choice of external time constants for sync separator
- Negative power supply not required
- RF AGC delay externally controlled
- **Application Note ICAN-6302, "Description and Application of the RCA-CA3120E Integrated-Circuit TV-Signal Processor"**

RCA-CA3120E is a monolithic silicon integrated circuit TV signal processor for use in color or monochrome receivers. The circuit provides low-impedance video output signals, stripped synchronization signals in both polarities, and AGC output signals for IF (reverse) and tuner (forward and/or reverse).

The circuit design of the CA3120E features impulse noise inversion, delay techniques to reduce the deleterious effects of impulse noise in the receiver AGC and sync circuits. In addition, the CA3120E incorporates standard AGC strobing techniques.

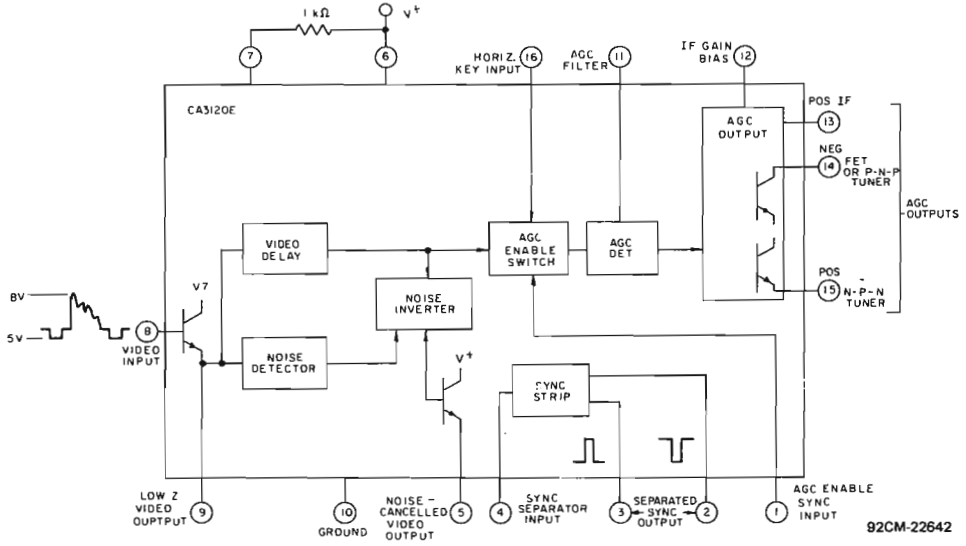


Fig. 1 — Simplified block diagram of the CA3120E.

ELECTRICAL CHARACTERISTICS at $T_A = 25^{\circ}C$, Supply Voltage (V^+) = 24 V and Referenced to Test Circuits and Test Conditions (Figs. 6, 7, and 8).

CHARACTERISTICS	TERMINAL MEASURED AND SYMBOL	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current (Pulse Test)	I_{T24}	20	–	40	mA
AGC Threshold (Sync Tip Level at Video Input)	V_{TH}	4.5	–	5.5	V
Video Input Amplitude (White Positive)	V_8	–	3	–	Vp-p
Video Output Amplitude (Low Impedance)	V_9	–	3	–	Vp-p
Noise Cancelled Video Output at V_{TH} (Black Positive, Gain ≅ 2)	V_5	6.6	–	9.2	V
AGC to Noise Separation	$V_{TH\ (SEP)}$	1.1	–	2.2	V
Sync Input Current for Full Amplitude Outputs	$I_{4\ (ON)}$	–	–	70	μA
Maximum Leakage Current at Terminal 4	$I_{4\ (OFF)}$	–	–	±6	μA
Sync Outputs:					
Negative Sync Low	$V_{2(L)}$	0	–	2.6	V
Negative Sync High	$V_{2(H)}$	23.8	–	24	V
Positive Sync Low	$V_{3(L)}$	0	–	0.2	V
Positive Sync High	$V_{3(H)}$	20.1	–	24	V
AGC Filter:					
Charge Current (Pulse Test)	$I_{11(CH)}$	12	–	36	mA
Discharge Current	$I_{11(DISCH)}$	1.1	–	2.6	mA
Leakage Current	$I_{11(LEAK)}$	–	–	±6	μA
AGC Enable:					
Horizontal Keying	$V_{16\ (ON)}$	3	–	6	V
Negative Sync Input Current	$I_{1\ (ON)}$	–	1	–	mA
Maximum IF Gain-Clamp Voltage	V_{11}	4.8	–	5.7	V
Maximum IF Gain Bias	V_{12}	4.2	–	5.2	V
IF AGC Voltage:					
Low	$V_{13\ (LOW)}$	0	–	3.3	V
High	$V_{13(HIGH)}$	5.7	–	6	V
Tuner Currents:					
Reverse AGC (FET) OFF Current	$I_{14\ (OFF)}$	–	–	±6	μA
Reverse AGC (FET) ON Current	$I_{14\ (ON)}$	1.8	–	5.5	mA
Forward AGC (n-p-n) OFF Current	$I_{15\ (OFF)}$	–	–	±6	μA
Reverse AGC (n-p-n) ON Current	$I_{15\ (ON)}$	4.5	–	15	mA
Internal Noise-Lockout Time	T	1	–	63	μs

MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^oC$

DC SUPPLY VOLTAGE	30	V
DEVICE DISSIPATION:		
Up to $T_A = 55^oC$	750	mW
Above $T_A = 55^oC$	Derate linearly at 7.9	mW/^oC

AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85 ^oC
Storage	−65 to +150 ^oC
LEAD TEMPERATURE (During soldering):	
At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265 ^oC

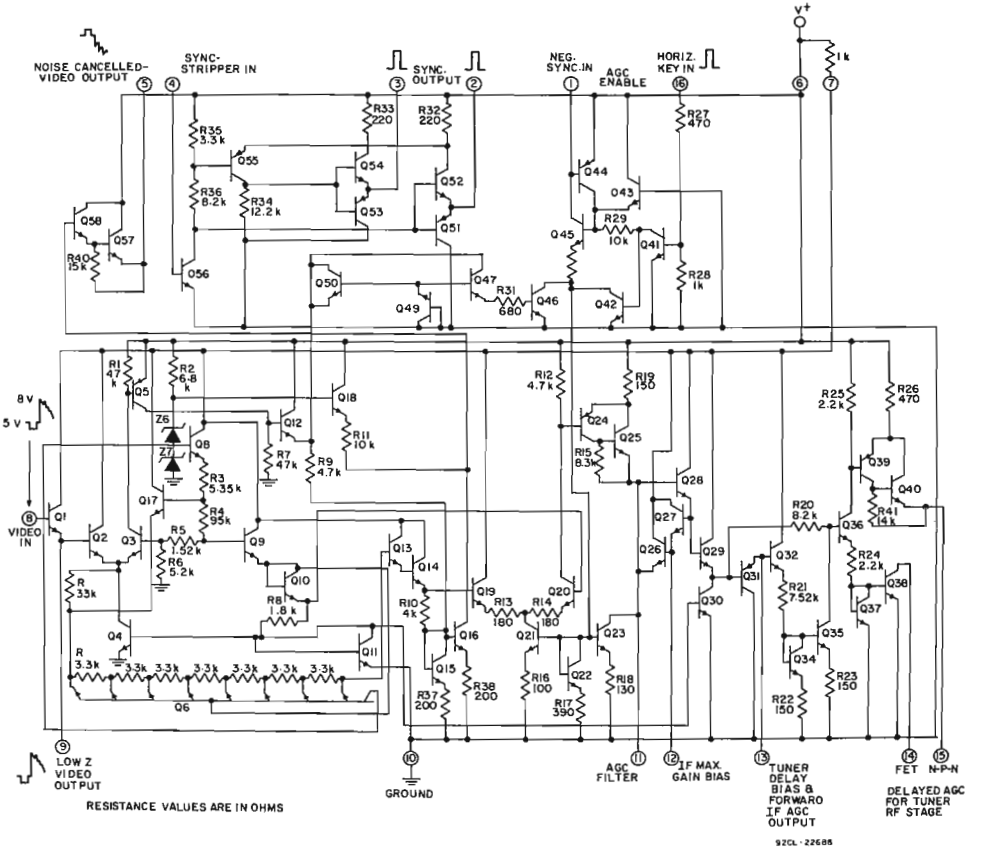


Fig. 2—Schematic diagram of the CA3120E.

CIRCUIT DESCRIPTION*

An AGC sample-and-hold system generates control voltages proportional to the video level. The sync-tip voltage is compared to an internal reference voltage during the horizontal sychronization (retrace) interval. The control voltages (AGC outputs) are supplied to the tuner's RF stage and the IF amplifier to maintain the video level at a constant value.

The composite positive and negative output sync signals are developed across a low impedance source (totem-pole circuit) at an amplitude of approximately 20 volts peak-to-peak.

Video Chain and Impulse Noise Inverter - The input video signal applied at Terminal 8 is white "positive" with a required amplitude in the range of 2 to 4 volts. The DC level of the sync peaks, AGC threshold voltage (V_{TH}) is approximately 5 volts. The level is maintained at 5 volts by the AGC loop in the circuit, comprised of the CA3120E and the TV receiver RF and IF amplifiers. A low source impedance video signal is available from the emitter of Q1 (Terminal 9 in Fig. 2). The external resistor (R_{X1} in Fig. 9) reduces the dissipation of Q1. The emitter-follower output of Q1 is direct coupled to a differential comparator stage (Q2, Q3). Unless a negative-going noise pulse is present, Q2 functions as an emitter follower and also cuts off transistors Q3, Q5, and Q17.

The output of Q2 is applied through a signal delay network, consisting of transistor Q60 and associated resistors, to the Darlington followers (Q13 and Q14). The delayed video signal at Q14 is fed via its emitter to an AGC comparator Q19 and to the junction of a noise-cancelling amplifier stage (Q16). The noise-cancelled video signal is inverted and amplified by Q16 and then connected to a Darlington emitter-follower output stage (Q57, Q58).

If impulse noise is present on the video signal, Q3 conducts and turns on transistors Q5 and Q12. Q5 inverts and "stretches" the noise pulse width. The output of Q5 is applied to an emitter follower stage (Q12). The signal from Q12, in turn, is applied to the summing junction to the noise-cancelling amplifier Q16. The noise pulse, which has now been amplified, inverted and stretched, is added to the delayed video signal from the emitter of Q14.

Because the video signal has been delayed approximately, 300 nanoseconds and the noise pulse has been widened ("stretched") approximately 500 nanoseconds, the output of the combined signal no longer contains impulse noise signals. The derived noise-gating pulse "surrounds" and effectively eliminates the effects of the impulse noise.

The noise-cancelled video signal, amplified and buffered, is available at Terminal 5 for use in the sync-separator stage. The peak-to-peak amplitude of the noise-cancelled output signal is approximately twice the amplitude of the input video signal at Terminal 8.

Sync Separator (See Figure 3) - The sync separator stage (Q56) clamps the detected sync tips to a fixed reference voltage ($\cong$ 0.7 V) across its base-emitter junction, and amplifies a portion of the sync signal to provide dual polarity sync-signal outputs at Terminals 2 (negative) and 3 (positive). The output signals, are derived from low-impedance complementary emitter-follower stages; a base current of 100 microamperes into Terminal 4 is sufficient to generate full-amplitude sync signals.

The choice of coupling the noise-cancelled video signal from the emitter-follower (Terminal 5) to the sync separator (Terminal 4) is a user option. Fig. 4 shows three typical coupling networks.

Fig. 5 illustrates the operation of the AGC circuits. An input ramp signal, simulating the potential to which the AGC filter capacitor may be charged, is applied to Terminal 11. The forward IF AGC output voltage appears at Terminal 13. Under low-signal level conditions (represented by A to B in Fig. 5), the output level is approximately 1.4 volts less than the voltage applied to Terminal 12.

The circuit designer should select the voltage at Terminal 12 to provide the maximum IF gain required for the system. At intermediate signal level conditions (represented by B to C in Fig. 5), the IF AGC signal follows the AGC filter potential. The tuner(s) will operate at maximum gain for good signal-to-noise ratios at these equivalent input signal levels. Point C is a turnover point determined by the open-circuit potential of the tuner-delay bias potentiometer. At this potential, further change in the IF AGC output is inhibited (for good dynamic range) and the tuner AGC potentials are activated (represented by C to D).

The output at Terminal 14 with suitable level shifting is used for tuners requiring reverse AGC, such as MOSFET or electron-tube types. The output at Terminal 15 is used for tuners requiring forward AGC, such as tuners utilizing n-p-n bipolar transistors.

* For additional information refer to the "IEEE Transactions on Broadcast and TV Receivers", August 1970, pp. 185–195, Vol. BTR No. 3.

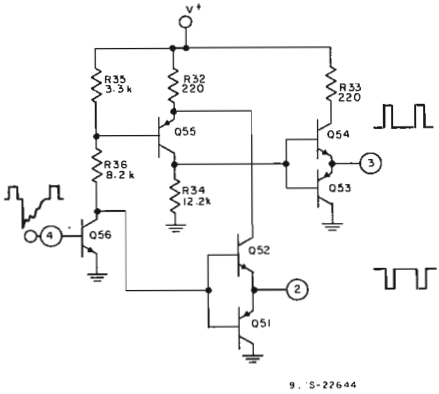


Fig. 3 – Sync separator stage.

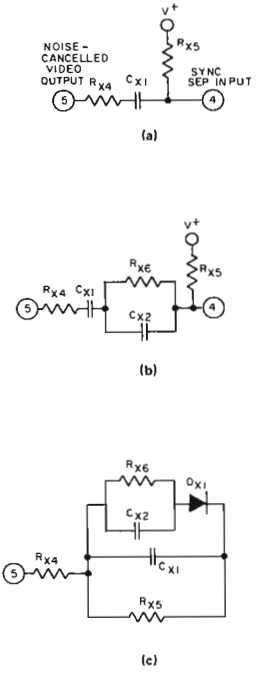


Fig. 4 – Typical coupling networks (Term. 5 to Term. 4).

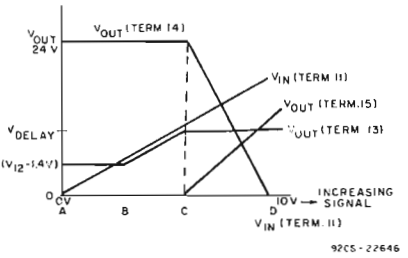


Fig. 5 – Typical operation of the AGC circuits using the CA3120E.

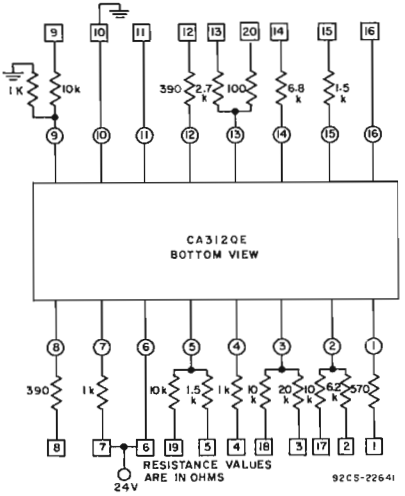


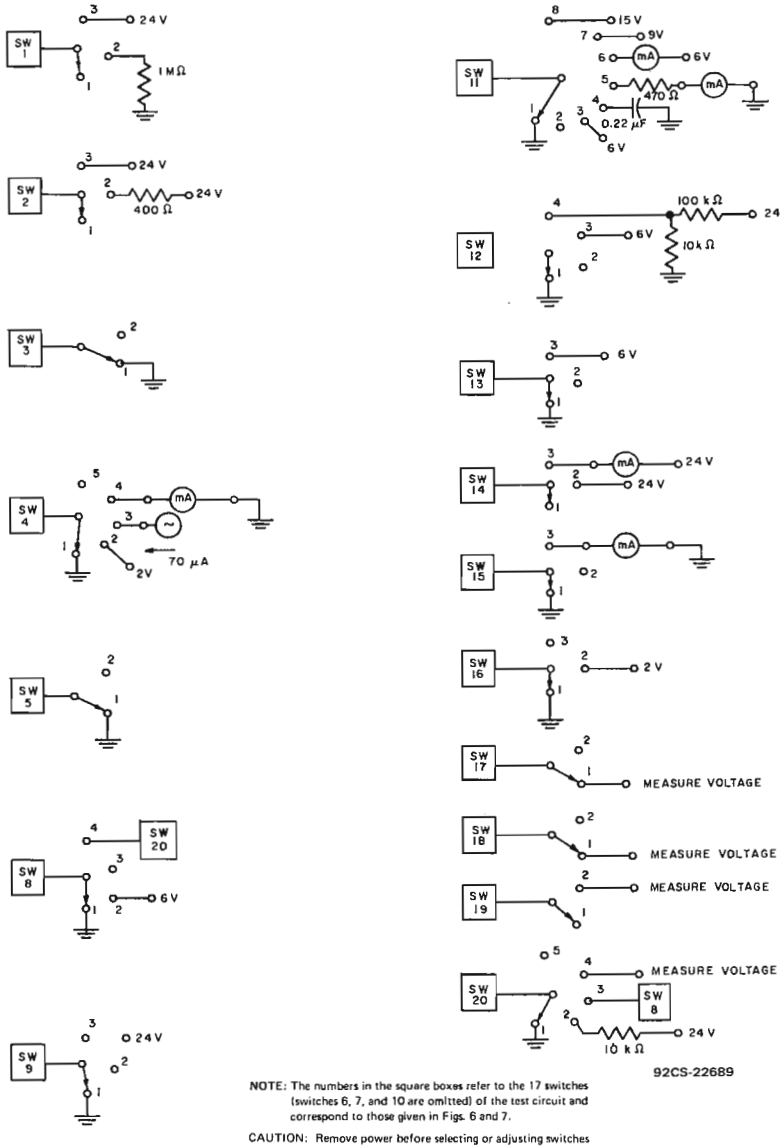
Fig. 6 – Test circuit for measuring electrical characteristics of the CA3120E. Refer to Figs. 7 and 8 for switch selector positions.

CHARACTERISTIC	TEST CONDITIONS																	TERMINAL MEASURED
	SWITCH NUMBERS																	
	1	2	3	4	5	8	9	11	12	13	14	15	16	17	18	19	20	
	SWITCH POSITION																	
I_{T24}	2	3	1	2	1	2	3	1	1	3	2	1	2	2	2	1	5	2 6 7 9 14
V_{TH}	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	1	3	8
V_5	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	2	3	19
$V_{TH(SEP)}$	3	1	2	1	1	*	3	3	4	1	1	2	1	2	2	2	1	*
$I_{4(OFF)}$	3	1	2	4	2	1	1	1	1	1	1	2	1	2	2	1	1	I_4
V_{2L}	1	2	2	3	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{2H}	3	3	1	1	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{3L}	3	3	1	1	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
V_{3H}	3	3	1	3	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
$I_{11(CH)}$	2	1	2	5	2	1	1	5	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(DISCH)}$	2	1	2	5	1	2	3	6	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(LEAK)}$	2	1	2	5	2	1	1	6	4	3	2	2	1	2	2	1	5	I_{11}
V_{11}	2	1	2	5	1	2	3	2	3	3	1	2	2	2	2	1	5	V_{11}
V_{12}	3	1	2	5	2	1	1	3	4	3	1	2	1	2	2	1	5	V_{12}
$V_{13(LOW)}$	3	1	2	5	2	2	3	1	1	2	1	2	1	2	2	1	2	V_{13}
$V_{13(HIGH)}$	3	1	2	5	2	2	3	7	4	3	2	1	1	2	2	1	4	V_{20}
$I_{14(OFF)}$	3	1	2	5	2	2	3	3	4	3	3	1	1	2	2	1	5	I_{14}
$I_{14(ON)}$	3	1	2	5	2	2	3	8	4	3	3	1	1	2	2	1	5	I_{14}
$I_{15(OFF)}$	3	1	2	5	2	2	3	3	4	3	2	3	1	2	2	1	5	I_{15}
$I_{15(ON)}$	3	1	2	5	2	2	3	8	4	3	2	3	1	2	2	1	5	I_{15}

CAUTION: Remove power before selecting or adjusting switches.

* Reduce voltage at Terminal 8 until V_{19} decreases. $V_{TH(SEP)} = V_{TH} - V_8$.

Fig. 7 – Test condition values for associated switches 1 through 20 (switches 6, 7, and 10 are omitted). Refer to Figs 6 and 8 for test circuit and test-condition selector-switch arrangements.



NOTE: The numbers in the square boxes refer to the 17 switches (switches 6, 7, and 10 are omitted) of the test circuit and correspond to those given in Figs. 6 and 7.

CAUTION: Remove power before selecting or adjusting switches

Fig. 8 – Test condition selector switch arrangement for measuring the electrical characteristics of the CA3120E.

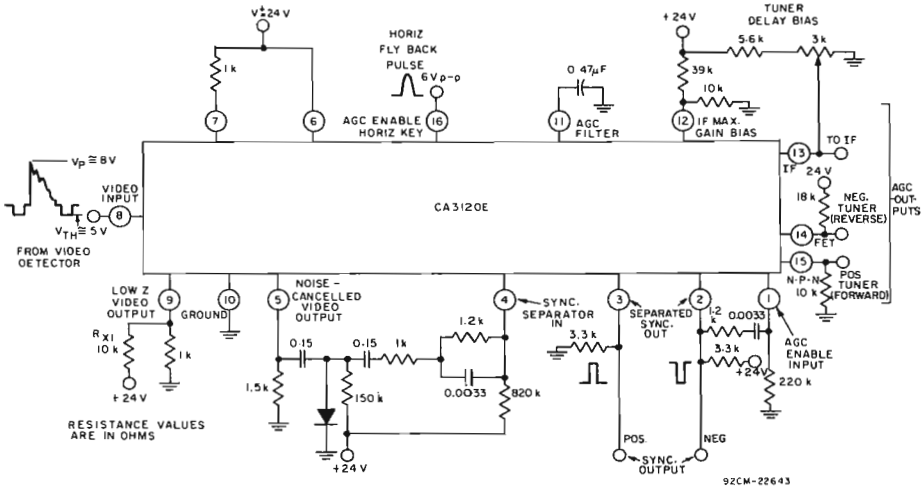


Fig. 9 – Typical application using the CA3120E.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3121E

16-Lead Dual-In-Line Plastic Package H-1622

TV Chroma Amplifier/Demodulator

Provides Complete System for Processing Chroma When Used with RCA-CA3070

Features

- Excellent linearity in dc chroma gain-controlled circuit
- Improved filtering reduces 7.2 MHz output from the color demodulators
- Current limiting for short-circuit protection
- Good tolerance to B+ supply variations
- Good temperature coefficient stability

RCA-CA3121E is a monolithic silicon integrated circuit chroma amplifier/demodulator with ACC and killer control for color-TV receivers. It is designed to function compatibly with the CA3070 in a two package chroma system. Figs. 3 and 4 show a functional block diagram and the outboard circuitry of a typical two-package chroma system incorporating the CA3121E and CA3070, respectively.

The CA3121E is supplied in a 16-lead dual-in-line plastic package.

MAXIMUM RATINGS at $T_A = 25^\circ C$

Supply Voltage	30 V
Device Dissipation:	
Up to $T_A = 55^\circ C$	750 mW
Above $T_A = 55^\circ C$	derate linearly 7.9 mW/°C
Operating Temperature Range	−40 to +85°C
Lead Temperature (During Soldering)	
At distance 1/16" ±1/32" (1.59 ±0.79 mm) from case for 10 s max.	+265°C

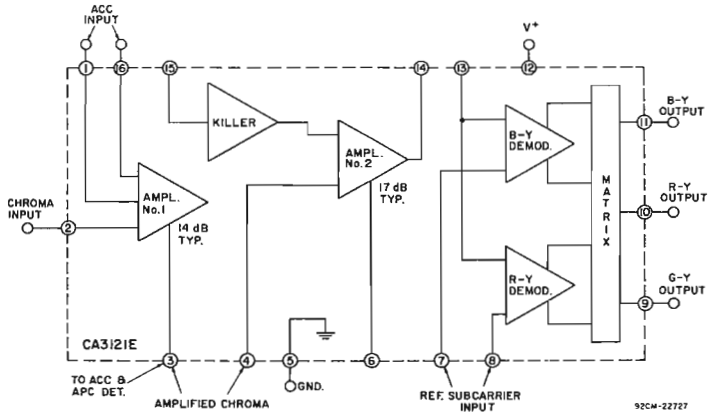


Fig. 1 – Functional block diagram of the CA3121E.

ELECTRICAL CHARACTERISTICS at T_A = 25°C and Referenced to Test Circuit (Fig. 8)

CHARACTERISTIC	TERMINAL MEASURED AND SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Supply Current	I_T	–	–	40	44	mA
Input Sensitivity	V_2	Vary Eg; set V_4 for 55 mV RMS	6	10	15	mV RMS
Second-Stage Sensitivity	V_4	Vary Eg; set V_{11} for 2 V RMS	25	55	100	mV RMS
Output Voltage (Killer off)	V_{11}	Switch Position: S1=2, S2=2, S3=2 Adjust killer potentiometer until output drops	–	–	70	mV RMS
Demodulator Characteristics:						
Output Voltages	V_9, V_{10}, V_{11}		13	14.3	15.6	V
DC Output Balance (Between any 2 outputs)	–	–	−0.6	–	+0.6	V
Unbalance	V_9, V_{10}, V_{11}	Eg=0; Switch Position: S1=1, S2=1, S3=1	–	–	0.8	Vp-p
Reletive Outputs– R-Y	V_{10}	Vary Eg; set V_{11} for 2 V RMS	1.4	1.52	1.68	V RMS
G-Y	V_9		0.3	0.4	0.5	V RMS
Relative Phase– R-Y	V_{10}	Vary Eg; set V_{11} for 2 V RMS; read phase of V_{10} and V_9	−101	−106	−111	degrees
G-Y	V_9	with V_{11} as reference	112	104	96	degrees
Max. Output Voltage	V_{11}	Eg = 750 mV	2.8	–	–	V RMS

CIRCUIT OPERATION

The CA3121E consists of three basic circuit sections: (1) amplifier No. 1, (2) amplifier No. 2, and (3) demodulator. Amplifier No. 1 contains the circuitry for automatic chroma control (ACC) and color-killer sensing. The output of amplifier No. 1 (Terminal 3) is coupled to the Chroma Signal Processor (CA3070 or equivalent) for ACC and automatic phase control (APC) operation and to the input of amplifier No. 2 (Terminal 4) containing the chroma gain control circuitry. The signal from the color-killer circuit in amplifier No. 1 acts upon amplifier No. 2 to greatly reduce its gain.

The output from amplifier No. 2 (Terminal 14) is applied, through a filtering network, to the demodulator input (Terminal 13). The demodulator also receives the R-Y and B-Y demodulation subcarrier signals (Terminals 7 and 8) from the oscillator output of the chroma signal processor. The R-Y and B-Y demodulators and the matrix network contained in the demodulator section of the CA3121E reconstruct the G-Y signal to achieve the R-Y, G-Y, and B-Y color difference signals. These high-level outputs signals with low impedance outputs are suitable for driving high-level R, G, B output amplifiers. Internal capacitors are included on each output to filter out unwanted harmonics. For additional operating information and signal waveforms, refer to Television Chroma System (utilizing RCA-CA3070, CA3071, CA3072), File No. 468.

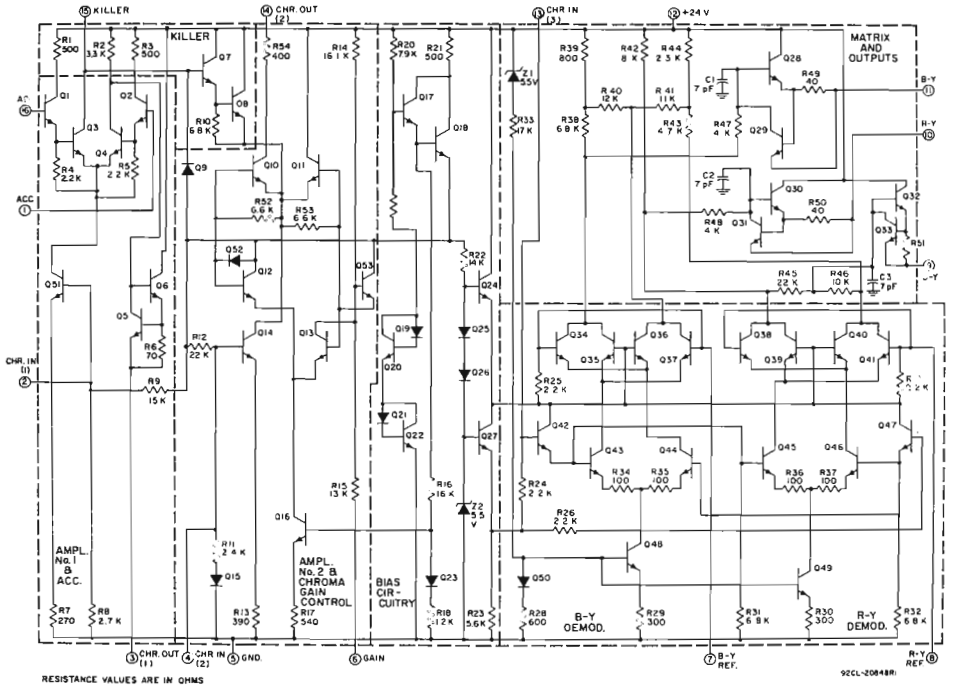


Fig. 2 – Schematic diagram of the CA3121E.

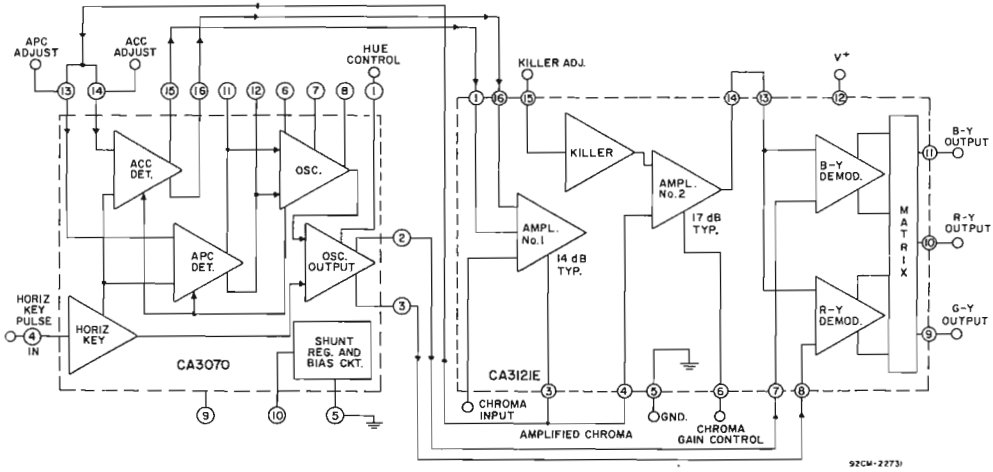


Fig. 3 – Simplified functional diagram of a two-package TV chroma system utilizing the CA3121E and CA3070.

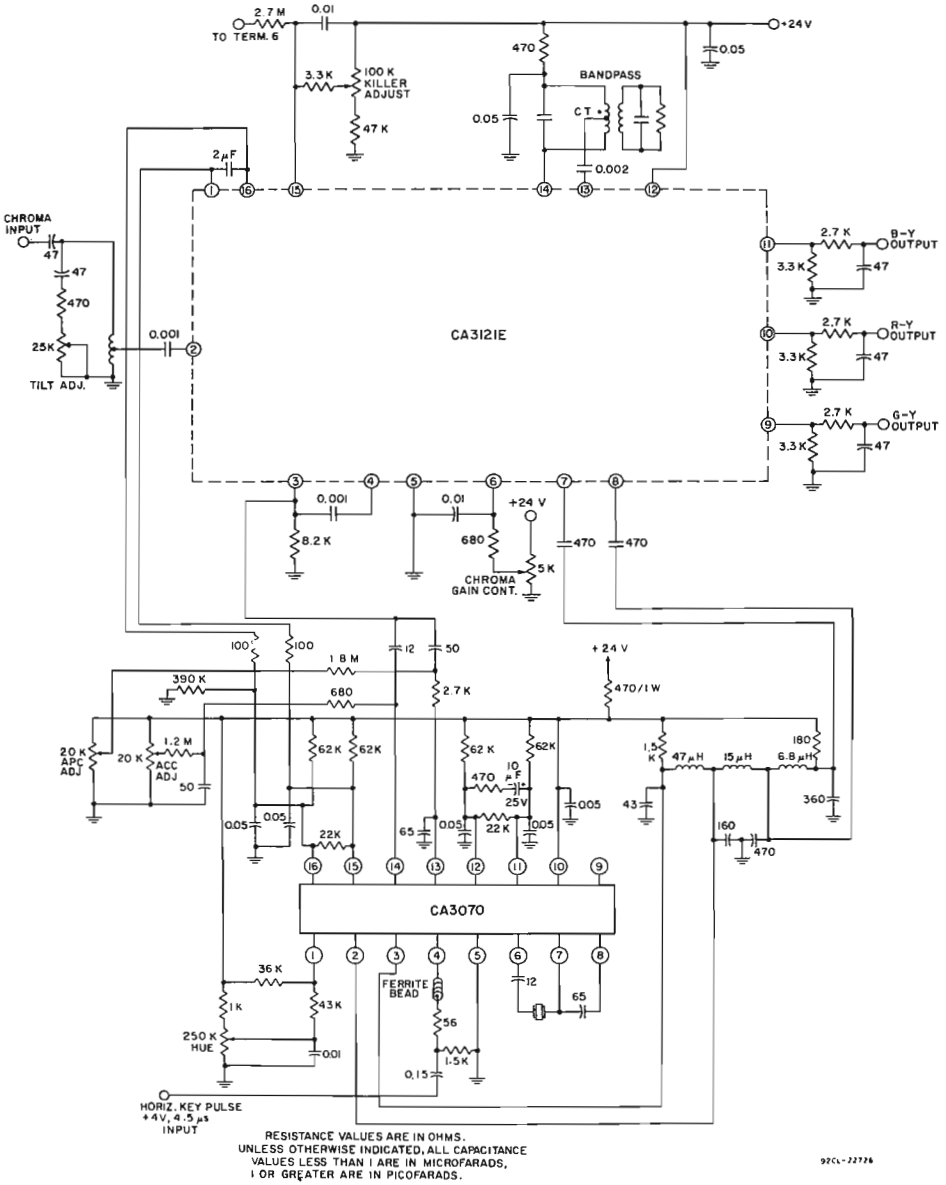


Fig. 4 — Outboard circuitry of a typical two-package chroma system for color-TV receivers utilizing the CA3121E and CA3070.

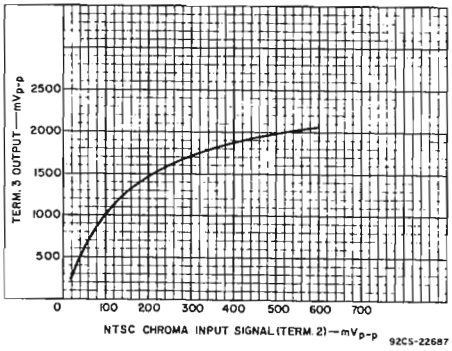


Fig. 5 — Typical ACC plot for the CA3121E when used with the CA3070.

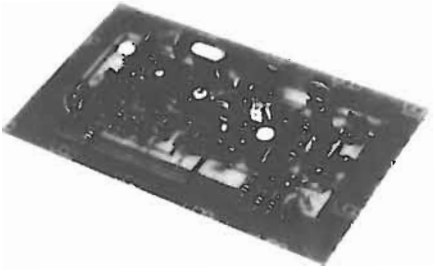


Fig.6 — Photograph of the component side of the circuit board (4 in. x 7 in.) of the two-package chroma system utilizing the CA3121E and CA3070.

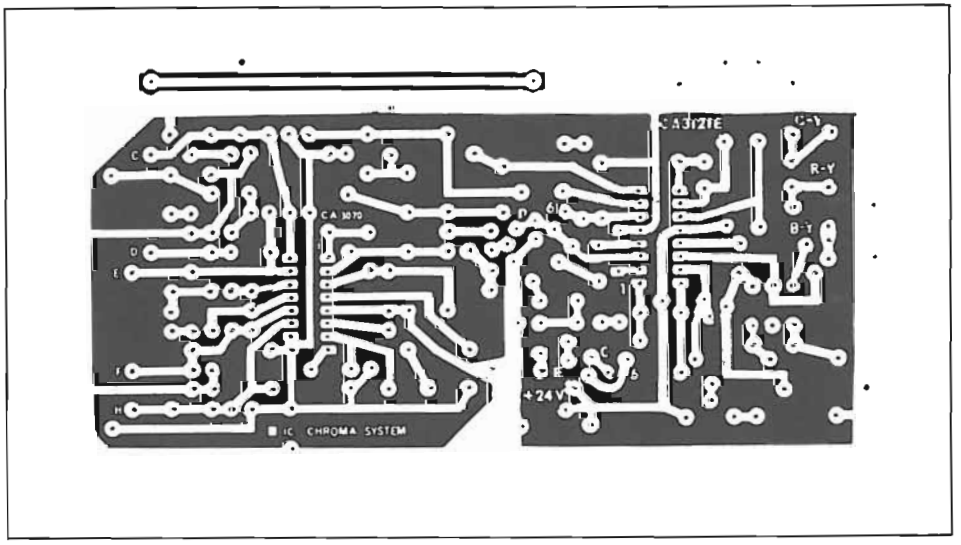


Fig.7 — Photograph of the foil side of the circuit board (4 in. x 7 in.) of the two-package chroma system utilizing the CA3121E and CA3070.

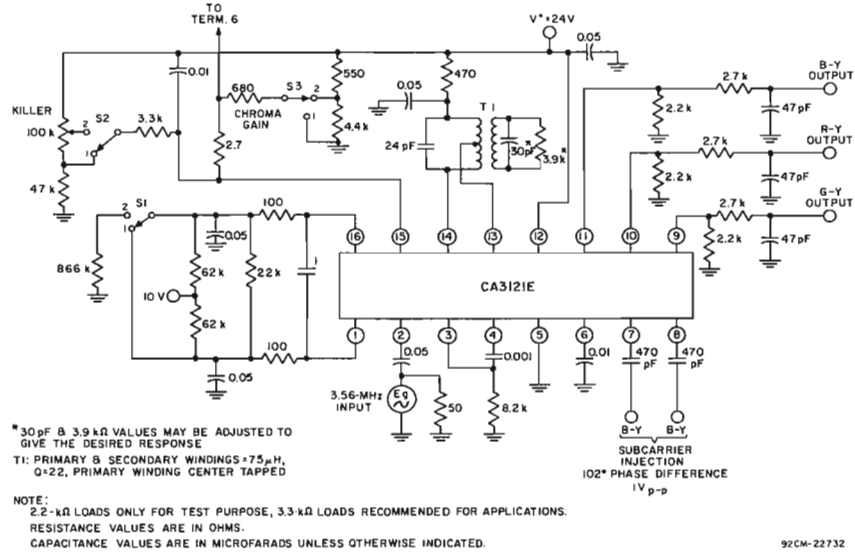


Fig. 8 — Typical characteristics test circuit for the CA3121E.

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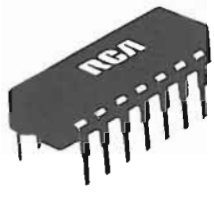
Monolithic Silicon

CA3123E



14-Lead Dual-in-Line Plastic Package

H-1517

AM Radio Receiver Subsystem

Includes RF Amplifier, IF Amplifier, Mixer, Oscillator, AGC Detector, and Voltage Regulator

Features:

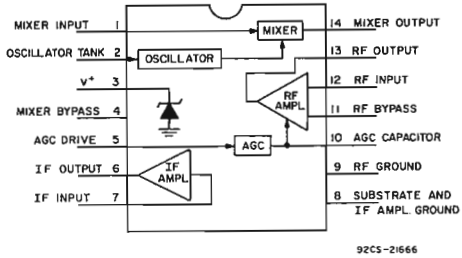
- Low-noise, low-R_b' rf stage in cascode connection — eliminates Miller-Effect regeneration and allows controlled power rise by the choice of external components
- Mixer-oscillator stage with internal feedback — eliminates need for tapped or multi-winding oscillator coils
- Cascode if amplifier with controlled output impedance and negligible Miller Effect — eliminates regeneretion and selectivity skewing
- Frequency-counter AGC circuit — allows control of AGC response by selection of the coupling capacitor
- Integral regulation with built-in surge protection
- Separately accessible amplifiers

The CA3123E* is a monolithic silicon integrated circuit that provides an rf amplifier, if amplifier, mixer, oscillator, AGC detector, and voltage regulator on a single chip. It is intended for use in super-heterodyne AM radio receiver applications particularly in automobiles. The CA3123E is supplied in a 14-lead dual-in-line plastic package and operates over the temperature range of −55° to 125°C.

* Formerly RCA Dev. No. TA6155

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:	
At Terminal No. 3 (V^+)	9 V
At Terminal No. 6 (IF Output)	40 V
At Terminal No. 13 (RF Output)	20 V
At Terminal No. 14 (Mixer Output)	20 V
DC CURRENT:	
Into Terminal No. 3 (V^+)	35 mA
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16" ± 1/3" (1.59 mm ± 0.79 mm) from case for 10 s max.	265°C



Terminal assignment diagram.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Static Characteristics In Circuit of Fig. 3						
DC Voltage:						
At Terminals 1, 4	V_1, V_4			4.7		V
At Terminals 2, 3, 14	V_2, V_3, V_{14}			6.8		V
At Terminal 5	V_5			0.25		V
At Terminal 6	V_6			12		V
At Terminal 7	V_7			0.76		V
At Terminals 8, 9	V_8, V_9			0		V
At Terminals 10, 11	V_{10}, V_{11}			0.71		V
At Terminal 12	V_{12}			0.71		V
At Terminal 13	V_{13}			4.0		V
DC Current:						
Into Terminals 1, 4, 5, 7 8, 9, 10, 11, 12	$I_1, I_4, I_5, I_7, I_8, I_9, I_{10}, I_{11}, I_{12}$			0		mA
Into Terminal 2	I_2			1.2		mA
Into Terminal 3	I_3			15		mA
Into Terminal 6	I_6			4.3		mA
Into Terminal 13	I_{13}			4.5		mA
Into Terminal 14	I_{14}			0.170		mA
Performance Characteristics In Circuit of Fig. 3						
Sensitivity		Input Signal to Dummy Antenna at f_{IN}=1 MHz, 30% AM Modulation at f_{MOD}=400 Hz, for 11 mV output at V_O	–	2.3	5	μV
Signal-to-Noise Ratio	S/N	Ratio of Output at V_O with Modulation ON and then OFF, Input Signal=100 μV, 30% AM Modulation at f_{MOD}=400 Hz	34	43	–	dB
Overload Distortion		Input Signal set at 1 MHz, 90% AM Modulation, Distortion at V_O must be $\leq$ 10%	160000	400000	–	μV

Dynamic Characteristics For Indicated Stages In Circuit of Fig. 3

Stage	Parallel Capacitance Input pF	Parallel Capacitance Output pF	Parallel Resistance Input Ω	Parallel Resistance Output Ω	Transconductance μmhos
RF Amplifier	80	6	750	2×10^6 min.	140000
IF Amplifier	35	3.5	950	10^4	80000
Mixer	6	2	2000	2×10^6 min.	2500 (Mixer) 3000 (Amplifier)

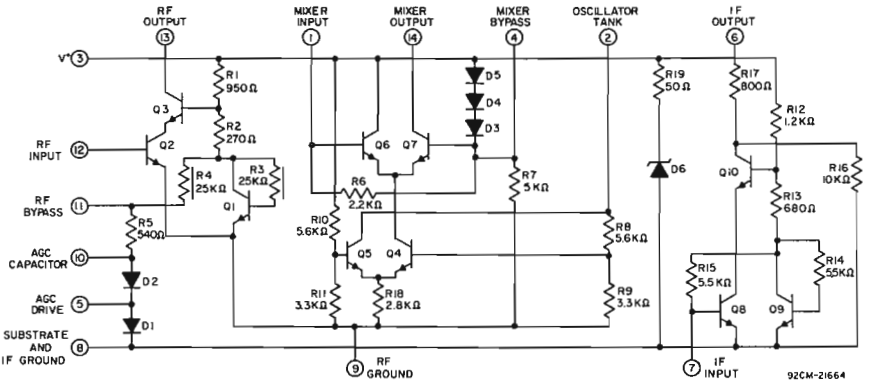
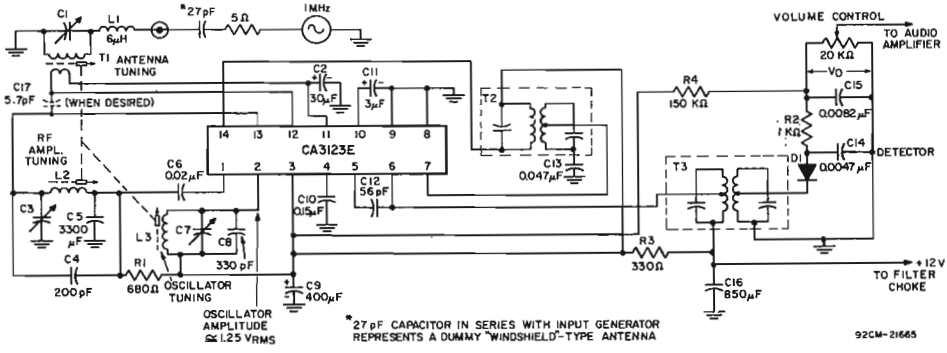


Fig. 2– Schematic diagram of CA3123E.



Transformer	Symbol	Frequency	Inductance μh (≈)	Capacitance pF (≈)	Q (≈)	Total Turns To Tap Turns Ratio	Coupling
First IF:							
Primary	T_2	262 kHz	2840	130	60	none	
Secondary			2840	130	60	or 30:1 / 31:1	critical ≈0.017 ≈1/Q
Second IF:							
Primary	T_3	262 kHz	2840	130	60	8.5:1	–
Secondary			2840	130	60	8.5:1	critical ≈0.017 ≈1/Q
Antenna:							
Primary	T_1	1 MHz	195	$(C_1)-130$	65		
Secondary		Adjusted to an impedance of 75 Ω with primary resonant at 1 MHz. Coupling should be as tight as practical. Wire should be wound around end of coil away from tuning core.					
Coils	L_1	7.9 MHz	6		50		
	L_2	1 MHz	55		50		
	L_3	1.262 MHz	41		40		

Fig. 3– Schematic diagram of AM radio receiver using CA3123E.

TYPICAL CHARACTERISTICS

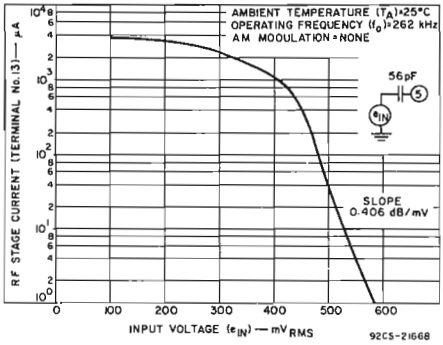


Fig.4 – Control of RF stage by signal into Terminal No.5.

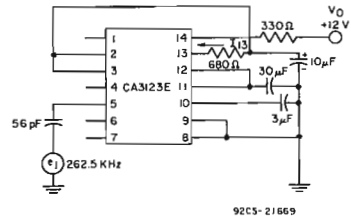


Fig.5 – Test circuit for Fig. 4.

PERFORMANCE CHARACTERISTICS IN CIRCUIT OF FIG. 3

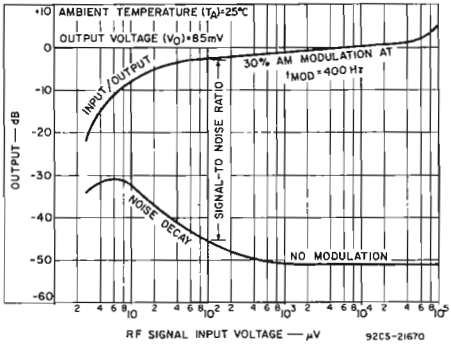


Fig.6 – Signal-to-noise performance.

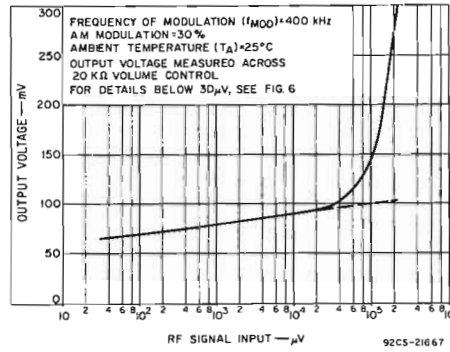


Fig.7 – AGC curve showing voltage rise (controlled by external capacitance of 5.7 pF: C_{17}, Fig.3).

Change in slope in the vicinity of 40000 μV signal input voltage is the result of the use of C_{17} (5.7 pF) in Fig.3. The dotted curve indicates expected performance if $C_{17} = 0$.

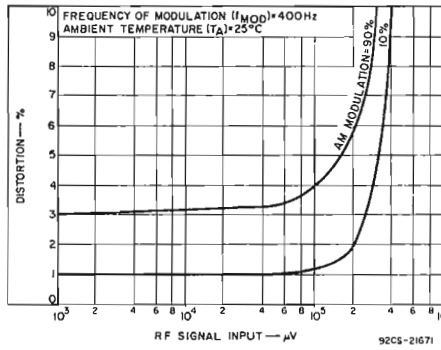


Fig.8 – Overload response.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3125E

14-Lead Dual-In-Line Plastic Package

H-1517

Television Chroma Demodulator

Features:

- Luminance input
- Blanking control input
- Three separate demodulators with independent phase control
- Low output offset voltage ..... 0.4 V

RCA-CA3125E is a monolithic silicon integrated-circuit chroma demodulator having three separate demodulators with independent phase control. It is designed to function compatibly with the CA1398E IC Chroma Processor as well as other commercially available Chroma Processors in R-G-B Systems of color-TV receivers. Fig. 2 shows a functional block diagram of a 2-package TV Chroma System incorporating the CA3125E and CA1398E. The CA3125E is supplied in a 14-lead dual-in-line plastic package.

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^\circ C$

SUPPLY VOLTAGE	25 V
SUPPLY CURRENT	20 mA
AMBIENT-TEMPERATURE RANGE:	
Operating	−40°C to +85°C
Storage	−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

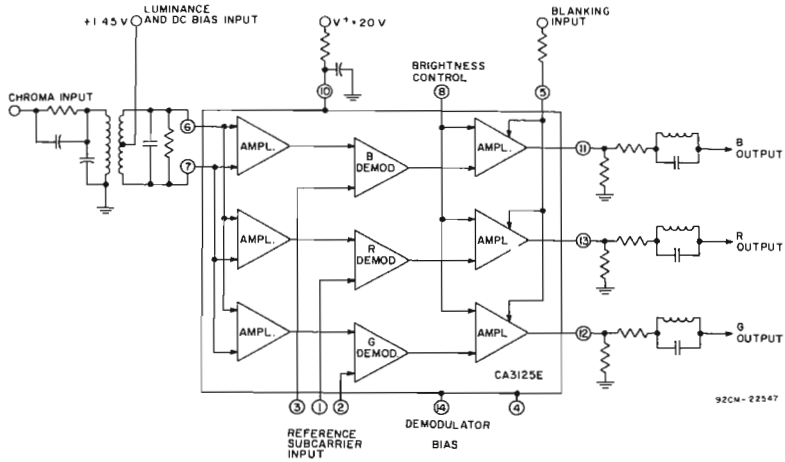


Fig. 1 — Functional block diagram of the CA3125E.

TYPICAL STATIC CHARACTERISTICS AT $T_A = 25°C$, $V^+ = +20$ VOLTS

SUPPLY CURRENT ..... 9.6 mA

BRIGHTNESS CONTROL VOLTAGE:

Measured with 8 volts at Terminals 11, 12, and 13 ..... 1.4 V

MAX. OUTPUT DIFFERENCE VOLTAGE:

Measured between any two of Terminals 11, 12, and 13 ..... ±0.4 V

MAXIMUM DC DETECTOR UNBALANCE VOLTAGE:

DC voltage shift on Terminals 11, 12, and 13 when Terminals 1, 2, and 3 are alternately biased 0.5 volt positive, then negative with reference to Terminal 14 ..... +150 mV

TYPICAL DYNAMIC CHARACTERISTICS AT $T_A = 25°C$, $V^+ = +20$ volts

BLUE CHROMA GAIN:

Peak-to-peak voltage at Terminal 11 with 1.0 volt peak-to-peak applied differentially between Terminals 6 and 7, and with a subcarrier injection voltage of 1 volt peak-to-peak 7.36 Vp-p

RED GAIN RATIO:

$$\frac{\text{Peak-to-peak voltage at Terminal 13}}{\text{Peak-to-peak voltage at Terminal 11}} \times 100 \text{ ..... } 100\%$$

GREEN GAIN RATIO:

$$\frac{\text{Peak-to-peak voltage at Terminal 12}}{\text{Peak-to-peak voltage at Terminal 11}} \times 100 \text{ ..... } 30\%$$

LUMINANCE GAIN:

Peak-to-peak voltage measured at Terminals 11, 12, and 13, with a peak-to-peak voltage of 0.1 volt applied to Terminals 6 and 7 (common mode), and with no subcarrier injection ..... 0.7 Vp-p

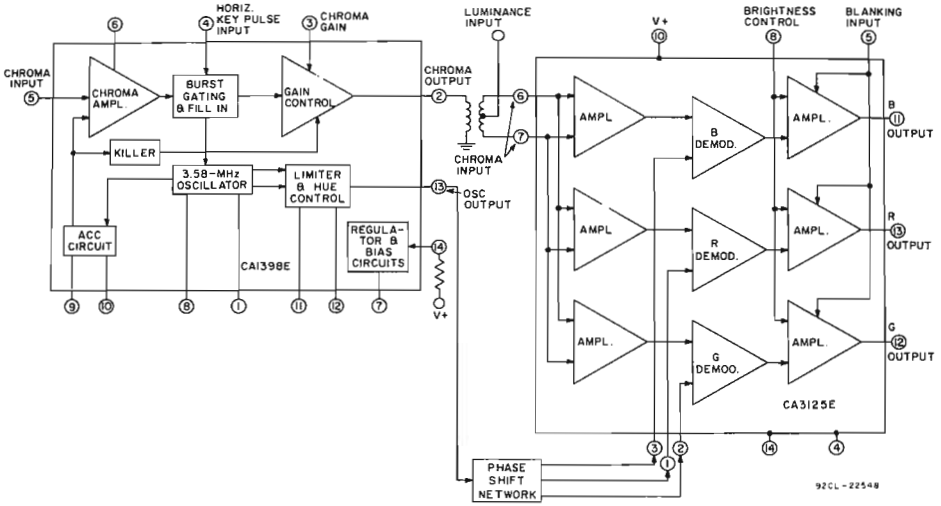


Fig. 2 – TV chroma system functional block diagram.

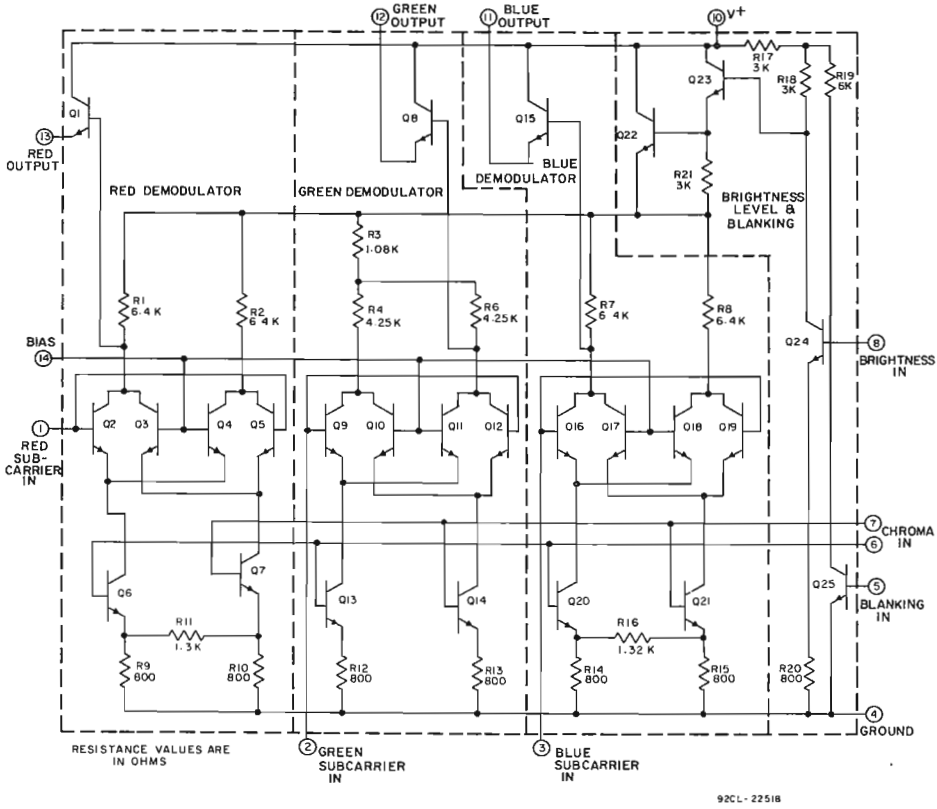


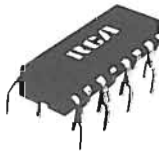
Fig. 3 – Schematic diagram of the CA3125E.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3126Q



16-lead Quad-in-line plastic package

H 1706

TV Chroma Processor

Features:

- Phase-locked subcarrier regeneration utilizes sample-and-hold techniques
- Automatic chrominance control (ACC)/killer detector employs sample-and-hold techniques
- Supplementary ACC with an overload detector to prevent oversaturation of the picture tube
- Sinusoidal subcarrier output
- Keyed chroma output
- Emitter-follower buffered outputs for low output impedance
- Linear dc saturation control
- Internal zener-regulated reference potentials

RCA-CA3126Q is a monolithic silicon integrated circuit designed for chroma processing applications in color TV receivers. It is compatible with the CA3067 chroma demodulator as well as other chroma demodulators.

- Only the initial crystal filter tuning is required. . . no killer or ACC adjustments required at any time
- Few external components required
- Compensation for temperature and supply variations
- All terminals protected against short circuits

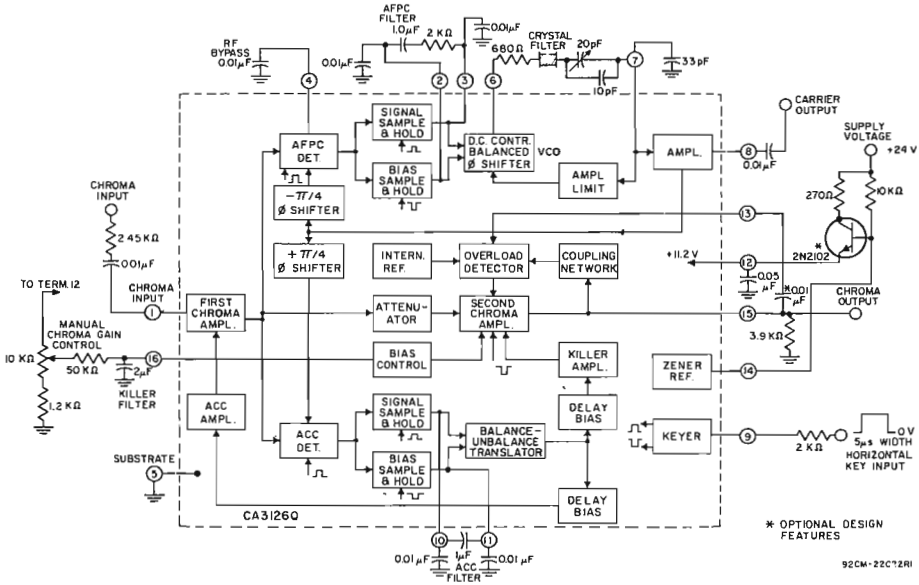


Fig. 1—Block diagram of CA3126Q TV Chroma Processor.

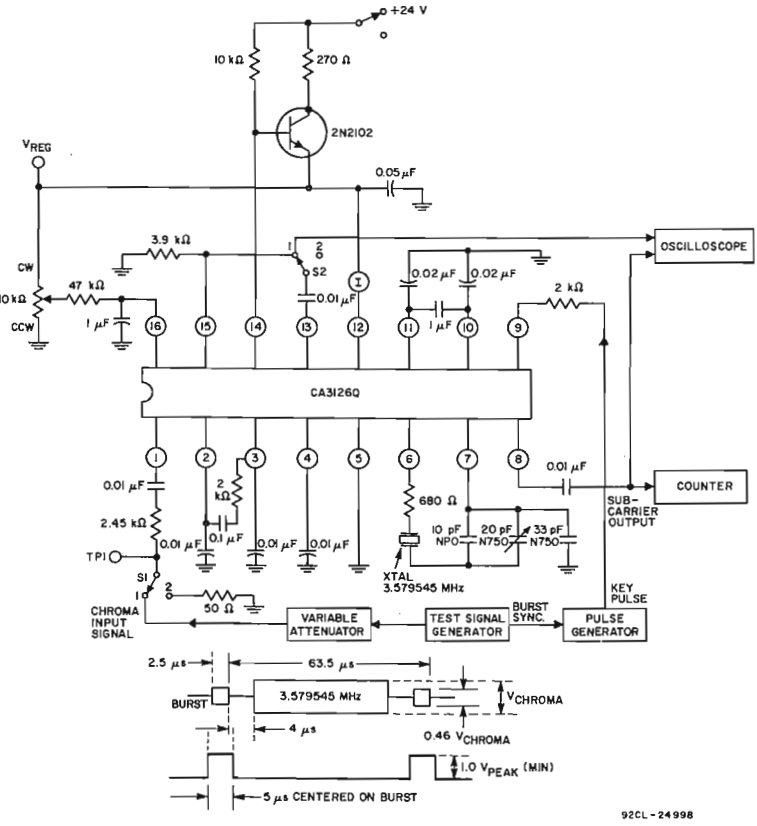


Fig. 2—Test circuit for CA3126Q.

CIRCUIT DESCRIPTION

The following paragraphs briefly describe the circuit operation of the CA3126Q (shown in Figs. 1 and 3). A detailed description of the operation of various portions of the CA3126Q is given in ICAN-6247, "Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Techniques".

The chroma input is applied to Terminal 1 through the desired band-shaping network. A 2,450-ohm resistor should be placed in series with Terminal 1 to minimize oscillator pickup in the first chroma amplifier. This amplifier supplies signals to the second chroma amplifier and to the ACC and AFPC detectors. The first chroma amplifier is gain-controlled by the ACC amplifier.

A horizontal keying pulse is applied to Terminal 9. This pulse must be present to ensure proper operation of the oscillator circuit. The subcarrier burst is sampled during the keying interval in the AFPC detector. The error voltage, produced at Terminal 2 and proportional to the burst phase, is compared to the quiescent bias voltage at Terminal 3 by the sample-and-hold circuitry. This "compared" voltage controls the phase-shifting network in the phase-locked loop. The operation of the AFPC loop is independent of any external adjustments or voltages except for an initial capacitor adjustment to set the free-running frequency.

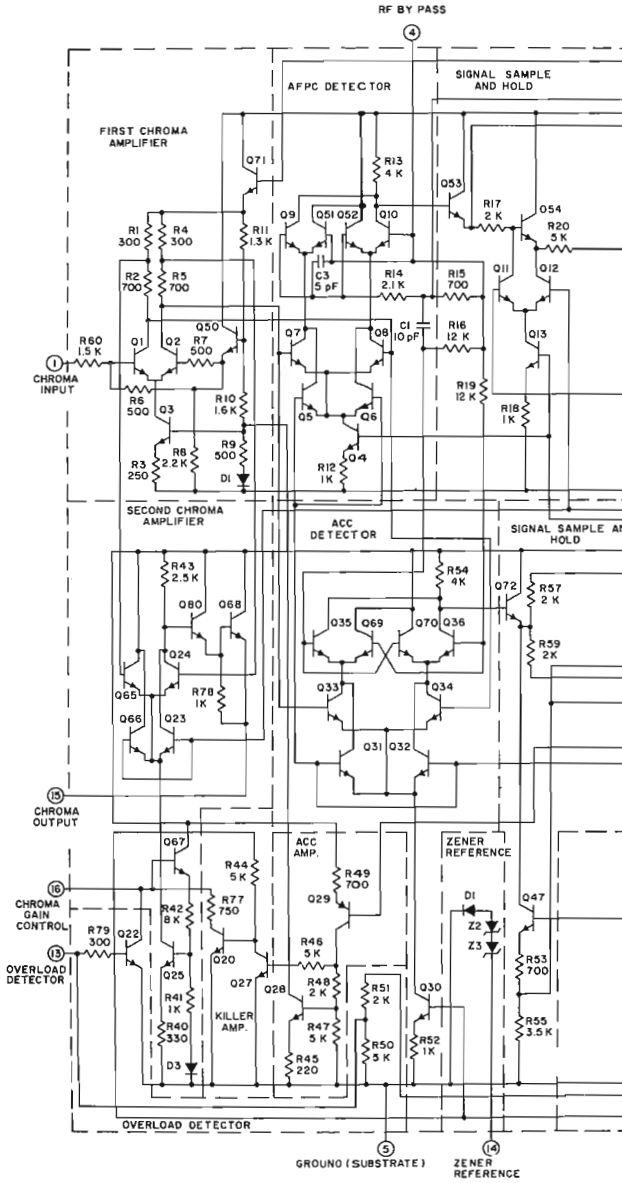


Fig. 3—Schematic diagram of the CA3126Q.

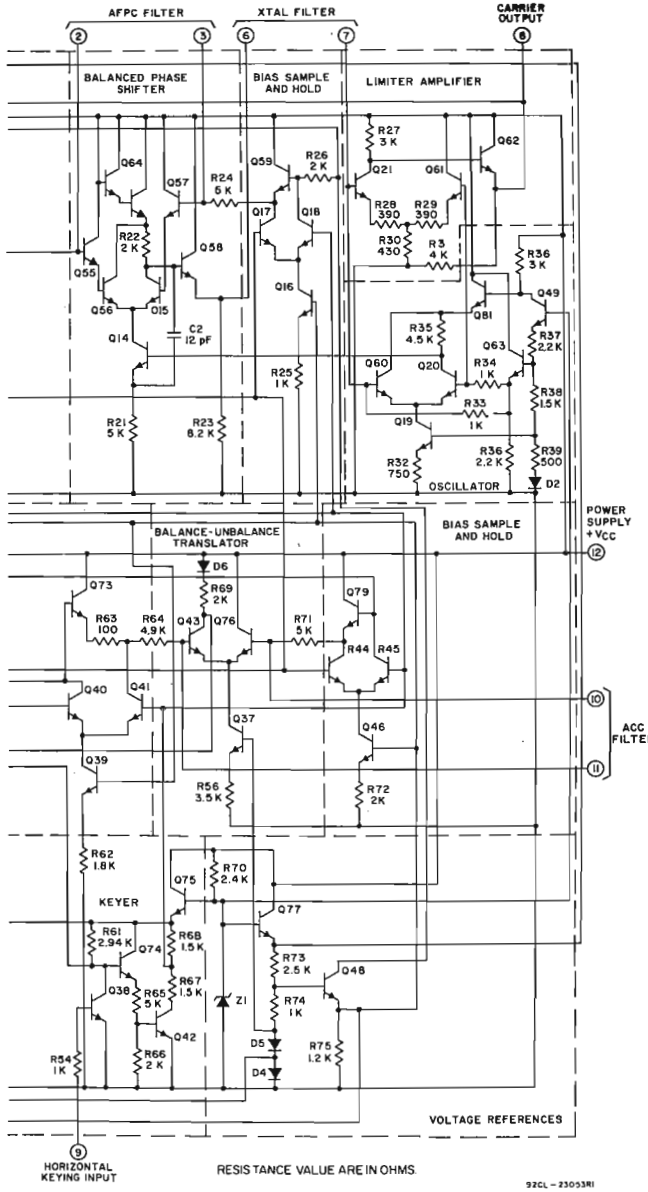


Fig. 3—Schematic diagram of the CA3126Q (cont'd).

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DEVICE DISSIPATION:
- Up to $T_A = 55^oC$ ..... 750 mW
- Above $T_A = 55^oC$ ..... derate linearly 7.9 mW/^oC

DC SUPPLY VOLTAGE (Across Terms. 5 and 12)▲ ..... 13.2 V

DC CURRENT:
- Into Term. 12 ..... 38 mA
- Into Term. 14 ..... 20 mA

DC VOLTAGE (Terminal 9):
- Negative Rating ..... −5 V
- Positive Rating ..... 3 V

AMBIENT TEMPERATURE RANGE:
- Operating ..... −40 to +85^oC
- Storage ..... −65 to +150^oC

LEAD TEMPERATURE (During Soldering):
- At a distance not less than 1/32 in. (0.79 mm) from case for 10 seconds max. ..... +265^oC

▲This rating does not apply when using the internal zener reference in conjunction with an external pass transistor.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25^oC$, chroma control at maximum position for all characteristics tests except for chroma output test. For this test, control should be set at minimum position. Electrical characteristics referenced to test circuit, Fig.2.

CHARACTERISTIC	TERMINAL, MEASUREMENT, AND SYMBOL	SWITCH POS.		CHROMA INPUT	LIMITS			UNITS
		S1	S2	TP1	Min.	Typ.	Max.	
Static Characteristics								
Voltage Regulator	V_{12}	2	2	0	10.1	11.2	12.1	V
Supply Current	I_{12}	2	2	0	16	25	38	mA
Dynamic Characteristics (See Note 1)								
Pull-in Range*	V_8	*	2	0.5 V_{p-p}	±250	–	–	Hz
Oscillator Output	V_8	2	2	0	0.6	1.0	–	V_{p-p}
100% Chroma Output	V_{15}	1	2	0.5 V_{p-p}	1.4	2.7	–	V_{p-p}
Overload Detector	V_{15}	1	1	0.5 V_{p-p}	0.4	–	0.7	V_{p-p}
Minimum Chroma Output	V_{15}	1	2	0.5 V_{p-p}	–	–	20	mV_{p-p}
200% Chroma Output	V_{15}	1	2	1 V_{p-p}	70	100	140	% of 100% reading
20% Chroma Output	V_{15}	1	2	0.1 V_{p-p}	40	–	105	
Kill Level	V_{TP1}	1	2	vary	5	–	60	mV_{p-p}

Note 1: Except for pull-in range testing, tune oscillator trimmer capacitor for free-running frequency of 3.579545 MHz ± 10 Hz.
*Set Switch 1 to Position 2, detune oscillator ± 250 Hz, set Switch 1 to Position 1, and check for oscillator pull-in.

The regenerated oscillator signal at Terminal 8 is applied internally to the AFPC and ACC detectors through +45- and −45-degree phase-shifter networks to establish the proper phase relationship for these detectors. The ACC detector, which also samples the burst during the keying interval, produces a correction voltage proportional to the burst amplitude. The correction voltage is compared to the quiescent bias level using sample-and-hold circuitry similar to that used in the AFPC portion of the circuit. The "compared" voltage is applied internally to the ACC amplifier and killer amplifier. Because the amplifier gains and killer threshold are determined by the ratios of the internal resistors, these functions are independent of external voltages or controls.

The attenuated chroma signal is fed to the second chroma amplifier, where the burst is removed by keyer action. The killer amplifier, the chroma gain control, and the overload detector control the action of the second chroma amplifier, whose gain is proportional to the dc voltage at Terminal 16. The overload detector (Terminal 13) receives a sample of the chroma output (Terminal 15) and detects the peak of the signal. The detected voltage is stored in an external capacitor connected to Terminal 16. This stored voltage on Terminal 16 affects the gain of the second chroma in the same manner as the chroma gain control.

APPLICATIONS INFORMATION

General Considerations

The block diagram shown in Fig. 1 is typical of the type of circuit used in the practical application of the CA3126Q. Several items are critical for proper operation of the circuit.

1. A series resistor of approximately 2,450 ohms (or high source impedance) must be used at the chroma input, Terminal 1. This high impedance minimizes pickup of unbalanced currents, particularly of the subcarrier oscillator signal.
2. When the overload detector is used, a large resistor (nominally 47,000 ohms) must be placed in series with Terminal 16 to set the required RC time constant. The same RC network series serves to set the killer time constant.
3. The setting of the free-running oscillator frequency requires the presence of the keying pulse. The free-running frequency will be erroneous if Terminal 1 is dc shorted during the setting operation because of the dc offset voltage introduced to the AFPC detector.
4. Care must be taken in PC board designs to provide reasonable isolation between the oscillator portion of the circuit (Terminals 6, 7, and 8) and the chroma input (Terminal 1).

Overload Detector

The overload detector accomplishes two purposes:

1. It prevents oversaturation due to low burst-to-chroma ratios.
2. It prevents overload conditions due to noise.

Both of these conditions are discussed in more detail in ICAN-6247. The extent to which the overload detector is used depends upon the individual receiver design goals. If greater than 0.5-volt peak-to-peak output is desired, the chroma output at Terminal 15 can be tapped to yield any desired degree of overload detector action.

Chroma Gain Control

The chroma gain control operates by varying the base bias on current source transistor Q25. To ensure proper temperature tracking of the chroma gain control, it is essential that the control be operated from a supply source derived from the reference voltage at Terminal 12. Because the control operates from a current source, chroma gain is much more predictable and far less temperature sensitive than controls that steer current by means of a differential amplifier. The typical chroma gain characteristic for the CA3126Q is shown in Fig. 4.

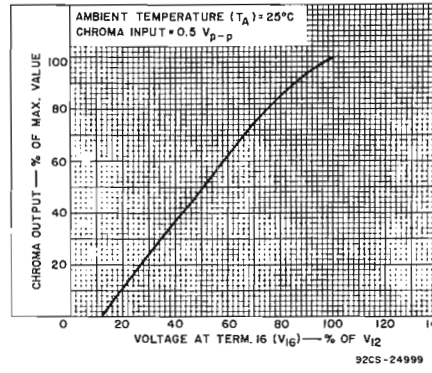


Fig. 4—Chroma gain control.

Subcarrier Regenerator Oscillator

The oscillator filter consists of a 3.579545-MHz crystal, a 680-ohm resistor, and a 10-pF capacitor connected in series across Terminals 6 and 7. A 33-pF capacitor, shunt connected from Terminal 7 to ground, rolls off higher-order harmonics, thereby preventing oscillation at the crystal third-harmonic frequency. A curve of the typical static phase error as a function of the free-running oscillator frequency is shown in Fig. 5. It should be noted that the slope of the curve determines the dc gain of the phase-locked loop, i.e., 40 Hz per degree.

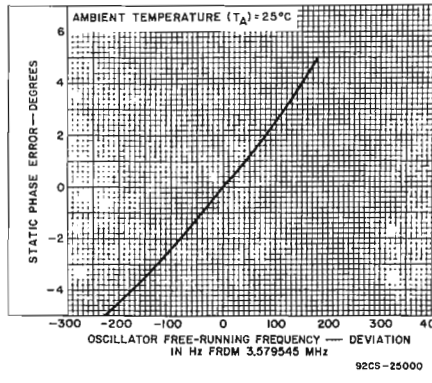


Fig. 5—Static phase error.

Thermal Considerations

The circuit of the CA3126Q is thermally compensated to achieve the optimal operating characteristics over the normal operating temperature range of TV receivers. Figs. 6 and 7 show the oscillator- and chroma-output amplitudes and phases as a function of temperature (Terminals 8 and 15), respectively. Both the oscillator- and chroma-output amplitudes and phases are measured relative to the chroma-input phase. The performance of the oscillator free-running frequency as a function of temperature is shown in Fig. 8. All the temperature plots are characteristic of the test circuit with the indicated component types and values given in Fig. 2.

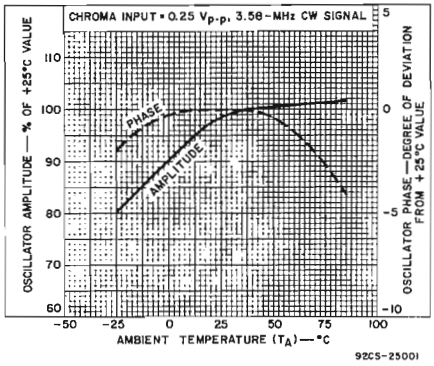


Fig. 6—Amplitude and phase variations of oscillator output vs. temperature.

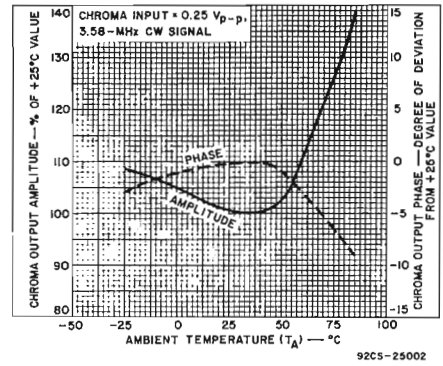


Fig. 7—Amplitude and phase variations of chroma output vs. temperature.

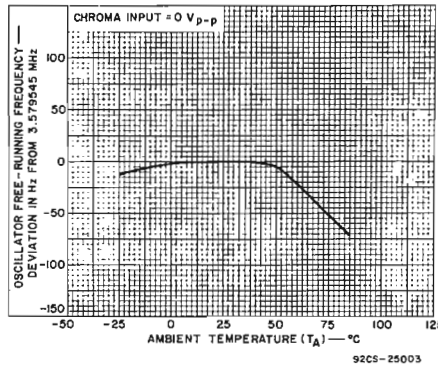


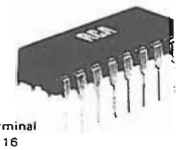
Fig. 8—Variation of oscillator free-running frequency vs. temperature.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3127E



16-Lead Dual-In-Line Plastic Package H-1622

High-Frequency N-P-N Transistor Array

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- Gain-Bandwidth Product (f_T) ≥ 1 GHz
- Power Gain = 30 dB (typ.) at 100 MHz
- Noise Figure = 3.5 dB (typ.) at 100 MHz
- Five independent transistors on a common substrate

Applications:

- VHF amplifiers
- VHF mixers
- Multifunction combinations – RF/mixer/oscillator
- IF Converter
- IF amplifiers
- Sense amplifiers
- Synthesizers
- Synchronous detectors
- Cascade amplifiers

RCA-CA3127E* consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1 GHz, making the CA3127E useful from dc to 500 MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127E provides close electrical and thermal matching of the five transistors.

The CA3127E is supplied in a 16-lead dual-in-line plastic package and operates over the full military temperature range of −55 to +125°C.

* Formerly RCA Dev. No. TA6206.

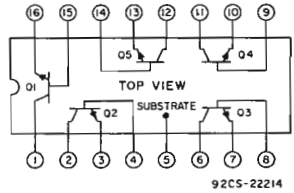


Fig. 1– Schematic diagram of CA3127E.

MAXIMUM RATINGS, *Absolute-Maximum Values, at T_A = 25°C*

POWER DISSIPATION, P_D:
- Any one transistor ..... 85 mW
- Total Package:
- For T_A up to 75°C ..... 425 mW
- For T_A > 75°C Derate Linearly at ..... 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... −55 to +125°C
- Storage ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

The following ratings apply for each transistor in the device.

Collector-to-Emitter Voltage, V_{CEO} ..... 15 V

Collector-to-Base Voltage, V_{CBO} ..... 20 V

Collector-to-Substrate Voltage, V_{CIO}* ..... 20 V

Collector Current, I_C ..... 20 mA

*The collector of each transistor of the CA3127E is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A$, $I_E = 0$	20	32	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{C1} = 10\ \mu A$, $I_B = 0$, $I_E = 0$	20	60	–	V
Emitter-to-Base Breakdown Voltage*	$V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$	4	5.7	–	V
Collector-Cutoff-Current	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	–	–	0.5	μA
Collector-Cutoff-Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	–	–	40	nA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 6$ V, $I_C = 5$ mA	35	88	–	
		$V_{CE} = 6$ V, $I_C = 1$ mA	40	90	–	
		$V_{CE} = 6$ V, $I_C = 0.1$ mA	35	85	–	
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6$ V, $I_C = 5$ mA	0.71	0.81	0.91	V
		$V_{CE} = 6$ V, $I_C = 1$ mA	0.66	0.76	0.86	
		$V_{CE} = 6$ V, $I_C = 0.1$ mA	0.60	0.70	0.80	
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10$ mA, $I_B = 1$ mA	–	0.26	0.50	V
Magnitude of Difference in V_{BE}	$\lvert\Delta V_{BE}\rvert$	Q_1 & Q_2 Matched	–	0.5	5	mV
Magnitude of Difference in I_B	$\lvert\Delta I_B\rvert$	$V_{CE} = 6$V, $I_C = 1$ mA	–	0.2	3	μA

*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible capacitive or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zenar current should be less than 10 mA.

DYNAMIC CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Fig. No.	LIMITS			UNITS
				Min.	Typ.	Max.	
I/F Noise Figure	NF	f = 100 kHz, $R_S = 500\ \Omega$, $I_C = 1$ mA	2	–	1.8	–	dB
Gain-Bandwidth Product	f_T	$V_{CE} = 6$ V, $I_C = 5$ mA	4	–	1.15	–	GHz
Collector-to-Base Capacitance	C_{CB}	$V_{CB} = 6$ V, f = 1 MHz	5	–	See	–	pF
Collector-to-Substrate Capacitance	C_{CI}	$V_{CI} = 6$ V, f = 1 MHz	5	–	Fig.	–	pF
Emitter-to-Base Capacitance	C_{EB}	$V_{BE} = 4$ V, f = 1 MHz	5	–	5	–	pF
Voltage Gain	A	$V_{CE} = 6$ V, f = 10 MHz, $R_L = 1\ K\Omega$, $I_C = 1$ mA	6, 18	–	28	–	dB
Power Gain	G_p	Cascode Configuration f = 100 MHz, $V^+ = 12$ V	19, 20	27	30	–	dB
Noise Figure	NF	$I_C = 1$ mA	19, 20	–	3.5	–	dB
Input Resistance	$1/g_{11}$	Common-Emitter	10	–	400	–	Ω
Output Resistance	$1/g_{22}$	Configuration	12	–	4.6	–	$k\Omega$
Input Capacitance	C_{11}	$V_{CE} = 6$ V	10	–	3.7	–	pF
Output Capacitance	C_{22}	$I_C = 1$ mA	12	–	2	–	pF
Magnitude of Forward Transadmittance	$\lvert Y_{21}\rvert$	f = 200 MHz	14, 15	–	24	–	mmho

CHARACTERISTICS CURVES
COMMON-EMITTER CONFIGURATION

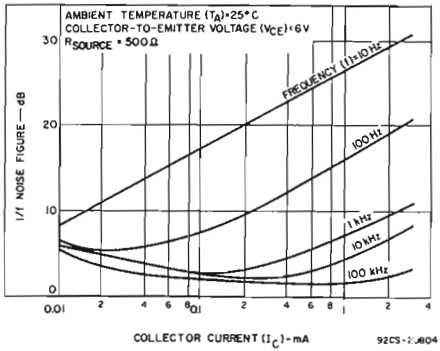


Fig. 2 – 1/f noise figure vs. collector current at R_{SOURCE} = 500 Ω.

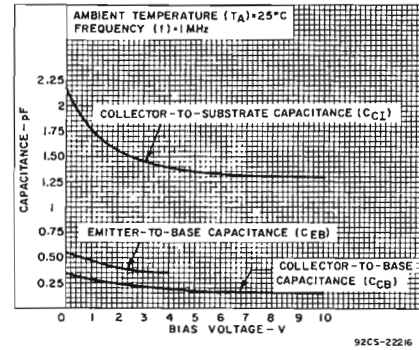


Fig. 5(a) – Capacitance vs. bias voltage for Q_2.

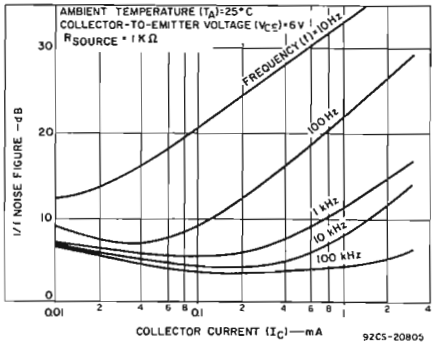


Fig. 3 – 1/f noise figure vs.collector current at R_{SOURCE} = 1 kΩ.

Transistor	Capacitance (pF)							
	C_{CB}		C_{CE}		C_{EB}		C_{CI}	
	Pkg.	Total	Pkg.	Total	Pkg.	Total	Pkg.	Total
Bias Voltage	–	6 V	–	6 V	–	4 V	–	6 V
Q1	0.025	0.190	0.090	0.125	0.385	0.610	0.475	1.68
Q2	0.015	0.170	0.225	0.265	0.130	0.360	0.085	1.36
Q3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q4	0.040	0.190	0.225	0.270	0.385	0.610	0.085	1.76
Q5	0.010	0.165	0.095	0.115	0.140	0.385	0.090	1.35

Fig. 5(b) – Typical capacitance values at f = 1 MHz. Three terminal measurement. Guard all terminals except those under test.

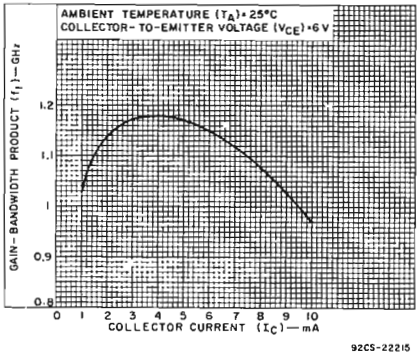


Fig. 4 – Gain-bandwidth product vs. collector current.

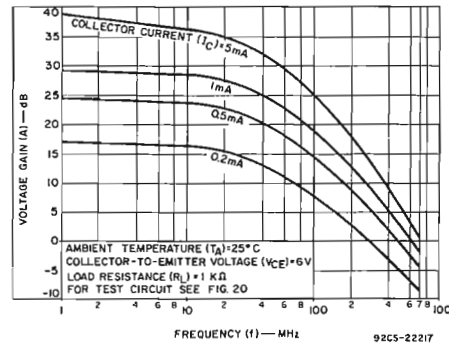


Fig. 6 – Voltage gain vs. frequency at R_L = 1 kΩ.

CHARACTERISTICS CURVES (Cont'd)
COMMON-EMITTER CONFIGURATION

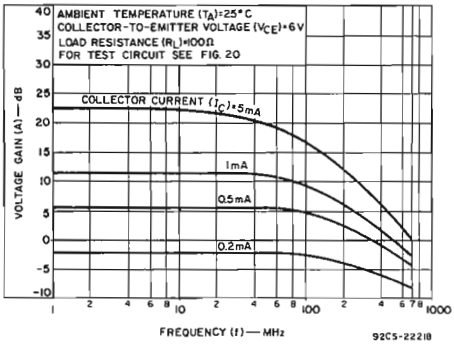


Fig. 7 – Voltage gain vs. frequency at R_L = 100 Ω.

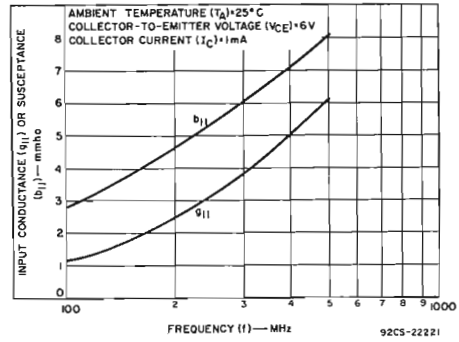


Fig. 10 – Input admittance (Y_{11}) vs. frequency.

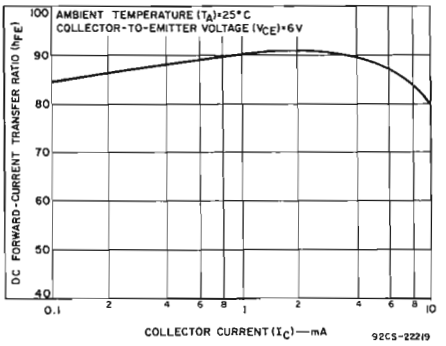


Fig. 8 – DC forward-current transfer ratio vs. collector current.

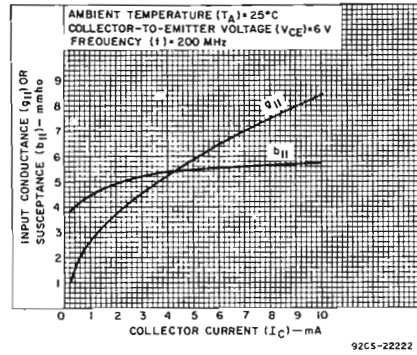


Fig. 11 – Input admittance (Y_{11}) vs. collector current.

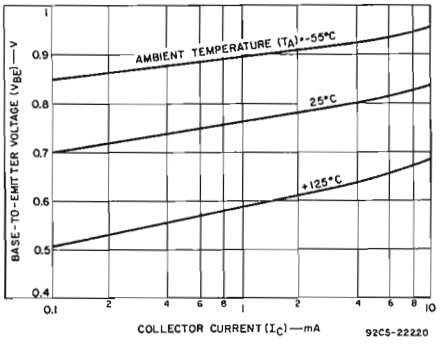


Fig. 9 – Base-to-emitter voltage vs. collector current.

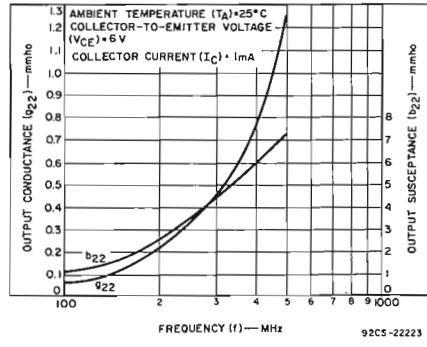


Fig. 12 – Output admittance (Y_{22}) vs. frequency.

CHARACTERISTICS CURVES (Cont'd)
COMMON-EMITTER CONFIGURATION

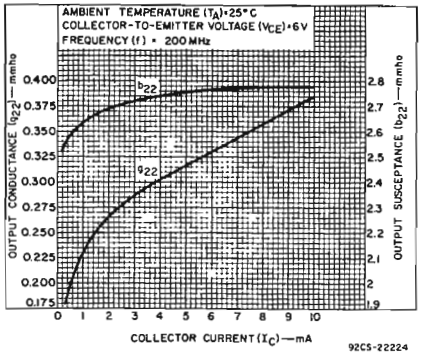


Fig. 13 – Output admittance (Y_{22}) vs. collector current.

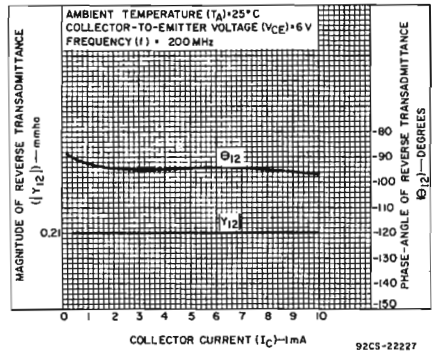


Fig. 16 – Reverse transadmittance (Y_{12}) vs. collector current.

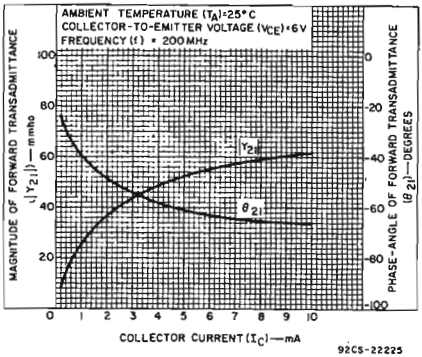


Fig. 14 – Forward transadmittance (Y_{21}) vs. collector current.

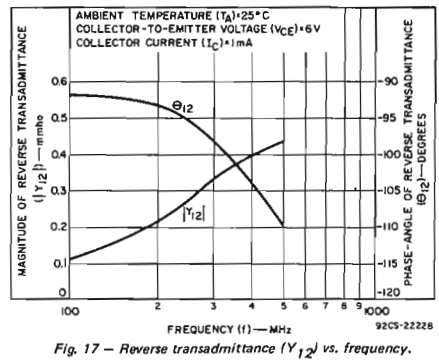


Fig. 17 – Reverse transadmittance (Y_{12}) vs. frequency.

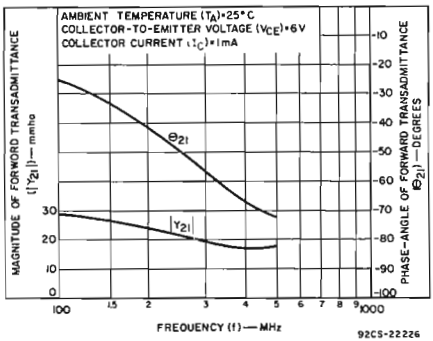


Fig. 15 – Forward transadmittance (Y_{21}) vs. frequency.

TEST CIRCUITS

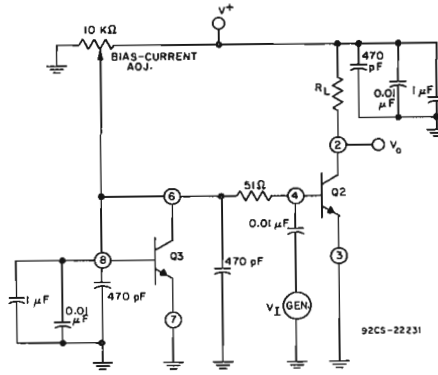
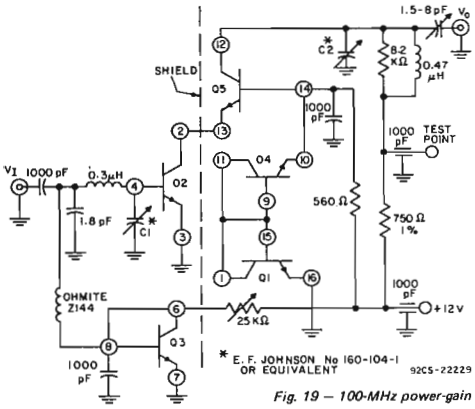


Fig. 18 – Voltage-gain test circuit using current-mirror biasing for Q_2.

TEST CIRCUITS (Cont'd)



This circuit was chosen because it conveneietly represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

Fig. 19 — 100-MHz power-gain and noise-figure test circuit.

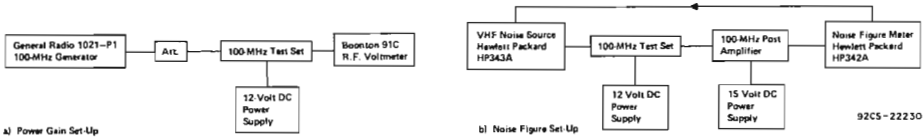


Fig. 20 — Block diagrams of power-gain and noise-figure test set-ups.

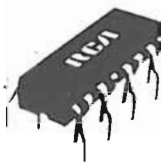
RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA3128Q

Preliminary Data



16-lead Quad-in-line plastic package

H-1706

TV Chroma Processor for PAL Systems

Features:

- Phase-locked subcarrier regeneration utilizes sample-and-hold techniques in the automatic frequency phase control (AFPC) servo loop
- Automatic chrominance control (ACC)/ killer detector employs sample-and-hold techniques
- Supplementary ACC with an overload detector to prevent oversaturation of the picture tube
- Sinusoidal subcarrier output
- Keyed chroma output
- Emitter-follower buffered outputs for low output impedance
- Linear dc saturation control
- PAL identification output

The RCA-CA3128Q is a monolithic silicon integrated circuit designed primarily for PAL chroma processing applications in color TV receivers. For a circuit description of the CA3128Q and an explanation of this device in PAL systems, refer to "A New Chroma Processing IC Using Sample -and-Hold Techniques" by L. A. Harwood (ST6144).

- Only the initial crystal filter tuning is required . . . no killer and ACC adjustments required at any time
- Few external components required
- Compensation for temperature and supply variations
- All terminals protected against short circuits

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25°C$

DC SUPPLY VOLTAGE (Between Terms. 12 and 5)	13.2	V
DC VOLTAGE (Term. 9):		
Positive Value	+3	V
Negative Value	−5	V
DEVICE DISSIPATION:		
Up to $T_A = 55°C$	750	mW
Above $T_A = 55°C$	derate linearly at 7.9	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING):		
At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

TYPICAL STATIC CHARACTERISTICS at $T_A = 25°C$:

DC Supply Current (I_{12}) with $V_{12} = 11.2$ V dc	25	mA

TYPICAL DYNAMIC CHARACTERISTICS at $T_A = 25°C$ with a Burst-to-Chroma Ratio of 46.5%:

100% Chroma Output Voltage at $V_{I\,(p\text{-}p)} = 0.5$ V	3.5	Vp-p
Oscillator-Level Output Voltage	1	Vp-p
Killer Threshold Input Voltage	0.018	Vp-p
Pull-in Frequency	500	Hz
PAL Identification Output Voltage	1	Vp-p

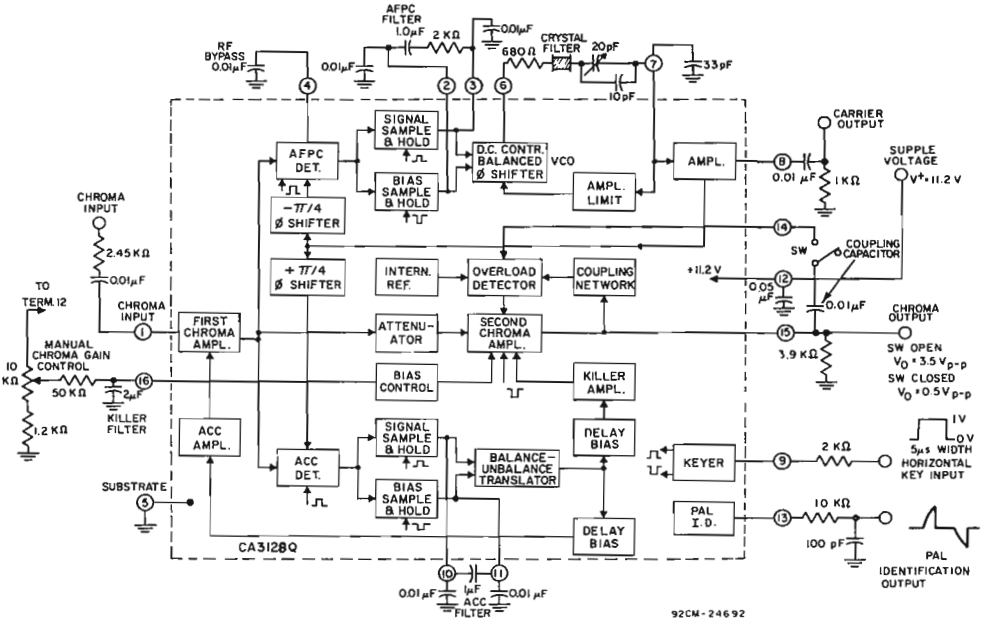


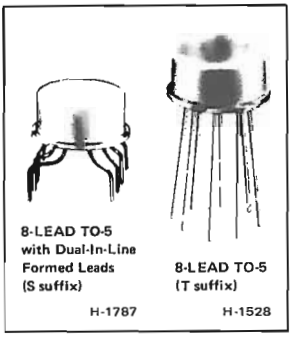
Fig. 1 — Block diagram of CA3128Q TV Chroma Processor.

RCA
Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3130BT, CA3130BS
CA3130AT, CA3130AS
CA3130T, CA3130S



8-LEAD TO-5 with Dual-In-Line Formed Leads (S suffix) H-1787

8-LEAD TO-5 (T suffix) H-1528

COS/MOS Operational Amplifiers

With MOS/FET Input

Features:

- MOS/FET input stage provides:
  very high Z_I = 1.5 TΩ (1.5 x 10^{12} Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  2 pA typ. at 5 V operation
- Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
- COS/MOS output stage permits signal swing to either (or both) supply rails

} Ideal for single-supply applications

- Low V_{IO}: 2 mV max. (CA3130B)
- Wide BW: 15 MHz typ. (unity-gain crossover)
- High SR: 10 V/μs typ. (unity-gain follower)
- High output current (I_O): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.
- Compensation with single external capacitor

Applications:

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- High-input-impedance comparators (ideal interface with digital COS/MOS)
- High-input-impedance wideband amplifiers
- Voltage followers (e.g., follower for single-supply D/A converter)
- Voltage regulators (permits control of output voltage down to zero volts)
- Peak detectors
- Single-supply full-wave precision rectifiers
- Photo-diode sensor amplifiers

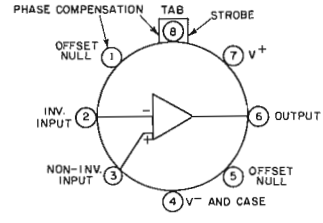
RCA-CA3130T, CA3130S, CA3130AT, CA3130AS, CA-3130BT, and CA3130BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor pair, capable of swinging the output voltage to within millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in either the standard 8-lead TO-5-style package (T suffix) or in the 8-lead dual-in-line formed-lead TO-5-style package "DIL-CAN" (S suffix) and operates over the full military-temperature range of −55°C to +125°C. The CA3130B is intended for applications requiring premium-grade specifications and with limits established for: input current, temperature coefficient of input-offset voltage, and gain over the range of −55°C to +125°C. The CA3130A offers superior input characteristics over those of the CA3130.



92CS-24713

Fig. 1—Functional diagram of the CA3130 Series.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) ..... 16 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC INPUT VOLTAGE ..... V^+ to (V^--0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK—
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
WITH HEAT SINK—
AT 125°C ..... 418 mW
BELOW 125°C ..... Increase linearly at 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING ..... −55 to +125°C
STORAGE ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
FROM CASE FOR 10 SECONDS MAX. ..... +265°C

*Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS — For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+=15 V, V^-=0 V, T_A=25°C (Unless Specified Otherwise)	CA3130B			CA3130A			CA3130			UNITS	FIG. NO.
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input Offset Voltage	$\|V_{IO}\|$	$V^{\pm}$=±7.5 V	–	0.8	2	–	2	5	–	8	15	mV	–
Input Offset Current	$\|I_{IO}\|$	$V^{\pm}$=±7.5 V	–	0.5	10	–	0.5	20	–	0.5	30	pA	–
Input Current	I_I	$V^{\pm}$=±7.5 V	–	5	20	–	5	30	–	5	50	pA	–
Large-Signal Voltage Gain	A_{OL}	V_O=10 $V_{p\text{-}p}$, R_L=2 kΩ	100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V	4,5
			100	110	–	94	110	–	94	110	–	dB	
Common-Mode Rejection Ratio	CMRR		86	100	–	80	90	–	70	90	–	dB	–
Common-Mode Input-Voltage Range	V_{ICR}		0	−0.5 to 12	10	0	−0.5 to 12	10	0	−0.5 to 12	10	V	–
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	$V^{\pm}$=±7.5 V	–	32	100	–	32	150	–	32	320	μV/V	–
	$\Delta V_{IO}/\Delta V^-$		–	32	100	–	32	150	–	32	320		
Maximum Output Voltage	V_{OM}^+	R_L=2 kΩ	12	13.3	–	12	13.3	–	12	13.3	–	V	9
	V_{OM}^-		–	0.002	0.01	–	0.002	0.01	–	0.002	0.01		10
	$\|V_{OM}^+\|$	R_L=∞	14.99	15	–	14.99	15	–	14.99	15	–		9
	$\|V_{OM}^-\|$		–	0	0.01	–	0	0.01	–	0	0.01		10
Maximum Output Current: Source	I_{OM}^+	V_O=0 V	12	22	45	12	22	45	12	22	45	mA	9
Sink	I_{OM}^-	V_O=15 V	12	20	45	12	20	45	12	20	45		10
Supply Current	I^+	V_O=7.5 V, R_L=∞	–	10	15	–	10	15	–	10	15	mA	7,8
		V_O=0 V, R_L=∞	–	2	3	–	2	3	–	2	3		
Input Current	I_I	T_A=−55 to 125°C, $V^{\pm}$=±7.5 V▲, V_O=10 $V_{p\text{-}p}$*, R_L=2 kΩ*	–	Fig. 11	15	–	Fig. 11	–	–	Fig. 11	–	nA	–
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		–	5	15	–	10	–	–	10	–	μV/°C	–
Large-Signal Voltage Gain	A_{OL}		50 k	320 k	–	–	320 k	–	–	320 k	–	V/V	5
			94	110	–	–	110	–	–	110	–	dB	

* Applies only to A_{OL}.

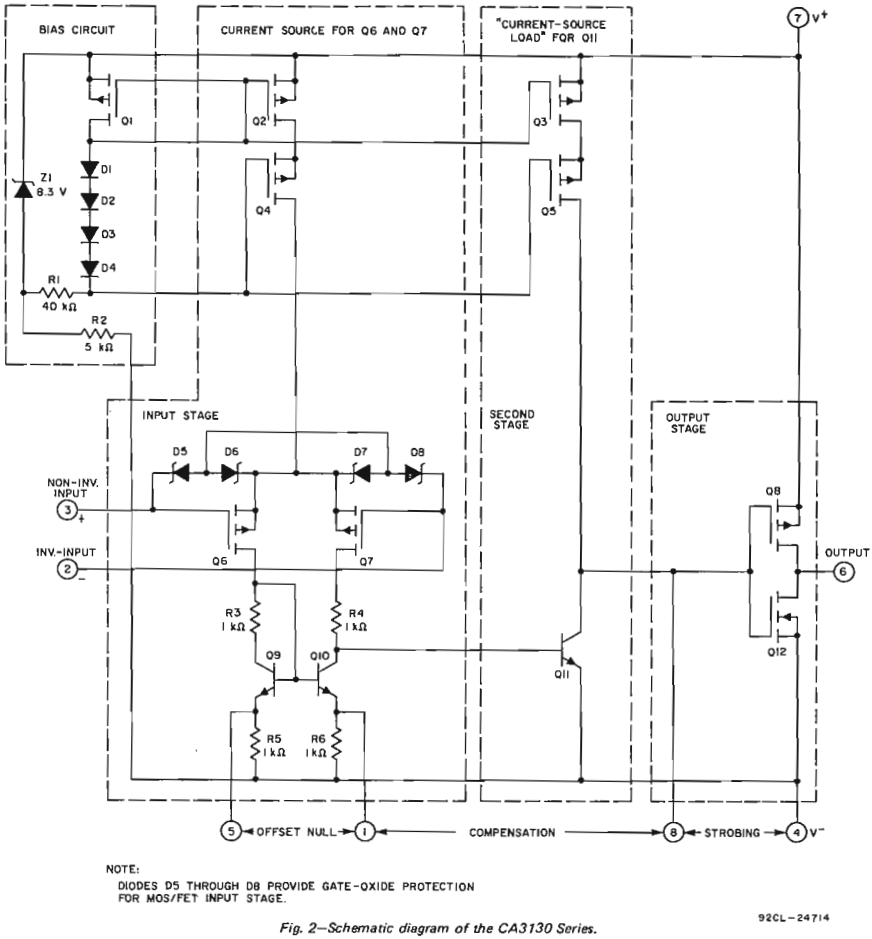
▲ Applies only to I_I and $\Delta V_{IO}/\Delta T$.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+=+7.5 V, V^-=−7.5 V, T_A=25°C (Unless Specified Otherwise)	CA3130B	CA3130A	CA3130	UNITS	FIG. NO.
Input Offset Voltage Adjustment Range		10 kΩ across Terms. 4 and 5 or 4 and 1	±22	±22	±22	mV	–
Input Resistance	R_I		1.5	1.5	1.5	TΩ	–
Input Capacitance	C_I	f = 1 MHz	4.3	4.3	4.3	pF	–
Equivalent Input Noise	e_n	BW=0.2 MHz, R_S=1 MΩ*	23	23	23	μV	14
Unity Gain Crossover Frequency	f_T	C_C = 0	15	15	15	MHz	4,15
		C_C = 47 pF	4	4	4		
Slew Rate: Open Loop	SR	C_C = 0	30	30	30	V/μs	–
Closed Loop		C_C = 56 pF	10	10	10		15
Transient Response: Rise Time	t_r	C_C = 56 pF, C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)	0.09	0.09	0.09	μs	15
Overshoot			10	10	10	%	15
Settling Time (4 Vp-p Input to <0.1%)			1.2	1.2	1.2	μs	15

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for sources of R_S up to 10 MΩ.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+ = 5 V, V^- = 0 V, T_A = 25°C (Unless Specified Otherwise)	CA3130B	CA3130A	CA3130	UNITS	FIG. NO.
Input Offset Voltage	V_{IO}		1	2	8	mV	–
Input Offset Current	I_{IO}		0.1	0.1	0.1	pA	–
Input Current	I_I		2	2	2	pA	–
Common-Mode Rejection Ratio	CMRR		100	90	80	dB	–
Large-Signal Voltage Gain	A_{OL}	V_O = 4 Vp-p, R_L = 5 kΩ	100 k	100 k	100 k	V/V	–
			100	100	100	dB	–
Common-Mode Input Voltage Range	V_{ICR}		0 to 2.8	0 to 2.8	0 to 2.8	V	–
Supply Current	I^+	V_O = 5 V, R_L = ∞	300	300	300	μA	7,8
		V_O=2.5 V, R_L = ∞	500	500	500		
Power Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V	–



NOTE:
DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOS/FET INPUT STAGE.

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Fig. 2—Schematic diagram of the CA3130 Series.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

Input Stages—The circuit of the CA3130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS

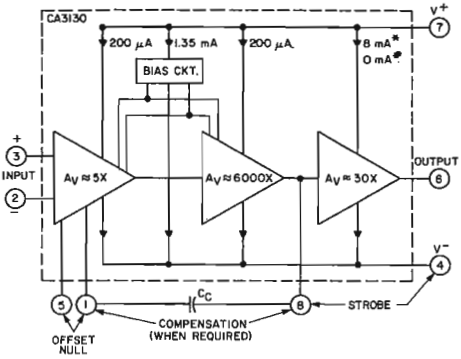


Fig. 3—Block diagram of the CA3130 Series.

transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g. including static electricity during handling for Q6 and Q7.

Second Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

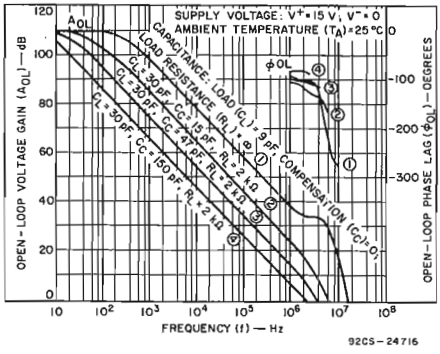


Fig. 4—Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q2 and Q3 are twice the size of Q1, the approximate 100-microampere current in Q1 establishes 200-microampere "mirrored" currents in Q2 and Q3 as constant-current sources for the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

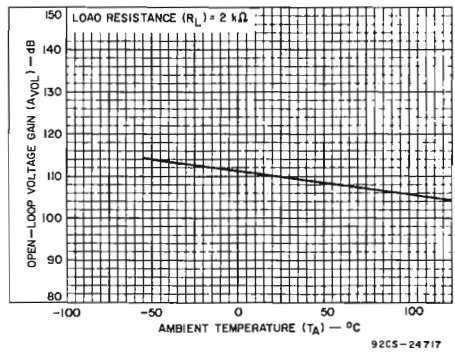


Fig. 5—Open-loop gain vs. temperature.

†For general information on the characteristics of COS/MOS transistor pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "COS/MOS Transistor Array."

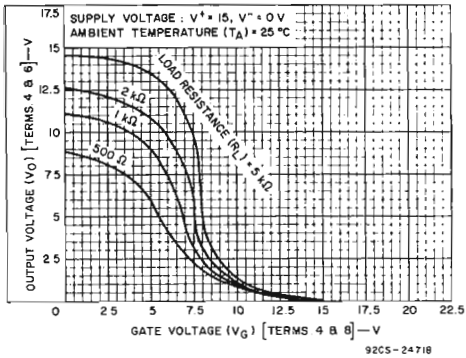


Fig. 6—Voltage transfer characteristics of CQS/MOS output stage.

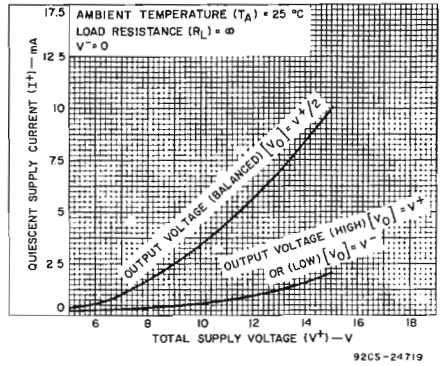


Fig. 7—Quiescent supply current vs. supply voltage.

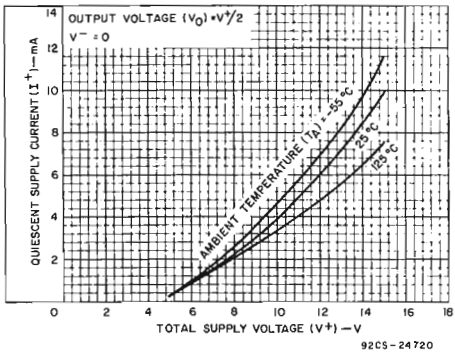


Fig. 8—Quiescent supply current vs. supply voltage at several temperatures.

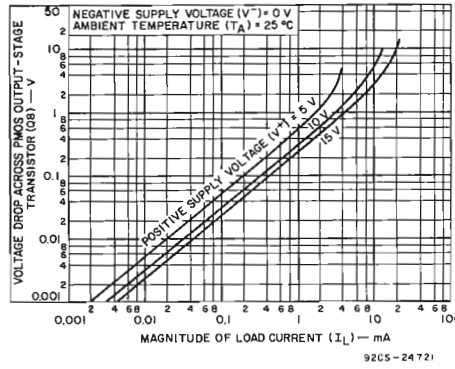


Fig. 9—Voltage across PMOS output transistor (Q8) vs. load current.

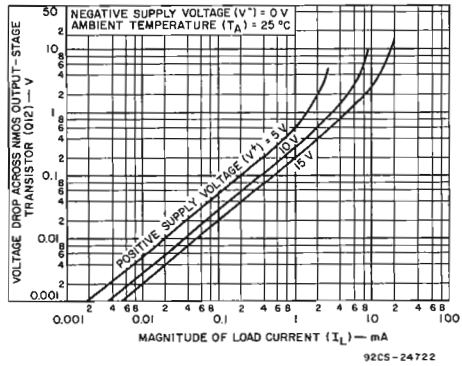


Fig. 10—Voltage across NMOS output transistor (Q12) vs. load current.

HANDLING AND OPERATING CONSIDERATIONS

Handling Considerations

The CA3130 uses MOS field-effect transistors in the input circuit. Because MOS/FET's have extremely high input resistances, they are susceptible to damage when exposed to extremely high static electrical charges. To minimize the possibilities of damaging the input stage transistors, Q6 and Q7, the CA3130 utilizes a protective diode network in the input stage. Nevertheless, it is good practice that the following precautions be observed during handling, testing, and actual operation of the CA3130 devices to minimize exposure to damage-inducing hazards:

1. Soldering-iron tips, metal parts of fixtures, tools, and handling facilities should be grounded.
2. Devices should not be inserted into or removed from circuits with the power ON because transient voltages may cause damage.
3. Signals should not be applied to the input (Terms. 2 and 3) when the device power supply is OFF. Input-terminal currents should not exceed 1 mA.
4. After CA3130 devices have been mounted on circuit boards, proper handling precautions should still be observed if the input terminals are unterminated. It is good practice during board-processing operations to return Terms. 2 and 3 to Term. 4 by jumping the appropriate conductors.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 11 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

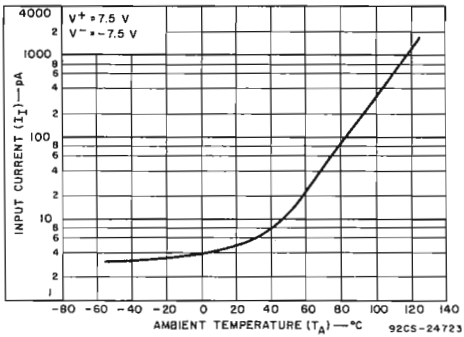


Fig. 11—Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Fig. 12 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices during life testing. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

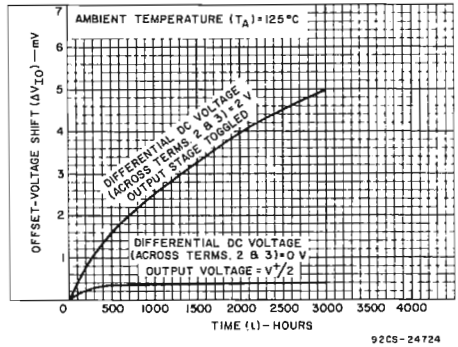


Fig. 12—Typical incremental offset-voltage shift vs. operating life.

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinant to review some considerations relating to power-supply current consumption under both single and dual-supply service. Figs. 13a and 13b show the CA3130 connected for both dual- and single-supply operation.

Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

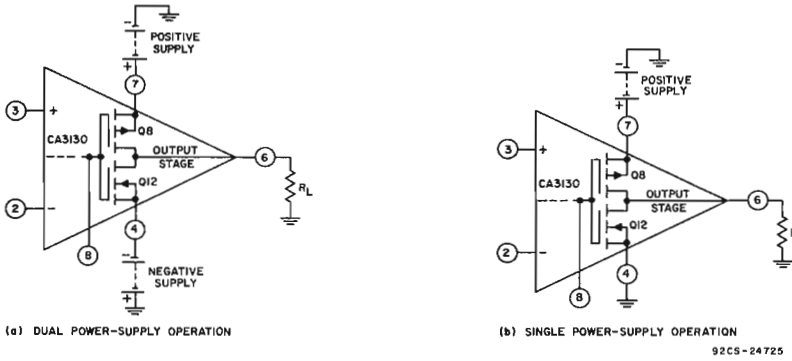


Fig. 13—CA3130 output stage in dual and single power-supply operation.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 13a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig. 13b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 μV when the test-circuit amplifier of Fig. 14 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

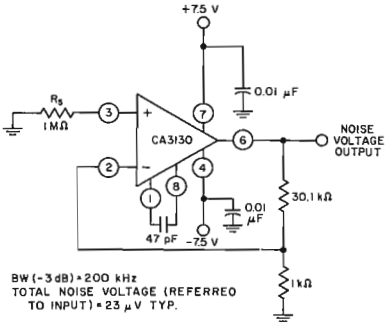
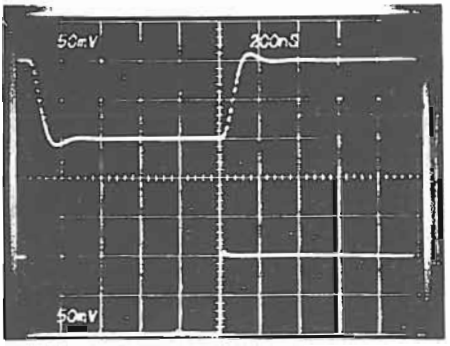
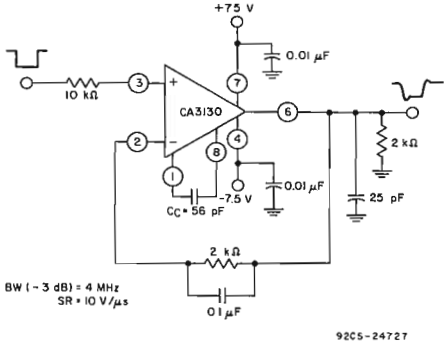


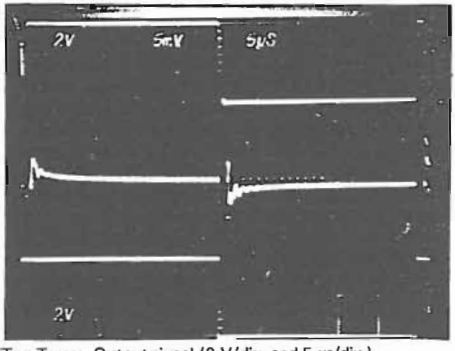
Fig. 14—Test-circuit amplifier (30-dB gain) used for wideband noise measurements.



Top Trace: Output
Bottom Trace: Input

(a) Small-signal response (50 mV/div. and 200 ns/div.)





Top Trace: Output signal (2 V/div. and 5 μs/div.)
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)

(b) Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)

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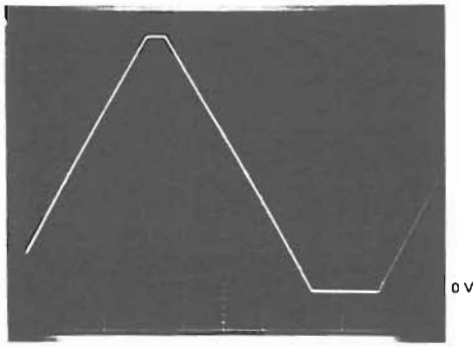
Fig. 15—Split-supply voltage follower with associated waveforms.

TYPICAL APPLICATIONS

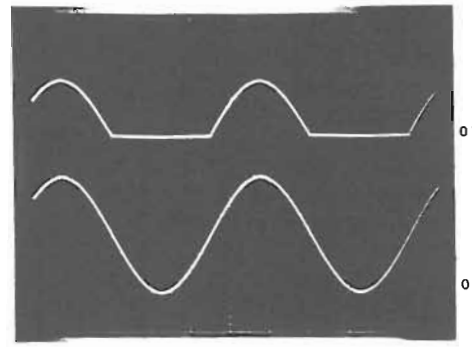
Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Fig. 15 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 16, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 16a with input-signal ramping. The waveforms in Fig. 16b show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 16b also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.



(a) Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)



Top Trace: Output (5 V/div. and 200 μs/div.)
Bottom Trace: Input (5 V/div. and 200 μs/div.)

(b) Output-waveform with ground-reference sine-wave input

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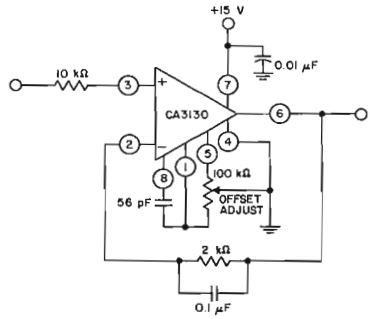

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Fig. 16—Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).

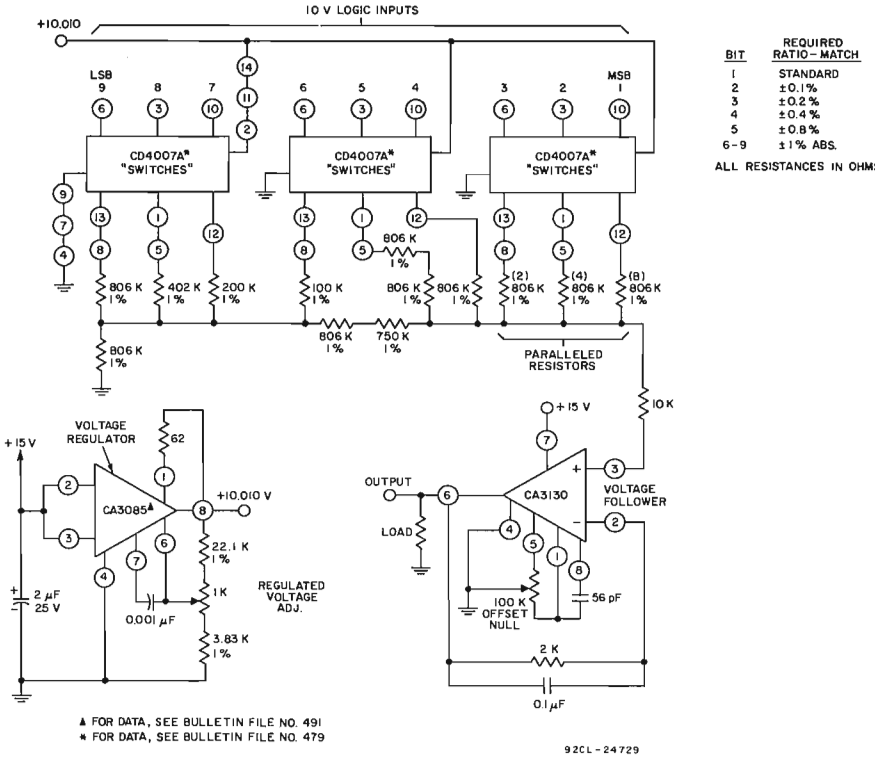
9-BIT COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig. 17. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op-amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 17.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output

*"Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC," Application Note ICAN-6080.



BIT	REQUIRED RATIO – MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS.

ALL RESISTANCES IN OHMS

Fig. 17—9-bit DAC using COS/MOS digital switches and CA3130.

control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

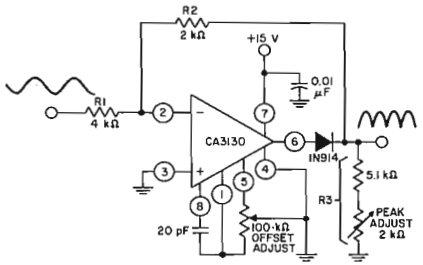
The absolute-value circuit using the CA3130 is shown in Fig. 18. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to $-R2/R1$. When the equality of the two equations shown in Fig. 18 is satisfied, the full-wave output is symmetrical.

Peak Detectors

Peak-detector circuits are easily implemented with the CA3130, as illustrated in Fig. 19 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.

Error-Amplifier in Regulated Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to



$$\text{GAIN} = \frac{R2}{R1} \cdot X = \frac{R3}{R1 + R2 + R3}$$

$$R3 = R1\left(\frac{X + X^2}{1 - X}\right)$$

$$\text{FOR } X = 0.5: \frac{2\text{ k}\Omega}{4\text{ k}\Omega} = \frac{R2}{R1}$$

$$R3 = 4\text{ k}\Omega\left(\frac{0.75}{0.5}\right) = 6\text{ k}\Omega$$

20 V p-p INPUT: BW(-3dB) = 230 kHz, DC OUTPUT (AVG.) = 3.2 V
1 VOLT p-p INPUT: BW(-3dB) = 130 kHz, DC OUTPUT (AVG.) = 160 mV

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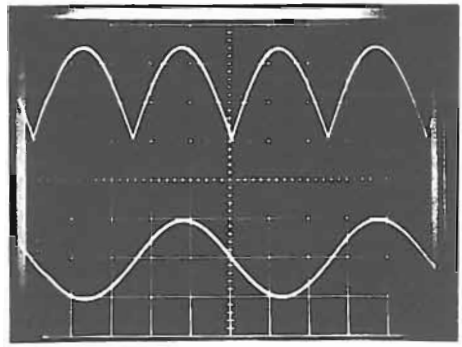
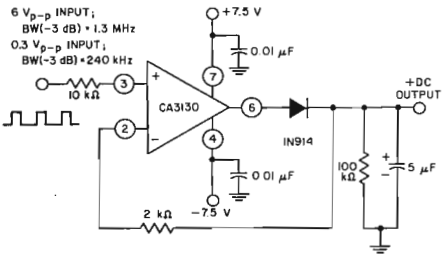


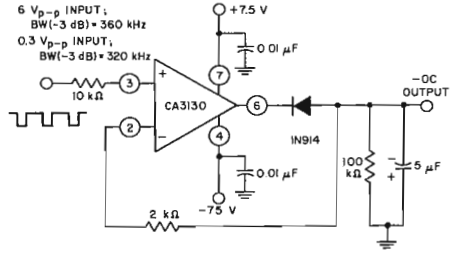
Top Trace: Output signal (2 V/div.)
Bottom Trace: Input signal (10 V/div.)
Time base on both traces: 0.2 ms/div.

92CS-24738

Fig. 18—Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.



(a) PEAK POSITIVE DETECTOR CIRCUIT



(b) PEAK NEGATIVE DETECTOR CIRCUIT

92CS-24731

Fig. 19—Peak-detector circuits.

approach zero. Fig. 20 shows the schematic diagram of a 40-mA power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.

Fig. 21 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 22. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor.

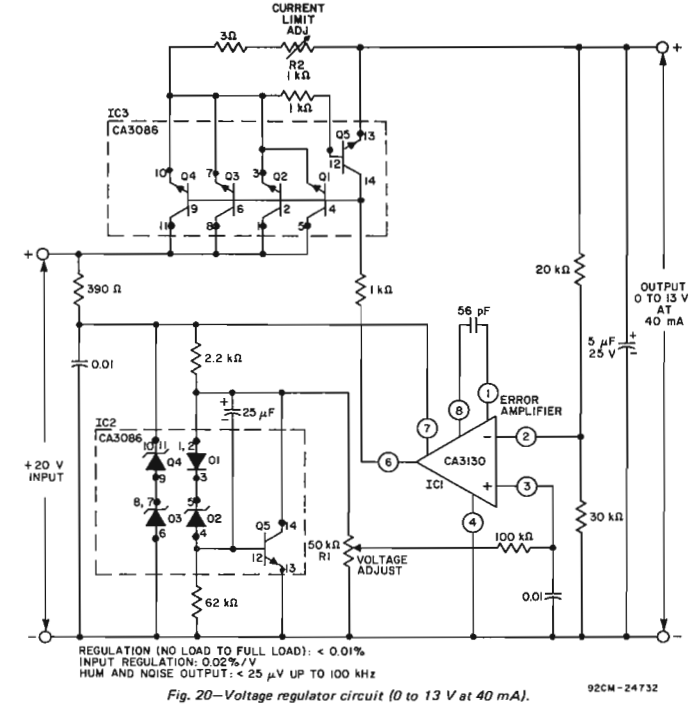


Fig. 20—Voltage regulator circuit (0 to 13 V at 40 mA).

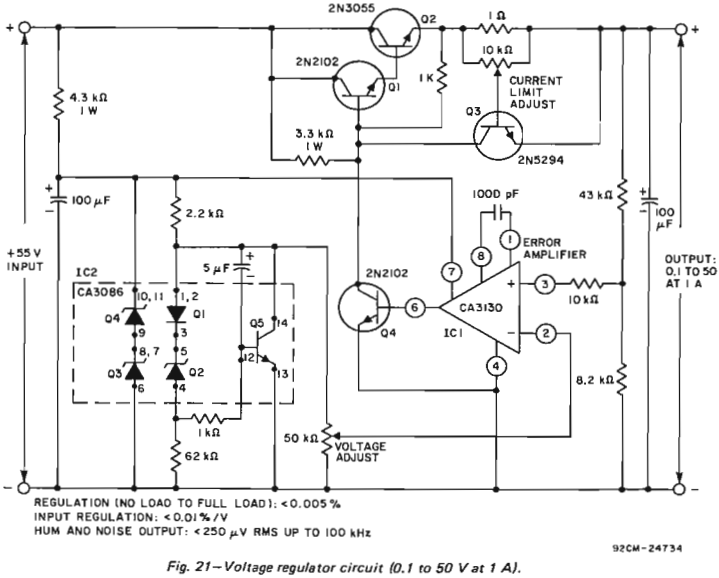


Fig. 21—Voltage regulator circuit (0.1 to 50 V at 1 A).

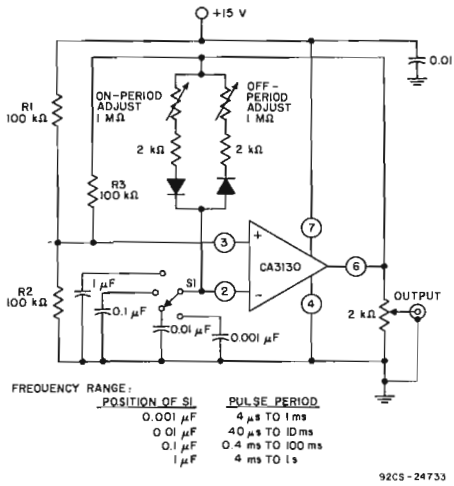


Fig. 22—Pulse generator (astable multivibrator) with provisions for independant control of "ON" and "OFF" periods.

Function Generator

Fig. 23 contains the schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

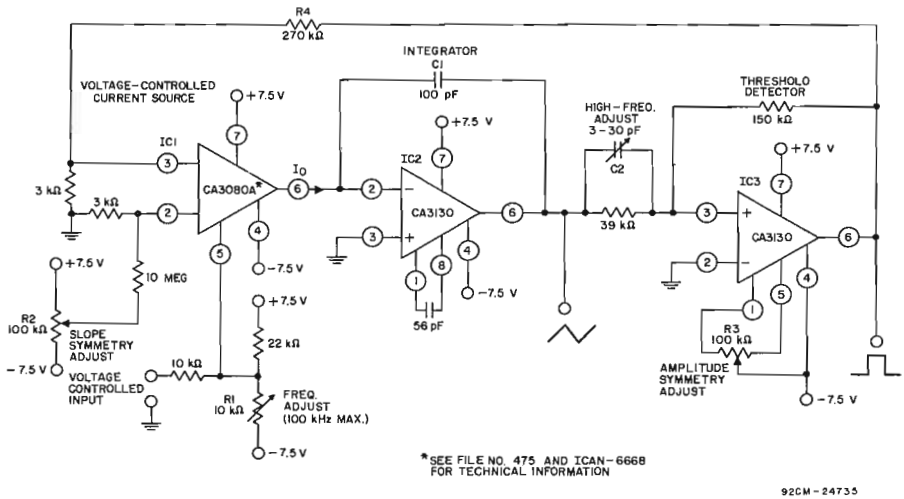


Fig. 23—Function generator (frequency can be varied 1,000,000/1 with a single control).

*See File No. 475 and ICAN-6668.

Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 24, three COS/MOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15 V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5x.

The amplifier circuit in Fig. 24 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (–3 dB) is 50 kHz.

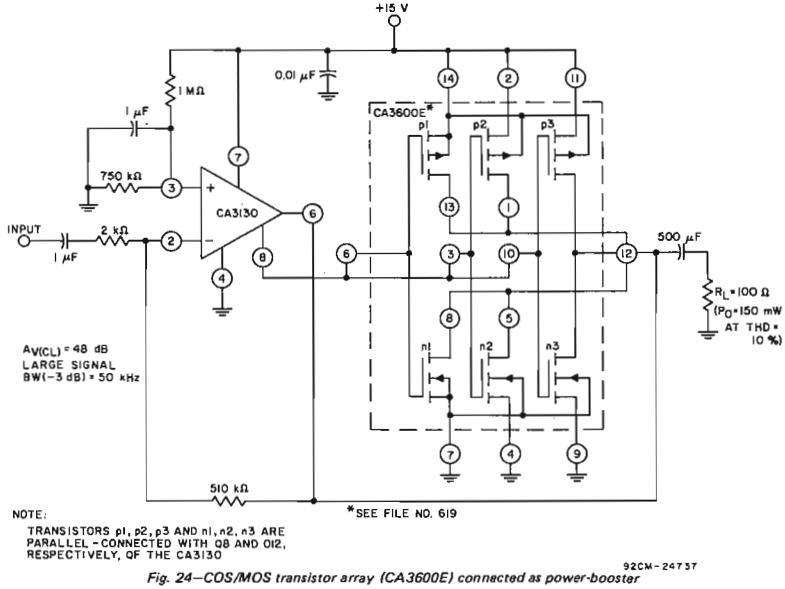


Fig. 24—COS/MOS transistor array (CA3600E) connected as power-booster in the output stage of the CA3130.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3131EM

CA3132EM

Preliminary Data

Modified
16-Lead Dual-in-Line
Plastic Package With
Heat Sink H-1827

5-Watt Audio Amplifiers

With Integral Heat Sink

Features:

- Power Output: 4 W min., 5 W typ.
- Complete amplifier including: preamplifier stages, power-output amplifier, and integral heat sink
- High power-supply rejection ratio
- Operating voltage: $V^+ = 24$ V typ.
- Available with internal feedback (CA3131EM) or without feedback (CA3132EM)

RCA-CA3131EM and CA3132EM are audio amplifiers with integral preamplifier stages on single integrated-circuit monolithic chips.

Utilizing a uniquely designed package with an integral heat sink, these devices can provide a power-output signal in excess of five watts at an ambient temperature of 25°C.

The CA3131EM employs an internal feedback network that sets the over-all gain of the amplifier to typically 48 dB.

The CA3132EM omits the internal feedback network. This arrangement offers the circuit designer a wide latitude in the choice of an external feedback network more suitable to a specific application.

Both types are encapsulated in a 16-lead dual-in-line plastic package with 4 center leads removed.

The CA3131EM and CA3132EM are electrically equivalent to and pin compatible with types SN76013 and SN76023, respectively.

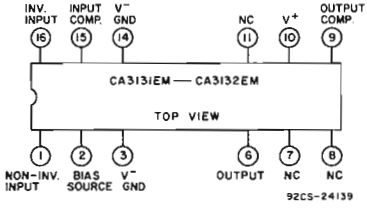


Fig. 1—Terminal assignment of the CA3131EM and CA3132EM.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY VOLTAGE, V^+	28 V
CONTINUOUS OUTPUT POWER, P_O (with $R_L = 8\ \Omega$ and $V^+ = 24$ V)	8 W RMS
MINIMUM RECOMMENDED LOAD IMPEDANCE, R_L	8 Ω
AMBIENT OPERATING TEMPERATURE, T_A (at 6 W RMS Output Power)	70 °C
STORAGE TEMPERATURE RANGE	−55 to +150 °C

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 24$ V

Characteristic	Symbol	Conditions	Values Min.	Values Typ.	Unit
Input Impedance	Z_I		200k	—	Ω
Power Output	P_O	At clipping onset			
		$R_L = 8\ \Omega$	4	—	W
		$R_L = 16\ \Omega$	3	—	W
Closed-Loop Gain — CA3131EM	A	f = 1 kHz	46	48	dB
Supply Current	I^+	Zero signal	—	10	mA
Total Harmonic Distortion	THD	$P_O = 50$ mW–4 W, $R_L = 8\ \Omega$	—	1	%
		$P_O = 50$ mW–3 W, $R_L = 15\ \Omega$	—	1	%
Noise Voltage	V_n	f=20 Hz–20 kHz	—	1.5	mV RMS

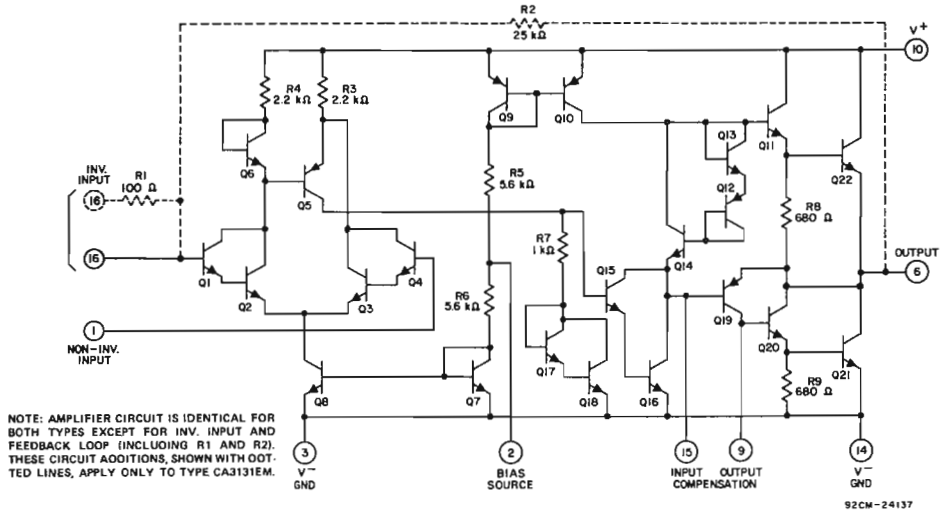
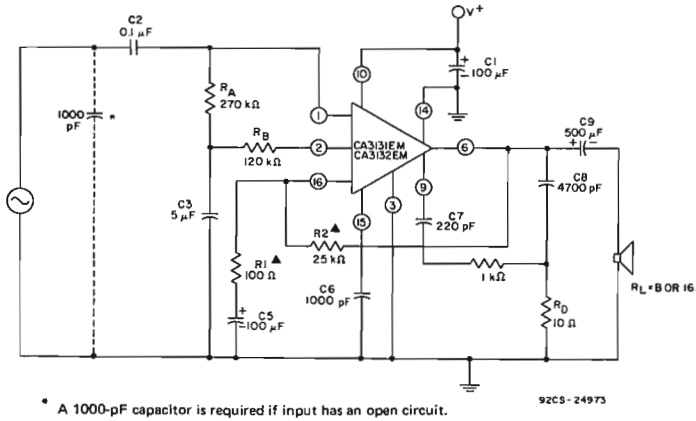


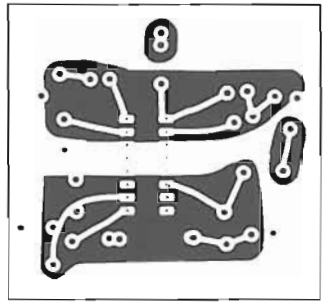
Fig. 2—Schematic diagram of types CA3131EM and CA3132EM.



* A 1000-pF capacitor is required if input has an open circuit.

▲ External resistors R1 and R2 are used only with the CA3132EM. When testing the CA3131EM, omit R1 and R2 and connect the (+) termination of C5 to Terminal 16.

Fig. 3—Test circuit for types CA3131EM and CA3132EM.



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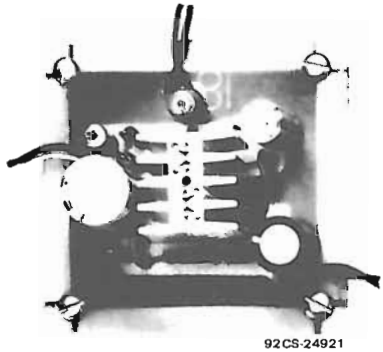
a. Bottom view of printed-circuit board.



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b. Component view of printed-circuit board - top view.

Fig. 4—Printed-circuit board containing the test circuit, shown in Fig. 3, for the CA3131EM.

Determining External Component Values (Refer to Figs. 2 & 3)

The dc quiescent output voltage is set by the voltage at Terminal 1. This voltage, in turn, is set by the internal voltage at Terminal 2 less I_I (input current, fixed by $R_A + R_B$, for Q4). The voltage at Terminal 2 is set slightly above half the supply voltage to allow for the voltage drop across $R_A + R_B$. Filter R_BC3 attenuates any ac ripple injected from the supply line and prevents positive feedback to Terminal 1. The rejection of supply voltage is a direct function of the filter attenuation.

The input impedance of the audio amplifiers is a function of the closed-loop gain and the magnitude of the Q8 current. In practice the input impedance is well above 1 megohm. The input signal, applied through C2, sees an impedance equivalent to the resistance of R_A connected in parallel with the amplifier input impedance. Hence, the value of R_A in most cases is dominant in establishing the input signal impedance.

The value of C1 depends on the regulation of the power supply. It is possible for the amplifier to work with a value of C1 as low as 0.1 μF to attenuate high-frequency signals in the supply line. Ideally, C1 should be placed as near Terminal 10 as possible. An electrolytic capacitor should be used for C1 if the power supply is poorly regulated to avoid ripple at the output.

Capacitor C6 at Terminal 15 provides over-all compensation. If a 1000-pF capacitor is used for C6, then the first breakpoint for a 46-dB closed-loop gain occurs at 200 kHz. Higher capacitance values will cause the constant current from Q10 to charge C6 on the positive voltage swing and thus limit the slew rate at high-signal levels. Because p-n-p transistor Q19 has a lower gain-bandwidth product (f_T) than the n-p-n transistors, C7 is connected to Terminal 9 to compensate for gain losses occurring in the negative voltage swings.

The use of the filter networks C8 and R_D at the output Terminal 6 is a standard requirement for class B audio outputs driving reactive speaker loads. Capacitor C8 compensates for the speaker inductance and R_D limits the current surges through C8.

The value of the coupling capacitor C9 to the load determines the low-frequency response of the amplifier.

Closed-Loop Gain

The closed-loop gain for either type is set by the ratio (R1 + R2)/R1. These resistors are included in the CA3131EM circuit and are external when used with the CA3132EM. In either type, the low-frequency value (−3 dB point) is reached when the impedance of C5 equals the value of R1.

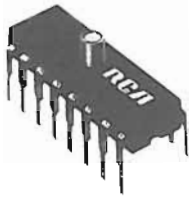
RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

Preliminary Data

CA3134E



16-Lead Plastic "Power-Stud" Dual-In-Line Package (E Suffix) H-1828

TV Sound IF and Audio Output Subsystem

Features:

- Nominal power output: 3 W (with suitable heat sink)
- Power amplifier with current limiting and thermal shutdown
- Wide power-supply range: 12 V to 40 V (30 V nominal)
- Low quiescent current: 30 mA typ.
- 5-kHz deviation sensitivity: 1 W output typ.
- 3-dB limiting sensitivity: 200 μV typ.
- Excellent AM rejection
- Differential peak detector—requires one tuned coil
- Electronic volume control with improved taper
- Optional unattenuated audio output

The RCA-CA3134E* Television Sound System is a monolithic integrated circuit which includes a multistage IF amplifier-limiter, an FM detector, an electronic attenuator, and an audio power amplifier that is designed to drive an 8-, 16-, or 32-ohm speaker. The CA3134E is encapsulated in a 16-lead plastic "power-stud" dual-in-line package that lends itself to a wide variety of techniques for mounting heat sinks.

* Formerly Dev. No. TA6480.

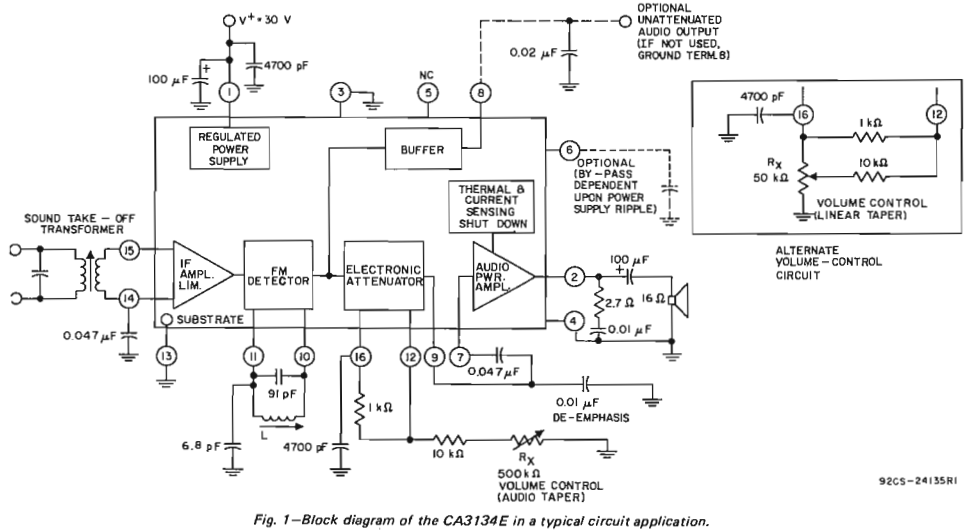


Fig. 1—Block diagram of the CA3134E in a typical circuit application.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE (Between Term. 1, V^+ and Terms. 4, audio-output ground and 13, substrate) ..... 40 V
DEVICE DISSIPATION:
With Infinite Heat Sink—
Up to T_A = 70°C ..... 6.5 W
Above T_A = 70°C ..... derate linearly 83.3 mW/°C
With No Heat Sink—
Up to T_A = 25°C ..... 1.4 W
Above T_A = 25°C ..... derate linearly 11.1 mW/°C
THERMAL RESISTANCE (Junction to Stud) ..... 12°C/W
AMBIENT TEMPERATURE RANGE:
Operating ..... −40 to +85°C
Storage ..... −65 to +150°C
LEAD TEMPERATURE (During Soldering):
At a distance 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C; V^+ = +30 V (applied to Term. 1); DC Volume Control, R_X = 500 kΩ; R_L = 16 Ω; unless otherwise indicated. Refer to Fig. 1.

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	NOMINAL VALUE	UNITS
Static Characteristics				
Current into Term. 1	I_1	P_O = 0	30	mA
Dynamic Characteristics				
IF Amplifier Input Limiting Voltage (at −3 dB point)	V_{15}(lim)	f_O = 4.5 MHz f_m = 400 Hz Δf = ±25 kHz	200	μV
AM Rejection	AMR	f_O = 4.5 MHz, f_m = 400 Hz, Modulation Index = 0.3, V_{15} = 20 mV	50	dB
Detector Recovered AF Voltage (Term. 9)	V_o(af)	f_O = 4.5 MHz, f_m = 400 Hz,	600	mV
Total Harmonic Distortion	THD	Δf = ±25 kHz, V_{15} = 100 mV	0.8	%
Attenuator Maximum Attenuation		R_X = 0	75●	dB
Unattenuated Audio Recovered AF Voltage (Term. 8)	V_o(af)	f_O = 4.5 MHz, f_m = 400 Hz,	−1.5#	dB
Total Harmonic Distortion	THD	Δf = ±25 kHz, V_{15} = 100 mV	0.8	%
Audio Power Amplifier Voltage Gain	A(af)	f = 1 kHz	35	dB
System Total Harmonic Distortion	THD(System)	P_O = 1 W (I_T = 120 mA typ.) P_O = 2 W (I_T = 165 mA typ.)	1.5 2.2	% %
Power Output	P_O	THD(System) = 10%	3.0*	W
Input Resistance	R_I(af)	f = 1 kHz	100	kΩ

* With suitable heat sink.

● The attenuation range can be increased by substituting lower-valued resistors for the 10-kΩ resistor in the volume-control circuit.

\# With respect to recovered AF voltage at Terminal 9 and volume control, R_X, at maximum resistance position.

OPERATING CONSIDERATIONS

Power measurements were taken with a tin-plated copper-strap-type heat sink attached to the CA3134E. The heat sink, 1/32-inch thick, 1/4-inch wide, 1-7/8-inch long, is "U" shaped and has a 0.107-inch mounting hole to accept the stud on the IC package. The strap was also attached to the top side of the plastic package with epoxy cement to minimize stress on the stud during the mounting and handling operation. The torque, applied to the stud, should be limited to less than 3 in.-lbs. The applied tensile stress should be limited to less than 15 pounds and the compression stress should be limited to less than 100 pounds. Conductive epoxy (such as Dupont 5504A) was used for the interface between the stud and the heat sink; whereas non-conductive epoxy (such as Uniset Structural Adhesive) was used to attach the heat sink to the plastic package. The assembly when soldered to a 3-inch by 4-inch PC board has a typical over-all thermal resistance ($\theta_{\text{Stud to Amb.}}$) of 20°C/W.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3401E

14-Lead Dual-In-Line Plastic Package

H-1517

Quad Single-Supply Operational Amplifier

For Automotive Electronics and Industrial Control Systems

Features:

- Single-supply operation — +5 V to +18 Vdc
- Internally compensated
- Wide unity-gain bandwidth — 5 MHz typ.
- Low input bias current — 50 nA typ.
- High open-loop gain — 2000 V/V typ.

RCA-CA3401E* is a high-gain monolithic quad operational amplifier designed specifically for applications using a single positive power supply. No external compensation is necessary. Closed-loop stability in each of the four independent amplifiers is maintained by a 3-pF on-chip capacitor. The CA3401E is ideally suited for applications in industrial control systems, automotive electronics, and general-purpose amplifiers, e.g., oscillators, tachometers, active filters, and multichannel amplifiers. The CA3401E is supplied in a 14-lead dual-in-line plastic package and operates over a temperature range of −55 to 125°C. It is a direct replacement for the Motorola MC3401P, is pin-compatible with the Motorola MC3301P, and pin compatible with the National Semiconductor LM3900N.

*Formerly RCA Dev. No. TA6306.

Applications:

- Automotive
- Constant-Current Sources
- Multivibrators
- Sample and Hold
- Square-Wave Generator
- Oscillators
- Tachometers
- Active Filters
- Multi-Channel Amplifiers
- Summing Amplifiers

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C*

DC Supply Voltage	+18	V
Input Signal Current	5	mA
Device Dissipation:		
Up to T_A = 25°C	625	mW
Above T_A = 25°C	Derate linearly 5 mW/°C	
Ambient Temperature Range:		
Operating	−55 to +125°C	
Storage	−65 to +150°C	
Lead Temperature (During soldering):		
At distance 1/16±1/32 inch (1.59±0.79 mm) from case for 10 seconds max.	300	°C

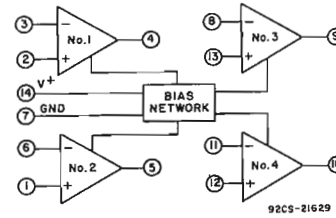


Fig. 1— Block diagram of CA3401E.

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$, $V^+ = 15$ V (UNLESS INDICATED OTHERWISE)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
		CIRCUIT Fig. No.		Typical Characteristics Curves Fig. No.	Min.	Typ.	Max.	
STATIC								
Output Voltage:								
High	V_{OH}	5,6			13.5	14.2	–	V
Low	V_{OL}				–	0.03	0.1	
Max. Undistorted Output Swing	V_{OP-P}		$0^oC \leq T_A \leq 75^oC$		10	13.5	–	
Output Current:								
Source	I_{SOURCE}	3		11, 12	5	10	–	mA
Sink	I_{SINK}				0.5	1	–	
Total Quiescent Current:								
Noninverting inputs open	I_Q	4		10	–	6.9	10	mA
Noninverting inputs grounded					–	7.8	14	
Input Bias Current	I_{IB}	3	$R_L = \infty$ $T_A = 25^oC$		–	50	300	nA
			$R_L = \infty$ $0^oC \leq T_A \leq 75^oC$		–	–	500	
DYNAMIC								
Open-Loop Voltage Gain	A_{OL}	3	$T_A = 25^oC$	7, 9	1000	2000	–	V/V
			$0^oC \leq T_A \leq 75^oC$		800	–	–	
Input Resistance	R_I	3			0.1	1	–	MΩ
Slew Rate	SR		$C_L = 100$ pF, $R_L = 5$ kΩ		–	0.6	–	V/μs
Unity Gain Bandwidth	BW				–	5	–	MHz
Phase Margin	ϕ				–	70	–	DEGREES
Power Supply Rejection			f = 100 Hz		–	55	–	dB
Channel Separation	e_{01}/e_{02}		f = 1 kHz		–	65	–	dB

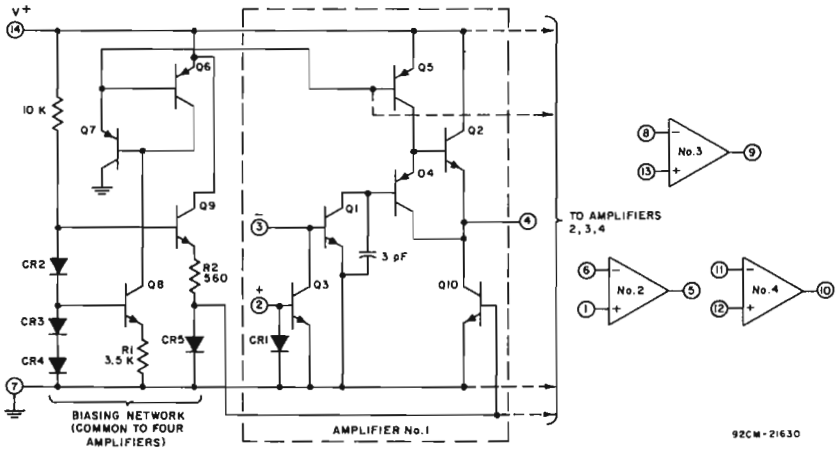


Fig. 2– Schematic diagram of CA3401E.

TEST CIRCUITS

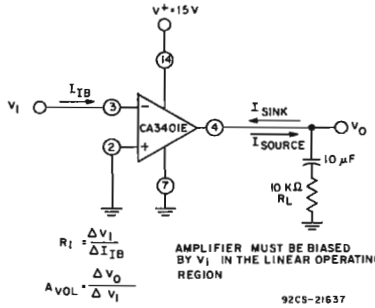


Fig.3 – Open-loop gain and input resistance, input bias current and output current test circuit.

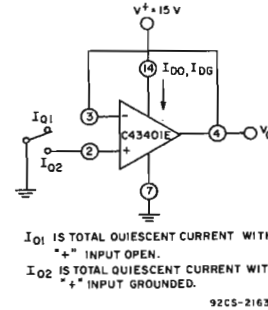


Fig.4 – Quiescent power supply current test circuit.

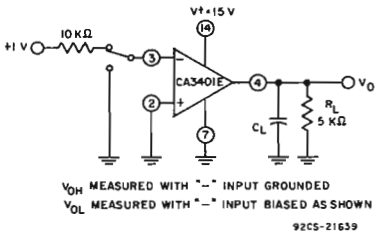


Fig.5 – Output voltage swing test circuit.

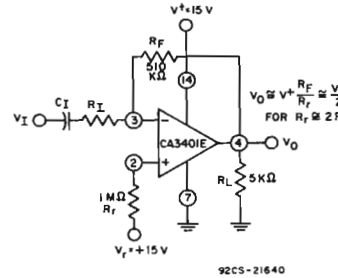


Fig.6 – Peak-to-peak output voltage test circuit.

TYPICAL CHARACTERISTIC CURVES

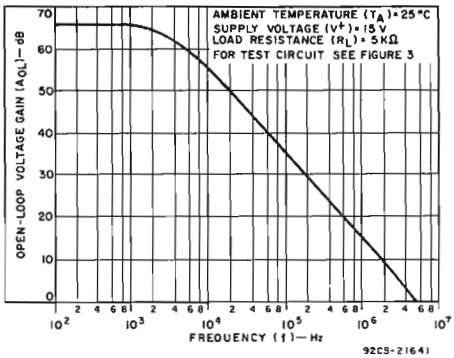


Fig.7 – Open-loop voltage gain vs. frequency.

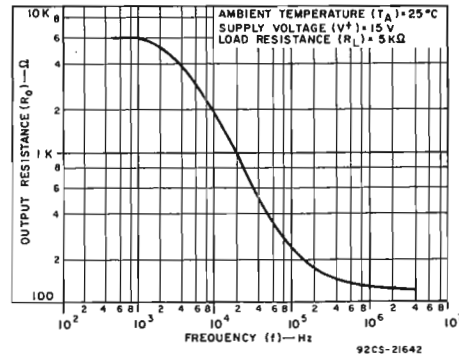


Fig.8 – Output resistance vs. frequency.

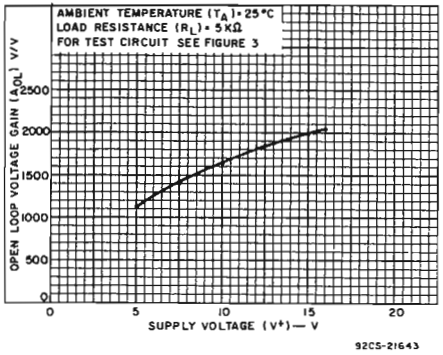


Fig.9 – Open-loop voltage gain vs. supply voltage.

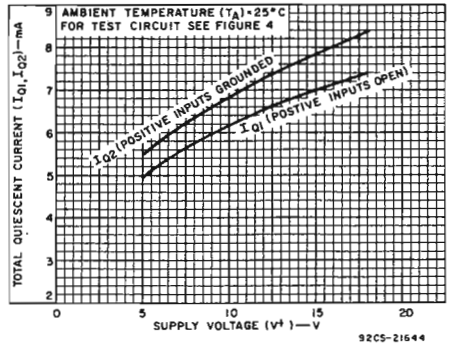


Fig.10 – Supply current vs. supply voltage.

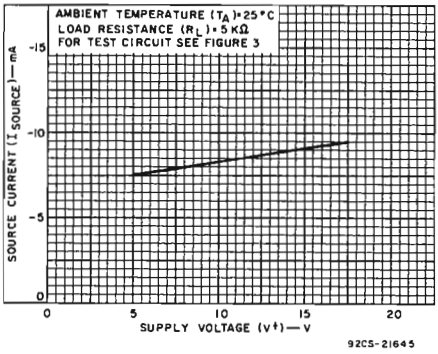


Fig.11 – Source current vs. supply voltage.

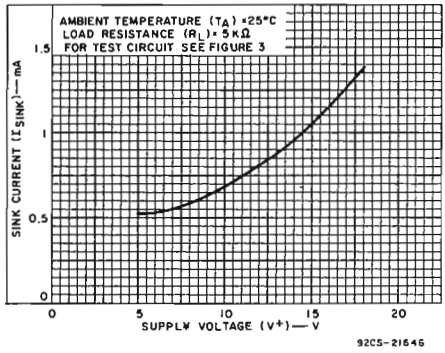


Fig.12 – Sink current vs. supply voltage.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

CA3600E

14-Lead dual-in-line plastic package

H-1517

COS/MOS Transistor Array

For Linear Circuit Applications

Applications:

- High input impedance, general-purpose amplifiers
- Pre-amplifiers
- Differential amplifiers
- Op-amps and comparators
- Constant-current sources and current mirrors
- Micropower amplifiers and oscillators
- Control of lamps, LED's, relays, and thyristors
- Timers
- Choppers
- Mixers

RCA-CA3600E is an array of COmplementary-Symmetry MOS Field-Effect Transistors* on a monolithic silicon substrate. It is comprised of three n-channel and three p-channel enhancement-type MOS transistors arrayed as shown in Fig. 1, and specified and tested for linear circuit operation. These transistors are uniquely suitable for service in complementary-symmetry circuits at supply voltages in the range of 3 to 15 volts and are useful at frequencies up to 5 MHz (untuned). Each transistor in the CA3600E can conduct currents up to 10 mA. This device is supplied in the 14-lead dual-in-line plastic package.

Formerly RCA Dev. No. TA6368.

* The theory and construction of COS/MOS transistors are described in the "RCA COS/MOS Integrated Circuits Manual," RCA Solid State Division Technical Series Publication No. CMS-271.

Features:

- High input resistance . . . . . 100 GΩ (typ.)
- Low gate-terminal current . . . . 10 pA (typ.)
- Matched p-channel pair:
  Gate-voltage differential (I_D = -100 μA) ±20 mV (max.)
- No "Popcorn" (burst) noise
- Stable transfer characteristics over an operating temperature range of −55°C to +125°C when operated in complementary circuit configuration at supply voltages in the 5 to 15 volt range (see Fig. 14)
- Integrated integral gate-protection system (see Fig. 34)
- High voltage gain (see Fig. 11). . . up to 53 dB (typ.) per COS/MOS stage
- Individual MOS transistors have square-law characteristics, superior cross-modulation performance, and greater dynamic range than bipolar transistors

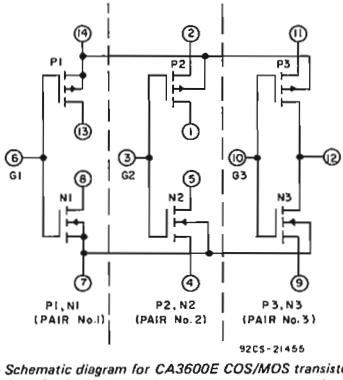


Fig. 1 – Schematic diagram for CA3600E COS/MOS transistor array. (See Fig. 34 for internal gate-and-channel-protection circuits)

1. Drain terminal, p-channel of pair no. 2
2. Source terminal, p-channel of pair no. 2
3. Common gate terminal of pair no. 2
4. Source terminal, n-channel of pair no. 2
5. Drain terminal, n-channel of pair no. 2
6. Common gate terminal of pair no. 1
7. Source terminal, n-channel of pair no. 1 and substrate connection for all n-channel transistors - - - V_{SS} terminal
8. Drain terminal, n-channel of pair no. 1
9. Source terminal, n-channel of pair no. 3
10. Common gate terminal of pair no. 3
11. Source terminal, p-channel of pair no. 3
12. Common drain terminal of pair no. 3
13. Drain terminal, p-channel of pair no. 1
14. Source terminal, p-channel of pair no. 1 and substrate connection for all p-channel transistors - - - V_{DD} terminal

Terminal Identification for Fig. 1.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DISSIPATION:	
Any one transistor at T_A up to 55°C	150 mW
Total package at T_A up to 55°C	750 mW
Above T_A = 55°C	derate linearly 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering)	
At distance not less than 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

The Following Ratings Apply for Each Transistor in the Device:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}:	
n-channel	+15 V
p-channel	−15 V
DRAIN-TO-GATE VOLTAGE, V_{DG}:	
n-channel	+15 V
p-channel	−15 V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}:	
n-channel	+15 V
p-channel	−15 V
GATE-TO-SOURCE VOLTAGE, V_{GS}:	
p-channel transistors (p_1, p_2, p_3)	0 V(min.),−V_D(max.)
n-channel transistors (n_1, n_2, n_3)	0 V(min.),+V_D(max.)
COS/MOS transistor-pairs (p_1-n_1, p_2-n_2, p_3-n_3)	0 V(min.),+V_{DD}(max.)
DRAIN CURRENT, $\|I_D\|$	10 mA
GATE CURRENT, $\|I_G\|$	100 μA

The Following Rating Applies for Each COS/MOS Transistor-Pair in the Device:

DC SUPPLY VOLTAGE ($V_{DD} - V_{SS}$)	+15 V

Rules for Maintaining Electrical Isolation Between Transistors and Monolithic Substrate

Terminal No. 14 must be maintained at the most positive potential (or equally positive potential) with respect to any other terminal in the CA3600E.

Terminal No. 7 must be maintained at the most negative potential (or equally negative potential) with respect to any other terminal in the CA3600E.

Violation of these rules will result in improper transistor operation, circuit "latching," and/or possible permanent damage to the CA3600E.

Note: Users should observe the "Considerations in Handling CA3600E Devices", discussed on pages 599 and 600.

ELECTRICAL CHARACTERISTICS, *At $T_A = 25^oC$*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	TYPICAL CURVE OR CIRCUIT FIG. NO.	LIMITS			UNIT
				Min.	Typ.	Max.	
For Each p-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=−10 V,V_{GS}=−3.6 V	2,3,4	−0.5	−1.1	−2.0	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=−10 μA	–	–	−1.75	–	V
Gate-to-Source Voltage Differential (p_1 vs. p_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=−100 μA,V_{DS}=−10 V	5	–	±4	±20	mV
Forward Transconductance	g_{fs}	I_D=−1 mA,f=1 kHz	6	–	920	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=−1 mA,f=1 kHz,R_s=0 Ω	7	–	0.03	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=−1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.2	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (p_1/p_2)	I_{MTR}	I_1=−100 μA,V_{DS}=−10 V	30	0.7	1.1	1.5	–
Gate-Terminal Current	I_{GT}	V_{DS}=−10 V,V_{GS}=−3.5 V	–	–	±0.015	−40	nA
Input Capacitance	C_I	–	–	–	6.3	–	pF
Output Capacitance	C_O	–	–	–	3	–	pF
Input-to-Output Capacitance	$C_{I\text{-}O}$	–	–	–	0.75	–	pF
For Each n-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=+10 V,V_{GS}=+3.6 V	2,3,4	0.4	0.9	1.6	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=10 μA	–	–	1.5	–	V
Gate-to-Source Voltage Differential (n_1 vs n_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=100 μA,V_{DS}=+10 V	5	–	±30	–	mV
Forward Transconductance	g_{fs}	I_D=1 mA,f=1 kHz	6	–	860	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=1 mA,f=1 kHz,R_s=0 Ω	7	–	0.2	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.3	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (n_1/n_2)	I_{MTR}	I_1=100 μA,V_{DS}=+10 V	29	0.7	1.3	2.0	–
Gate-Terminal Current	I_{GT}	V_{DS}=+10 V,V_{GS}=+3.7 V	–	–	±0.01	+40	nA
Input Capacitance	C_I	–	–	–	5.5	–	pF
Output Capacitance	C_O	–	–	–	2.0	–	pF
Input-to-Output Capacitance	$C_{I\text{-}O}$	–	–	–	0.35	–	pF
For Each COS/MOS Transistor Pair							
Drain Current	I_{DD}	V_{DD}=+10 V	9,10	1.0	2.2	4.0	mA
Drain-to-Source Cutoff Current	$I_{DD(off)}$	V_{DD}=+10 V,V_{SS}=0 V Gate Voltage(V_G)=+10 V or 0 V	8	–	0.5	100	nA
DC Output Voltage	V_O	V_{DD}=+10 V	10	4.2	5.0	5.8	V
Forward Transconductance	g_{fs}	V_{DD}=+10 V, f = 1 kHz	6	–	2300	–	μmho
Slew Rate (Open-Loop)	SR	V_{DD}=+15 V	10	–	95	–	V/μs
Amplifier Voltage Gain	A_{OL}	V_{DD}=+10 V,f=1 kHz,R_b=22 MΩ R_s=50 Ω	10,11	–	32	–	dB
Gate-Terminal Current	I_{GT}	V_{DD}=+10 V	10	–	±0.005	±20	nA
Broadband Output Noise Voltage	E_{ON}	V_{DD}=+10 V,R_b=22 MΩ,R_s=10 kΩ	10,11	–	500	–	μV
Input Capacitance	C_I	–	–	–	11.8		pF
Output Capacitance	C_O	–	–	–	5.0		pF
Input-to-Output Capacitance	$C_{I\text{-}O}$	–	–	–	1.1		pF

TYPICAL CHARACTERISTICS CURVES

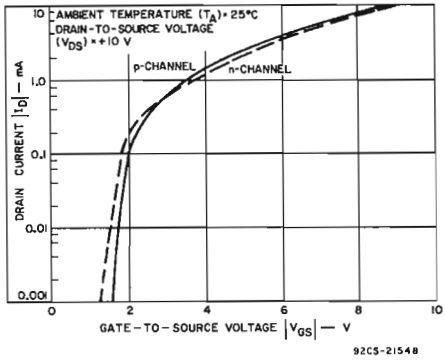


Fig. 2—Drain current vs. gate-to-source voltage.

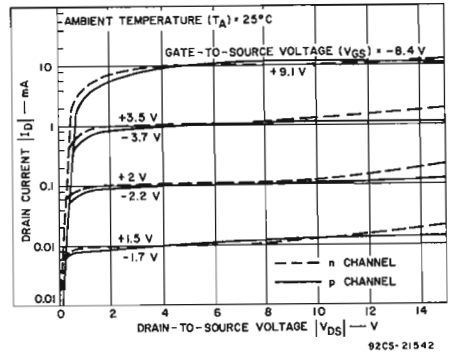


Fig. 3— Drain current vs. drain-to-source voltage.

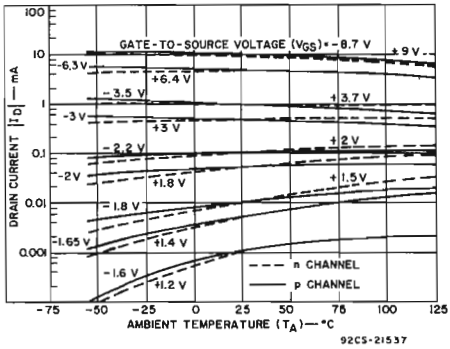


Fig. 4— Drain current vs. ambient temperature.

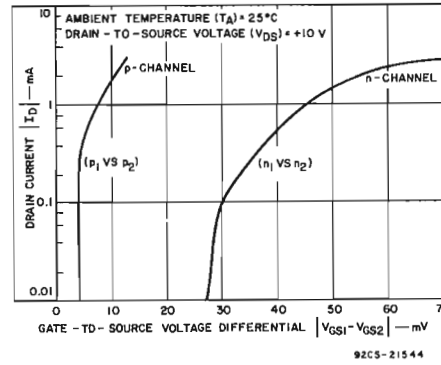


Fig. 5— Gate-to-source voltage differential vs. drain current.

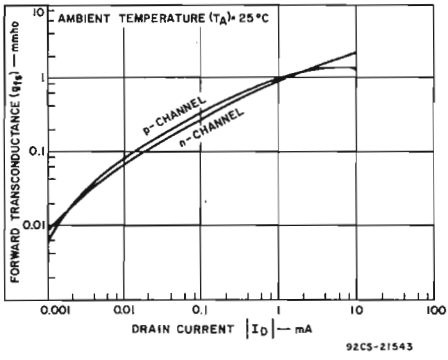


Fig. 6— Forward transconductance vs. drain current.

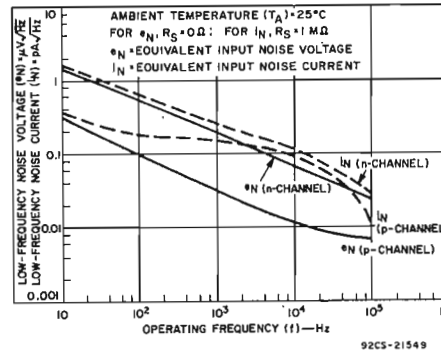


Fig. 7— Noise voltage and noise current vs. operating frequency.

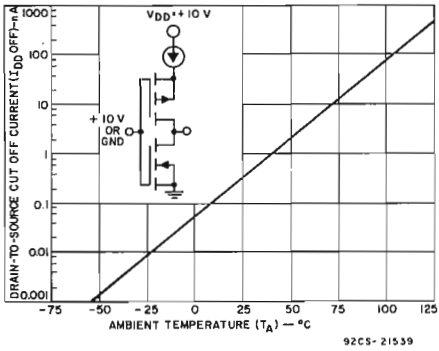


Fig. 8– Drain-to-source cutoff current vs. ambient temperature.

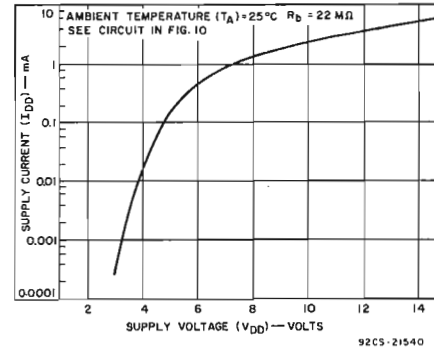


Fig.9 – Typical V_{DD} vs. I_{DD} characteristics for amplifier circuits of Fig.10 and Fig.15.

APPLICATIONS

The Basic COS/MOS Linear Amplifier

P-n-p and n-p-n bipolar transistors have been used for many years in the design of so-called "true-complementary" linear amplifier circuits[1]. Since mutually compatible p-channel and n-channel MOS/FET devices were not generally available, "true-complementary" amplifier circuits using MOS transistors were seldom used. Now, COS/MOS transistor technology[5] has made it possible to supply compatible p-channel/n-channel transistors in monolithic IC form such as the CA3600E COS/MOS transistor array shown in Fig. 1.

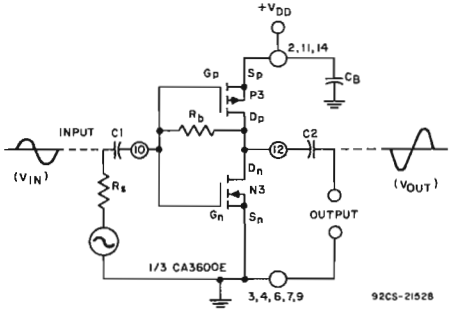


Fig. 10– COS/MOS transistor-pair biased for linear-mode operation.

A "True-Complementary" Linear Amplifier Using COS/MOS Transistors

Fig. 10 shows the schematic diagram of a single-stage "true-complementary" linear amplifier using one pair of the complementary MOS transistors in the CA3600E, connected in a common-source circuit. Resistor R_b is used to bias the complementary pair for Class A operation, as described subsequently, and R_s represents the source resistance of the signal source. This generic amplifier is suitable for operation with a single or split voltage supply in the range of 3 to 15 volts. Fig. 11 shows voltage gain as a function of operating frequency at various supply voltages for the single-stage amplifier. This amplifier is capable of producing very high output-swing voltages (V_{out}); for example, its output voltages can be swung to within several millivolts of either supply-voltage "rail". Fig. 9 shows typical supply voltage (V_{DD}) vs. supply current (I_{DD}) characteristics for the single-stage amplifier. The curves in Fig. 12 show the normalized amplifier supply current as a function of ambient temperature at various supply voltages. When the amplifier is operating at V_{DD} = 3 V, the supply current changes rapidly as a function of temperature because the MOS transistors are operating in the proximity of their individual gate-source threshold voltages.

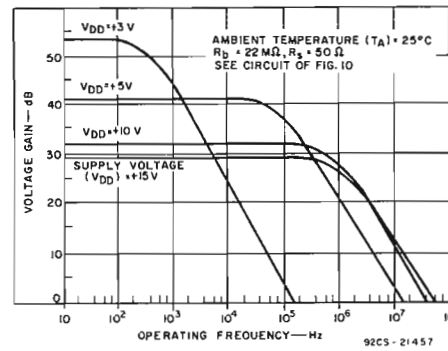


Fig. 11– Typical voltage gain vs. frequency characteristics for amplifier circuit of Fig. 10.

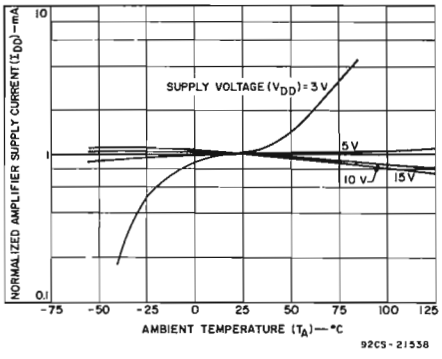


Fig. 12— Normalized amplifier supply current vs. ambient temperature characteristics for amplifier circuit of Fig. 10.

Voltage-Transfer Characteristics

Fig. 13 illustrates a voltage-transfer characteristic curve of a COS/MOS transistor pair connected in the amplifier circuit of Fig. 10, with a biasing resistor (R_b) connected between the drain and gate terminals (10,12). If the p- and n-channel transistors have identical characteristics, their channel resistances are equal, and the biasing method shown establishes a steady-

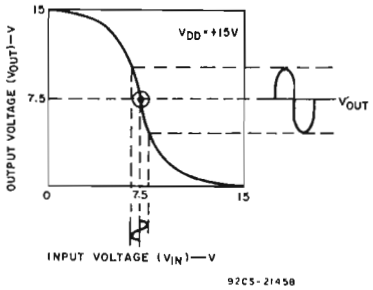


Fig. 13 — Representation of voltage-transfer characteristics for COS/MOS transistor pair.

state condition such that terminal 12 is at mid-potential between V_{DD} and ground. Thus, with negligibly small gate-source leakage resistances, under zero-signal conditions, the biasing resistor (R_b) establishes gate potential at the mid-point between V_{DD} and ground, i.e., $V_{in} = V_{out}$. Under these conditions the amplifier is biased for operation about the mid-point ("0") in the linear segment on the steep transition of the voltage-transfer characteristic as shown in Fig. 13. When the input signal (V_{in}) swings in the positive direction, there is a reduction in the instantaneous output voltage (V_{out}) with respect to ground. Negative-going input signals have inverse effects. Thus, phase-inversion occurs in the COS/MOS-pair amplifier. Power-supply current is constant during dynamic linear operation, i.e., Class A amplifier service. When the signal input-voltage level (V_{in}) becomes very large, the output signal (V_{out}) waveforms become distorted because the transistors are driven into the non-linear portions of their voltage-transfer characteristics. If the positive-going input-signal is sufficiently large, for example, the p-channel transistor can be driven to cutoff and the amplifier supply current (I_{DD}) is reduced to essentially zero.

Fig. 14 shows typical voltage-transfer characteristics of each COS/MOS pair in the CA3600E at several values of V_{DD}. The shape of these transfer characteristics is comparatively constant despite temperature changes from −55 to +125°C.

The biasing arrangement used in the circuit of Fig. 10 provides an easy method of establishing feedback for ac signals in accordance with the R_b/R_s ratio. When the feedback of ac signals is not desirable, the circuit of Fig. 15 may be used. The ac bypass capacitor (C_3) minimizes ac signal feedback.

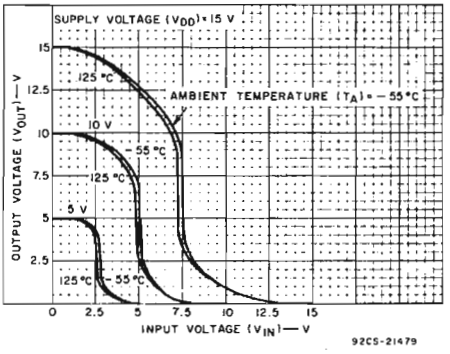


Fig. 14— Voltage transfer characteristics for COS/MOS transistor-pair amplifier in Fig. 10.

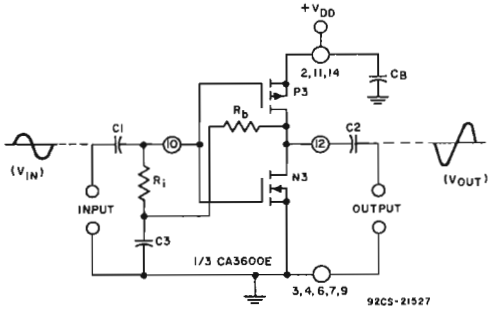


Fig. 15— Alternate method of biasing COS/MOS transistor-pair for linear-mode operation.

Cascading Amplifier Stages of COS/MOS Transistor Pairs

Ultra-high-gain amplifiers can be designed by cascading stages of COS/MOS transistor pairs as shown in Fig. 16. The biasing system used is similar to that described above in connection with Fig. 10. The supply current for the three-stage amplifier shown in Fig. 16 is typically three times the values shown in Fig. 9. Gain and frequency-response characteristics of the amplifier are shown in Fig. 17.

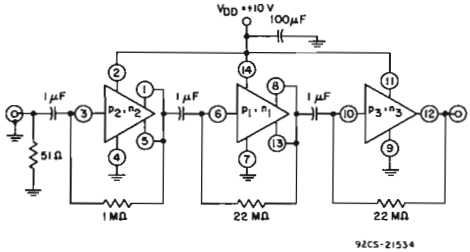


Fig. 16— High-gain amplifier uses cascaded COS/MOS transistor-pair in CA3600E.

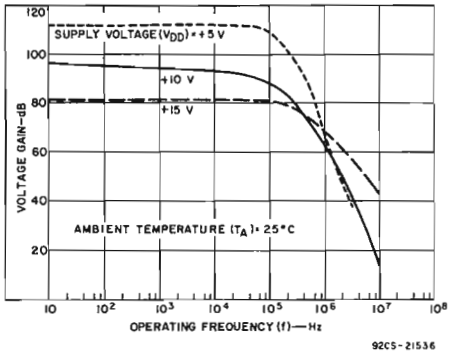


Fig. 17— Typical voltage gain vs. operating frequency characteristics for three-stage COS/MOS transistor-pair amplifier in Fig. 16.

Post-Amplifiers For Op-Amps

COS/MOS transistor-pairs can be advantageously applied as post-amplifiers for op-amps. Because the input impedance of the COS/MOS pair is comparatively high, the op-amp operates under essentially unloaded conditions. Each COS/MOS pair can sink and source output current up to about 10 mA. Additionally, the op-amp output can be directly coupled to bias the COS/MOS pair. A detailed description of the subject has been published previously.[2]

The schematic diagram in Fig. 18 shows a COS/MOS transistor-pair serving as a post-amplifier to an RCA-CA3080 Operational Transconductance Amplifier.[3] The approximate 30-dB gain in a single COS/MOS transistor-pair is an added increment to the 100-dB gain in the CA3080, yielding a total forward gain of about 130 dB. The open-loop slew rate of the circuit in Fig. 19 is approximately 65 V/μs. When compensated for the unity-gain voltage-follower mode shown in Fig. 19, the slew rate is about 1 V/μs. For greater current output, the two remaining transistor pairs of the CA3600E may be connected in parallel with the single stages shown in Figs. 18 and 19.

The use of the two-stage COS/MOS post-amplifier shown in Fig. 20 increases the total open-loop gain of the system to about 160 dB (100,000,000X). Open-loop slew rate remains at about 65 V/μs. A slew rate of about 1 V/μs is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 21. These circuits operate in concert with stability.

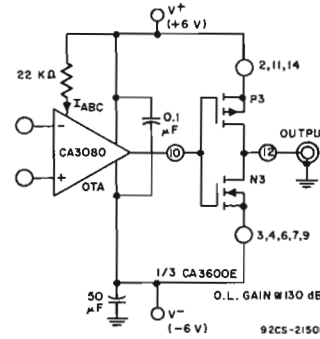


Fig. 18— COS/MOS transistor-pair used as post-amplifier to op-amp in open-loop circuit.

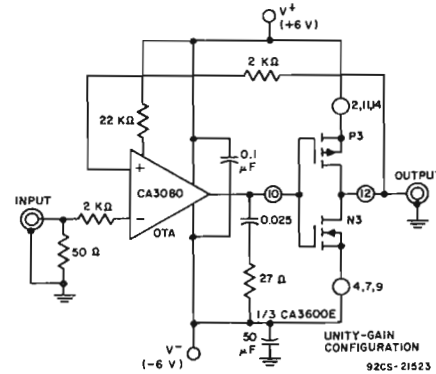


Fig. 19— COS/MOS transistor-pair used as post-amplifier to op-amp in unity-gain circuit.

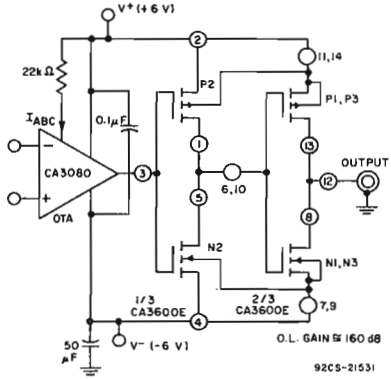


Fig. 20– COS/MOS transistor-pairs used as two-stage post-amplifier to op-amp in open-loop circuit.

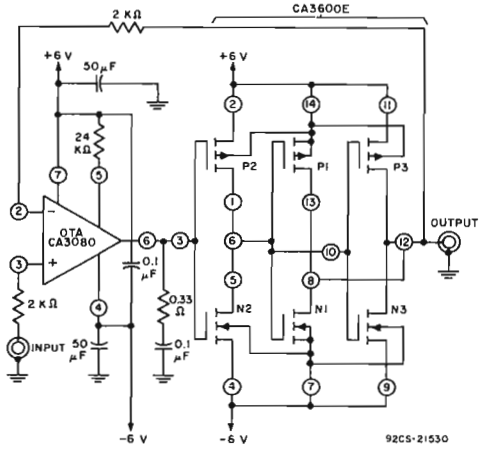


Fig. 21– Unity-gain amplifier uses COS/MOS transistor-pairs as two-stage post-amplifier to op-amp.

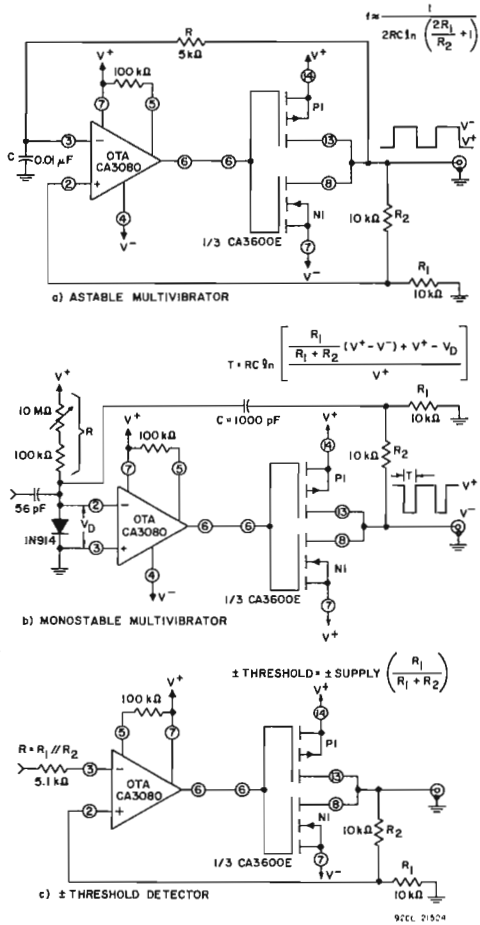


Fig. 22– Multistable circuits using COS/MOS transistor-pairs.

Multivibrators, Threshold Detectors, and Comparators

Descriptions of several circuits using COS/MOS transistor-pairs in both monostable and astable multivibrators have been published.[4,5] The characteristics of COS/MOS pairs are also ideal for mating with micropower op-amps in circuits such as the precision multistable circuits shown in Fig. 22. In these circuits precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080 Operational Transconductance Amplifier.[2,3] Moreover, speed vs. power consumption tradeoffs can be made by adjustment of the Amplifier-Bias-Current (I_{ABC}) supplied to terminal 5 of the CA3080. The quiescent power consumption of the circuits shown in Fig. 22 is typically 6 mW, but can be made to operate in the micropower region by suitable modifications.

The schematic diagram of a programmable micropower comparator, shown in Fig. 23 employs the combination of an op-amp (CA3080A) and COS/MOS transistor-pairs in the CA3600E. Quiescent power consumption of the circuit is about 10 μW(typ.). When the comparator is strobed "ON", transistor P1 is driven into conduction and the OTA becomes active. Under these conditions, the circuit consumes 420 μW and responds to a differential-input signal in about 8 μs. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 ns but the power consumption is increased to 21 mW. The differential amplifier input common-mode range for this circuit is −1 V to +10.5 V. Voltage gain of this micropower comparator is typically 130 dB.

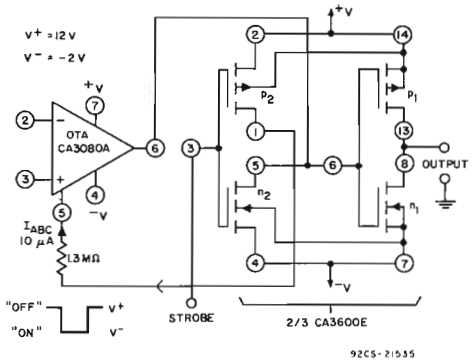


Fig. 23— Programmable micropower comparator.

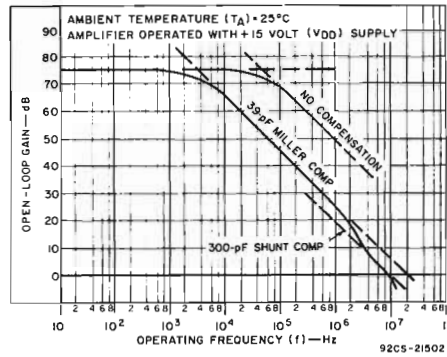


Fig. 25— Open-loop gain characteristic for op-amp in Fig. 24.

Operational Amplifiers

COS/MOS transistor-pairs can be used in conjunction with a bipolar transistor-array IC to build an op-amp as shown in Fig. 24. It is particularly suited for single-supply operation (e.g., mobile and aircraft service). The op-amp is unique in that it is responsive to small-signal ground-referenced inputs and the output stage can easily be driven within 1 mV of ground potential. Its open-loop gain characteristics are shown in Fig. 25; the open-loop slew rate is approximately 30 V/μs.

This circuit is ideal for use as a unity-gain voltage-follower and has been described for operation in connection with a 9-Bit Single-Supply Digital-to-Analog Converter (DAC) using COS/MOS transistors in the resistor-network switches.[6]

The op-amp in Fig. 24 has three stages; its first stage is a differential input circuit using two p-channel transistors (P_4,P_5) in a CA3600E. The second stage is an n-p-n

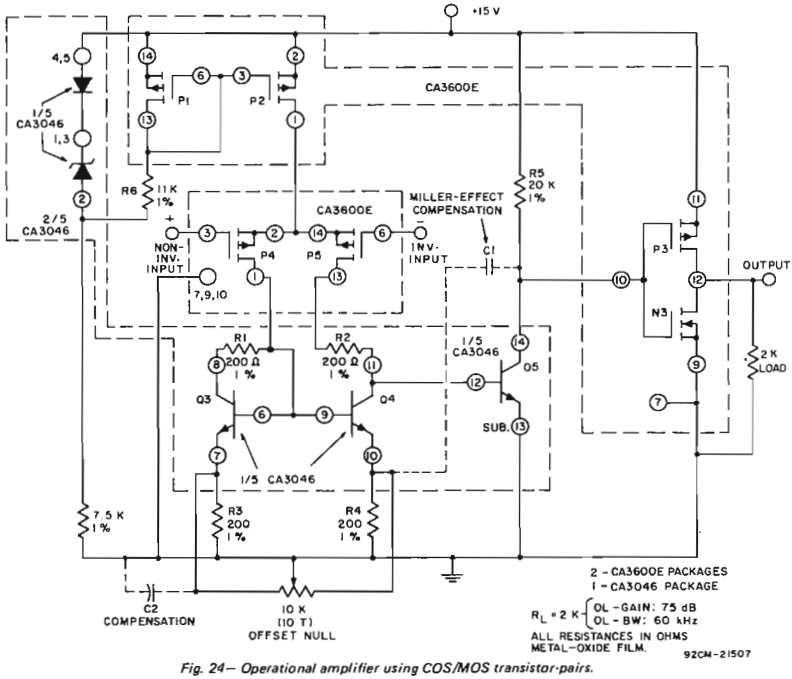


Fig. 24— Operational amplifier using COS/MOS transistor-pairs.

transistor (Q_5) and the output stage is a COS/MOS transistor-pair (P_3,N_3) operating in the manner described above. A constant current of about 400 μA is established in the differential input stage by the zener network in the upper-left portion of Fig. 24. The zener network energizes a current mirror comprised of two p-channel transistors (P_1,P_2) to establish constant-current flow in the differential amplifier stage (P_4,P_5). The drain load for the differential amplifier consists of resistors R_1–R_4 and a current mirror (Q_3 Q_4) to optimize conditions for balanced operation of the differential amplifier. The operating theory of current-mirror circuits has been described in reference [2]. Amplifier voltage-offset is nulled with the 10-kilohm balance potentiometer. The second-stage current is established by R_5, and is selected to approximate the first-stage current level (400 μA), to assure similar positive and negative slew rates. The amplifier is shown driving a 2-kilohm load, a typical value used with monolithic op-amps. Voltage gain varies inversely with the choice of load resistance.

The amplifier can be compensated with a single capacitor (C_1), connected as shown by the dotted lines. However, optimum compensation for the unity-gain non-inverting mode is provided by two capacitors: Miller Effect feedback through a 39-pF capacitor C_1 (connected as shown), and a 300-pF capacitor connected between terminals 7 and 13 of the CA3046 transistor array to shunt one-half the driving current. Fig. 25 shows the open-loop gain characteristics with compensation for unity-gain operation. When the amplifier is operated as a voltage-follower, it is recommended that a 1-kilohm resistor, shunted with a 150-pF capacitor, be connected between the amplifier output terminal and terminal 6 of P_5 to avoid a potential latch situation involving the integral gate-protection network. The circuit can also be latched if either input terminal is driven more than about 0.7 volt below ground potential. This latch situation can be avoided by connecting a 1N914 diode from each input terminal to ground, with the diode anode grounded.

Analog Timer

The CA3600E is useful in the design of analog timer circuits. A typical circuit is shown in Fig. 26. For purposes of explanation, let it be assumed that capacitor C_1 initially is in a completely discharged condition; terminal 10, therefore, is initially at ground potential and transistor N_3 is non-conductive. The circuitry at the left of terminal 10 provides a source of constant-current flow through P_1 to charge capacitor C_1 increasingly positive with respect to ground. After the passage of time (T), capacitor C_1 is charged sufficiently in the positive direction so that transistor N_3 is driven into conduction by its gate and the lamp is lighted to signify the end of the time-delay period. The circuit is reset by momentarily closing switch S_1 to discharge capacitor C_1 through R_4. Resistor-divider network R_1,R_2 establishes the supply voltage to a constant-current network comprised of resistor R_3 and the series-connected COS/MOS pair N_2,P_2, biased for linear operation by resistor R_b as previously described. This combination is connected to the gate terminal (No. 6) of transistor P_1 to form a current mirror, i.e., the current flowing through P_1 to charge C_1 will be essentially equal to the constant-current flow established through R_3, N_2, and P_2. A description of current-mirror operation with MOS transistors is given subsequently.

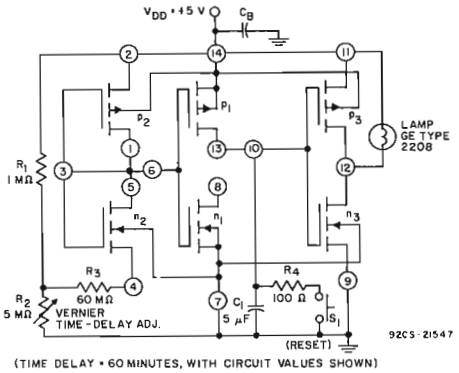


Fig. 26– Analog timer using CA3600E.

Oscillator Circuits

Oscillator circuits using COS/MOS transistor-pairs have been widely used for several years in clock and watch circuits because of their low power consumption and good frequency stability. Details of their operating theory and characteristics have been published.[5,7]

The design of COS/MOS oscillator circuits, like the design of any oscillator circuit, involves the provision of an amplifying section to operate compatibly with an appropriate feedback network. A single stage amplifier using a COS/MOS transistor-pair has already been described. A suitable feedback network to insure stable oscillator performance is easily added, as illustrated in connection with the crystal oscillator circuit shown in Fig. 27. The familiar pi-network has been connected between the input and output terminals, points "D" and "G", to provide the required 180° phase shift for stable oscillator performance. The frequency-determining crystal is an integral part of the pi-network feedback circuit. The resistors R_1 and R_2 decrease the total power consumption of the oscillator at a particular supply voltage and enhance the frequency stability. Variable frequency oscillators can be built by replacing the crystal with an appropriate inductance and tuning the pi-network by conventional means.

Current Mirrors Using MOS Transistors

Monolithic linear IC's using bipolar transistors frequently employ so-called "current-mirror" circuits. The theory and practical applications of current mirrors using bipolar transistors have been described in the literature.[2] As shown in

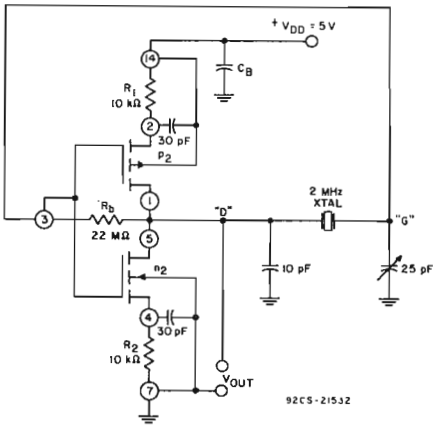


Fig. 27– Typical crystal-oscillator circuit using COS/MOS transistor-pair (1/3 CA3600E).

Fig. 28, a rudimentary form of "current-mirror" consists of a transistor Q_1 with a second transistor Q_2 connected as a diode. When both transistors have identical characteristics, a current I_1 forced to flow through Q_2 produces a current (I_2) of equal magnitude to flow in the collector of Q_1 (provided there is sufficient collector potential for Q_1). In a common form of application, a source of potential is used to force

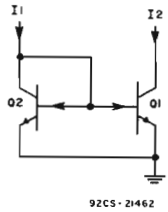


Fig. 28– Current mirror using n-p-n bipolar transistors.

constant-current flow I_1, and thus to establish the flow of constant current I_2 through Q_1. Arrangements of this generic current-mirror type are frequently used when Q_1 acts as the common-emitter impedance in a differential-amplifier circuit.

MOS transistors are also applicable as current mirrors, as shown in Fig. 29. The diode-connected MOS transistor N_2 functions as a transistor with 100 per-cent feedback. Therefore, the gate-to-source voltage (V_{GS}) in N_2 retains control of the drain current as in normal transistor action, i.e., $I_D \cong g_{fs}V_{GS}$, where g_{fs} is the forward transconductance of the device. If a current I_1 is forced into the diode-connected transistor (N_2), the gate-to-source voltage will rise until equilibrium is reached. Thus, a gate-to-source voltage is established in N_2 such that N_2 "sinks" the applied current I_1.

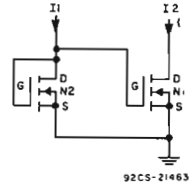


Fig. 29– Current mirror using n-channel MOS transistors.

If the gate and source terminals of another transistor (N_1) are connected in shunt with the gate and source terminals of N_2, as shown in Fig. 29, N_1 is also able to "sink" a mirror current approximately equal to that flowing in the drain lead of the diode-connected transistor N_2. It is assumed that both MOS transistors have identical characteristics, a prerequisite that is essentially established by the monolithic IC fabrication technology used in manufacturing the CA3600E COS/MOS transistor array.

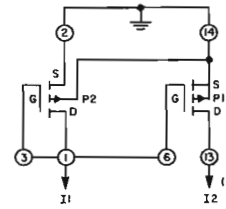


Fig. 30– Current mirror using p-channel MOS transistors in CA3600E.

Current mirrors can also be designed with p-channel MOS transistors as illustrated by the arrangement in Fig. 30 using transistors in the CA3600E. The characteristics of a current mirror using the p-channel transistors in the CA3600E are superior to those which can be achieved with a current mirror using the n-channel transistors because the characteristics of the p-channel transistors are more nearly matched. The data

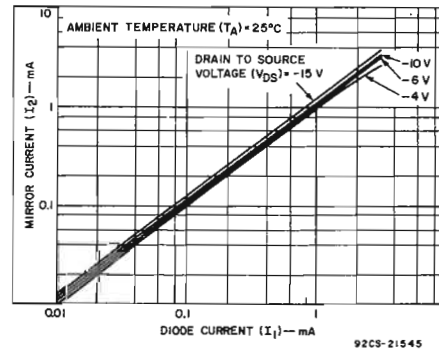


Fig. 31– Characteristics of current mirror circuit of Fig. 30 using p-channel transistors.

contained in Fig. 31 show the high degree of tracking between I_1 and I_2 for several values of drain voltage V_D. Fig. 32 also illustrates the fact that this high degree of tracking between I_1 and I_2 can be maintained to within about one per-cent despite wide variations in ambient temperature.

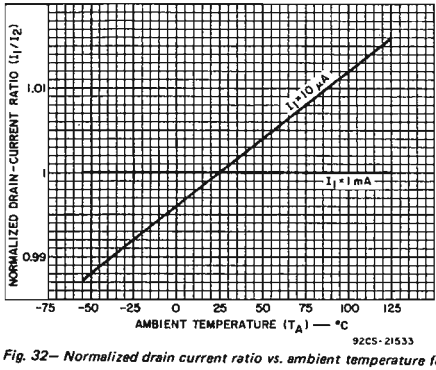


Fig. 32– Normalized drain current ratio vs. ambient temperature for typical current mirror using p-channel transistors (Fig. 30).

The op-amp circuit in Fig. 24 contains an illustrative example of a current-mirror circuit using two p-channel transistors in the CA3600E. Transistor P_2 serves as a constant-current source (≅ 400 μA) for the differential amplifier, consisting of transistors P_4 and P_5 and their drain-load network. Transistor P_2 is in a "mirrored" connection with transistor P_1. A stabilized source of supply potential is developed across the zener diode (terminals 11 and 12 of the CA3083) and drives about 400 μA of current through R_6 and P_1.

Complementary Current Mirrors Using COS/MOS Transistor-Pairs

COS/MOS transistor-pairs can be applied advantageously in the design of Complementary Current-Mirrors, as shown in Fig. 33. Transistors P_1 and N_1 are series-connected and biased for linear operation as previously described, so that there is a current flow I_{D1} through P_1 and N_1. The potential developed between terminals 13 and 14 is applied as gate-source (2,3) voltage for P_2, forcing "mirror" operation of P_2 to produce a current source $I_{D2\text{-}P}$ equal to I_{D1}. Likewise, the potential developed between terminals 7 and 8 is applied as gate-source (3,4) voltage for N_2 forcing "mirror" operation of N_2 to produce a current-sink $I_{D2\text{-}N}$ equal to I_{D1}.

A variant of this complementary current mirror is used in the analog timer circuit shown in Fig. 26. Transistors P_2 and N_2 are series-connected together with a 60-megohm resistor to establish their drain current at 5 nA. The potential developed across terminals 1 and 2 also appears as the gate-source voltage for transistor P_1, thereby establishing a mirror-current source of 5 nA at terminal 13 to charge capacitor C_1 linearily. In this circuit, the "mirrored" current-sink available at terminal 8 (transistor N_1) is unused. This type of current-mirror configuration is exceptionally stable with temperature variations.

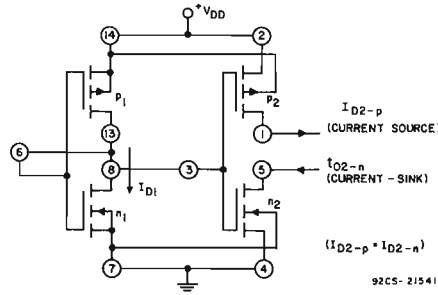


Fig. 33– Complementary current mirrors using COS/MOS transistor-pairs in CA3600E.

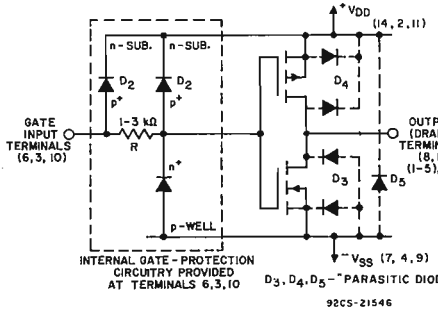


Fig. 34– Integral protection circuits used in CA3600E.

Considerations in Handling CA3600E Devices

Failure of the gate-channel oxide was a persistent problem in early MOS devices. The breakdown of the oxide is generally in the order of 100 volts, and the dc resistance is in the order of 10^{12} ohms. Because of this extremely high resistance, even a very-low-energy source (such as static charge) is capable of developing sufficient voltage to cause damage. Furthermore, the oxide can be punctured and damaged by a single voltage excursion beyond the breakdown limit.

Fig. 34 shows a protection circuit[5,8] which is incorporated at each gate-lead of the CA3600E. A typical value of 1 to 3 kilohms is used for the input resistor R, which functions in combination with the capacitance of the gate and the associated protective diode to integrate and clamp input voltages to a safe level. This circuit also shows the "substrate diodes" (D_3, D_4, and D_5) which provide protection to the MOS channels at the output terminals.

Although the gate-protection system is very effective in guarding against damage due to static charges, it is prudent to observe the following precautions:[5,9]

1. The leads of devices should be in contact with a conductive material, except when being tested or in actual operation. A conductive material such as "ECCOSORB LD26"* or equivalent is suggested for use during storage and/or handling. Devices should not be

inserted in non-conductive containers such as conventional plastic "snow" or trays.

* Trade Mark: Emerson and Cumming, Inc.

2. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
3. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
4. Signals from low-impedance sources should not be applied to the gate terminals while the power supply is off. As a corollary, it follows that the power supply should not be turned off while a signal from a low-impedance source is being applied to any gate terminal. When the V_{DD} supply is off, the positive "back-bias" voltage is removed from the cathode of diode D_2 (see Fig. 34). Consequently, an input signal with positive-going polarity can drive D_2 into conduction. Under these conditions a low-impedance signal source can provide sufficient current to permanently damage D_2 and/or melt aluminum interconnection paths. Therefore, if, in any system design using the CA3600E, any gate input excursion is expected to exceed $+V_{DD}$ or fall below $-V_{SS}$, the current through the input diodes should be limited to 100 μA.
5. All unused gate-input terminals should be connected to V_{SS} (ground). When source terminals (e.g., Nos. 2 and 11) of p-channel transistors are unused in circuitry, they should be connected to terminal No. 14. Likewise, when source terminals (e.g., Nos. 4 and 9) of n-channel transistors are unused, they should be connected to terminal No. 7.
6. After CA3600E units have been mounted on circuit boards, proper handling precautions should still be observed. Until these subassemblies are inserted into a complete system, the board is no more than an extension of the device leads mounted on the board. It is a good practice to place conductive tape or jumpers on circuit-board terminals to "ground" gate terminals.
7. In some applications of the CA3600E separate positive and negative power supplies may be employed (e.g., see Fig.22). In such applications provisions must be made so that the positive supply voltage is applied prior to the application of negative supply voltage and vice versa on shutdown. This precaution is necessary to avoid possible damage due to "latching" involving the substrate and protective diode circuits.

REFERENCES

1. "RCA Solid State Power Circuits Designer's Handbook," RCA Solid State Division Technical Series SP-52.
2. "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers," RCA Solid State Division Application Note ICAN-6668.
3. Technical Bulletin for RCA Types CA3080 and CA3080A, File No. 475 RCA Solid State Division.
4. "Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits," RCA Solid State Division Application Note ICAN-6267.
5. "COS/MOS Integrated Circuits Manual," RCA Solid State Division Technical Series CMS-271.
6. "Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC," RCA Solid State Division Application Note ICAN-6080.
7. "Timekeeping Advances Through COS/MOS Technology," RCA Solid State Division Application Note ICAN-6086.
8. "Gate-Oxide Protection Circuit in RCA COS/MOS Digital Integrated Circuits," RCA Solid State Division Application Note ICAN-6218.
9. "Handling Considerations for MOS Integrated Circuits," RCA Solid State Division Application Note ICAN-6000.

14-Lead Dual-In-Line
Plastic Package

H-1517

High-Current N-P-N Transistor Arrays

Four Individual Sealed-Junction High-Current N-P-N Transistors

Features:

- High Current – 1 A
- High Breakdown Voltage:
  CA3725G = 80 V dc min. $V_{(BR)CES}$ @ I_C = 10 μA
  CA3724G = 70 V dc min. $V_{(BR)CES}$ @ I_C = 10 μA
- Fast Switching Speeds:
  t_{on} = 30 ns typ. @ I_C = 500 mA
  t_{off} = 36 ns typ. @ I_C = 500 mA
- "Hermetic Chip" Construction
- Silicon Nitride Passivated
- Platinum Silicide Ohmic Contacts
- Gold Chip-Metallization
- Electrically similar and pin compatible with industry types MPQ3724, MPQ3725; FPQ3724, FPQ3725; DH3724, DH3725; SP3724, SP3725 in similar packages

The RCA-CA3724G and -CA3725G are high-current n-p-n transistor arrays each containing 4 individual sealed-junction high-current n-p-n transistors. They are intended for high-current, high-speed switching and driver applications.

These devices are alike except for breakdown voltage ratings.

The CA3724G and CA3725G are supplied in a 14-lead dual-in-line plastic package and operate over the full military temperature range of −55°C to +125°C. The transistor chips used in these packages are of the sealed-junction type to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure.

The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multi-layered, highly corrosion-resistant, terminal-connection system of unique design is employed.

Applications:

- Core-Memory Driver
- High-Speed Switching
- High-Current LED Driver
- High-Voltage Switching
- Relay and Solenoid Driver
- Lamp Driver

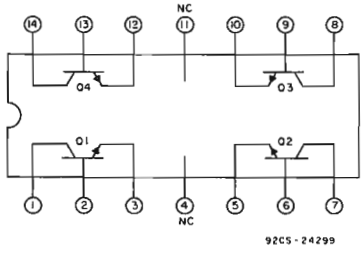


Fig. 1—Terminal diagram (top view).

MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^oC$

		CA3724G	CA3725G	
COLLECTOR-TO-EMITTER VOLTAGE With Base Open	V_{CEO}	40	50	V
COLLECTOR-TO-BASE VOLTAGE With Emitter Open	V_{CBO}	70	80	V
EMITTER-TO-BASE VOLTAGE With Collector Open	V_{EBO}	6	6	V
COLLECTOR CURRENT	I_C	1.0	1.0	A
POWER DISSIPATION: At T_A up to 25°C:	P_D			
For Each Transistor		1.0	1.0	W
Total Package		2.0	2.0	W
At T_A above 25°C derate linearly		20		mW/°C
AMBIENT TEMPERATURE RANGE:				
Operating		−55 to +125	−55 to +125	°C
Storage		−65 to +150	−65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/32" (3.17 mm) from seating plane for 10 s max.		300	300	°C

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$

Characteristic	Symbol	Test Conditions	Limits						Units
			CA3724G			CA3725G			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-to-Emitter Sustaining Voltage *	$V_{CEO}(sus)$	I_C = 10 mA, I_B = 0	40	–	–	50	–	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CES}$	I_C = 10 μA, I_B = 0	70	–	–	80	–	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	70	–	–	80	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	6	–	–	6	–	–	V
Base-to-Emitter Saturation Voltage *	$V_{BE}(sat)$	I_C = 500 mA, I_B = 50 mA	0.75	–	1.0	0.75	–	1.0	V
Collector-to-Emitter Saturation Voltage *	$V_{CE}(sat)$	I_C = 500 mA, I_B = 50 mA	–	–	0.5	–	–	0.5	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 40 V, I_E = 0	–	–	1.7	–	–	1.7	μA
Static Forward-Current Transfer * Ratio (Beta)	h_{FE}	I_C = 100 mA, V_{CE} = 1.0 V I_C = 500 mA, V_{CE} = 1.0 V I_C = 1 A, V_{CE} = 1.0 V	35 30 20	– – –	– – –	35 30 20	– – –	– – –	
Small-Signal Forward-Current Transfer Ratio	h_{fe}	I_C = 50 mA, V_{CE} = 10 V f = 100 MHz	2.0	–	–	2.0	–	–	
Turn-On Time (See Test Ckt. Fig. 2)	t_{on}	I_C = 500 mA, I_{B1} = 50 mA	–	–	40	–	–	40	ns
Turn-Off Time (See Test Ckt. Fig. 2)	t_{off}	I_C = 500 mA, $I_{B1} = I_{B2}$ = 50 mA	–	–	60	–	–	60	ns
Emitter-to-Base Capacitance	C_{eb}	I_C = 0, V_{EB} = 0.5 V	–	95	–	–	95	–	pF
Collector-to-Base Capacitance	C_{cb}	I_E = 0, V_{CB} = 10 V	–	12	–	–	12	–	pF

* Pulse Conditions: width = 300 μs; duty cycle = 1%

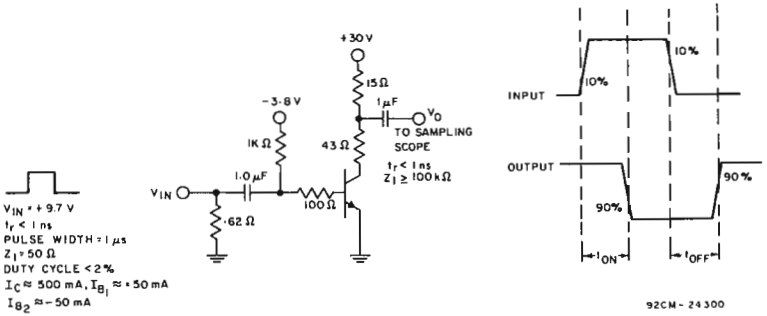


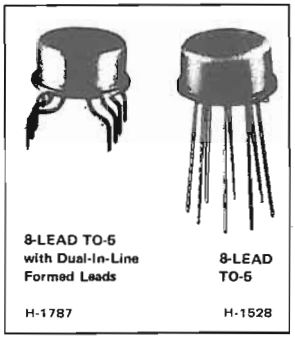
Fig. 2—Switching time test circuit.

RCA Solid State Division

Linear Integrated Circuits

Monolithic Silicon

Premium Types CA6078AS, CA6078AT CA6741S, CA6741T



8-LEAD TO-5 with Dual-In-Line Formed Leads H-1787

8-LEAD TO-5 H-1528

Operational Amplifiers

CA6078AT — Micropower Type
CA6741T — General-Purpose Type

For Applications where Low Noise (Burst + 1/f) is a Prime Requirement

Virtually free from "popcorn" (burst) noise: device rejected if any noise burst exceeds 20 μV (peak), referred to input over a 30-second time period.

RCA-CA6078AT and CA6741T* are low-noise linear IC operational amplifiers that are virtually free of "popcorn" (burst) noise.

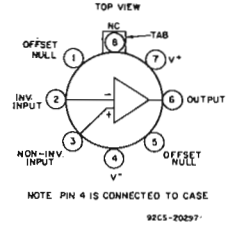
These low-noise versions of the CA3078AT and CA3741T are a result of improved processing developments and rigid burst-noise inspection criteria. A highly selective test circuit (See Fig. 2) assures that each type meets the rigid low-noise standards shown in the data section. This low-burst-noise property also assures excellent performance throughout the 1/f noise spectrum.

In addition the CA6078AT and CA6741T offer the same features incorporated in the CA3078AT and CA3741T respectively, including output short-circuit protection, latch-free operation, wide common-mode and differential-mode signal ranges, and low-offset nulling capability.

For detailed data, characteristics curves, schematic diagram, dimensional outline, and test circuits, refer to the Operationel Amplifier Data Bulletins File No. 531 and 535. In addition, for details of considerations in burst-noise measurements, refer to Application Note, ICAN-6732, "Measurement of Burst ("Popcorn") Noise in Linear IC's".

The CA6078AT and CA6741T utilize the hermetically sealed 8-lead TO-5 type package. The CA6078AT and the CA6741T can also be supplied on request with dual-in-line formed leads. These types are identified as the CA6078AS and CA6741S. This formed-lead configuration conforms to that of the 8-lead dual-in-line (Mini—Dip) package. For terminal arrangements, see page 4.

*Formerly Dev. No. TA5807X and TA6029 respectively.



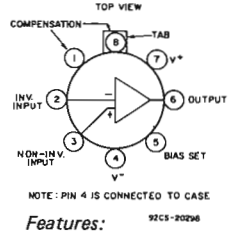
CA6741T

Applications:

- Low-noise AC amplifier
- Narrow-band or band-pass filter
- Integrator or differentiator
- DC amplifier
- Summing amplifier

Features:

- Internal phase compensation
- Input bias current: 500 nA max.
- Input offset current: 200 nA max.
- Open-loop voltage gain: 50,000 (94 dB) min.
- Input offset voltage: 5 mV max.



CA6078AT

Applications:

- Portable electronics
- Medical electronics
- DC amplifier
- Narrow-band or band-pass filter
- Integrator or differentiator
- Instrumentation
- Telemetry
- Summing amplifier

Features:

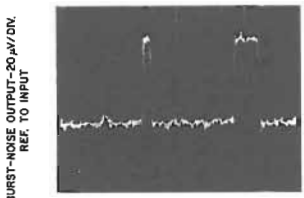
- Open-loop voltage gain: 40,000 (92 dB) min.
- Input offset voltage: 3.5 mV max.
- Operates with low total supply voltage: 1.5 V min. (± 0.75 V)
- Low quiescent operating current: adjustable for application optimization
- Input bias current: adjustable to below 1 nA

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

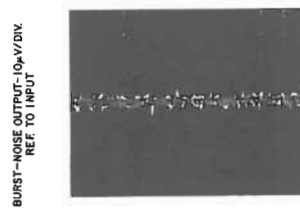
	CA6741T	CA6078AT
DC Supply Voltage (between V^+ and V^- terminals)	44 V	36 V
Differential-Mode Input Voltage	±30 V	±6 V
Common-Mode DC Input Voltage▲	±15 V	V^+ to V^-
Device Dissipation:		
Up to 75°C (CA6741T), Up to 125° (CA6078AT)	500 mW	250 mW
Above 75°C	Derate linearly 5 mW/°C	
Temperature Range:		
Operating	−55 to +125 °C	−55 to +125 °C
Storage	−65 to +150 °C	−65 to +150 °C
Output Short-Circuit Duration●	No limitation	No limitation
Lead Temperature (During soldering):		
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm)		
from case for 10 seconds max.	300 °C	300 °C

▲If Supply Voltage is less than ±15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

●Short circuit may be applied to ground or to either supply.



a. Typ. device with high-burst-noise characteristic.



b. Typ. device controlled for burst noise.

Fig.1—Typ. waveforms of type with high burst noise and type controlled for burst noise.

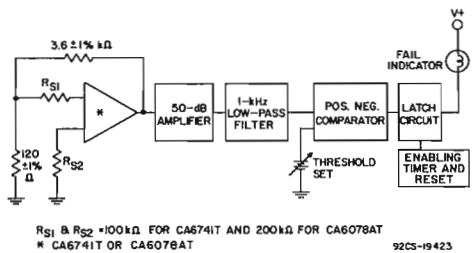


Fig.2—Block diagram of burst-noise "popcorn" test equipment.

ELECTRICAL CHARACTERISTICS – CA6078AT, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
		Supply Volts: $V^+ = 6$, $V^- = -6$ $T_A = 25^oC$, $I_Q = 20\ \mu A$	MIN.	TYP.	MAX.	
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz $R_{S1} = R_{S2} = 200\ k\Omega$	Device is rejected if the total noise voltage (burst + $1/f$), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3078AT Data Bulletin, File No. 535.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	0.7	3.5	mV
Input Offset Current	I_{IO}		–	0.5	2.5	nA
Input Bias Current	I_{IB}		–	7	12	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 10\ k\Omega$	40,000	100,000	–	
		$V_O = \pm 4V$	92	100	–	dB
Common-Mode Input Voltage Range	V_{ICR}	$V^+ = V^- = 15$ V	±14	–	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	80	115	–	dB
Output Voltage Swing	$V_{O(P\text{-}P)}$	$R_L \geq 10\ \Omega$	±13.7	±14.1	–	V
		$R_L \geq 2\ k\Omega$	–	±14	–	
Supply Current	I_Q		–	20	25	μA

ELECTRICAL CHARACTERISTICS – CA6741T, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
		Supply Volts; $V^+ = 15$, $V^- = -15$ $T_A = 25^oC$	MIN.	TYP.	MAX.	
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz $R_{S1} = R_{S2} = 100\ k\Omega$	Device is rejected if the total noise voltage (burst + $1/f$), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3741T Data Bulletin, File No. 531.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	1	5	mV
Input Offset Current	I_{IO}		–	20	200	nA
Input Bias Current	I_{IB}		–	80	500	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2\ k\Omega$	50,000	200,000	–	
		$V_O = \pm 10$ V	94	106	–	dB
Common-Mode Input Voltage Range	V_{ICR}		±12	±13	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\ \Omega$	70	90	–	dB
Output Voltage Swing	$V_{O(P\text{-}P)}$	$R_L \geq 10\ k\ \Omega$	±12	±14	–	V
		$R_L \geq 2\ k\ \Omega$	±10	±13		
Supply Current	I_Q		–	1.7	2.8	mA

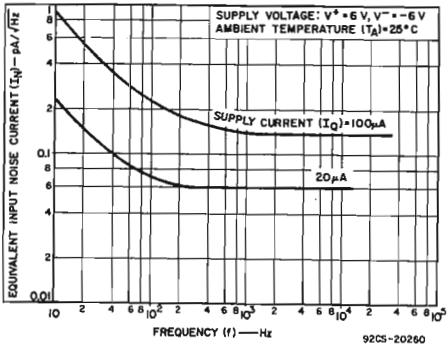


Fig.3—I_N vs. Frequency for CA6078AT.

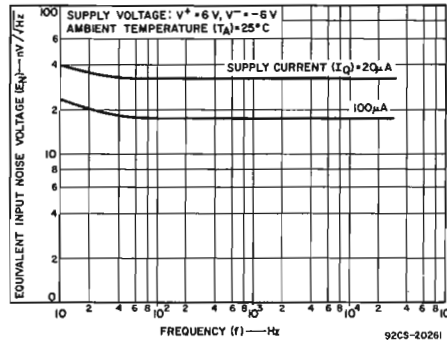


Fig.4—E_N vs. Frequency for CA6078AT.

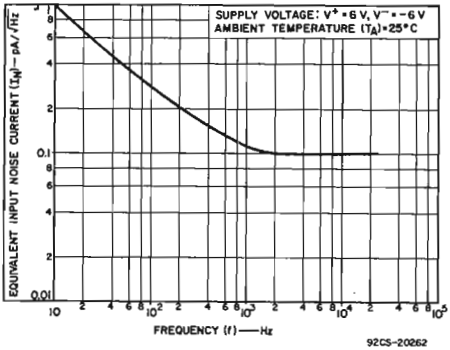


Fig.5—I_N vs. Frequency for CA6741T.

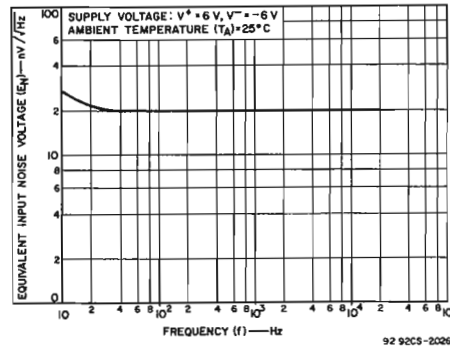


Fig.6—E_N vs. Frequency for CA6741T.

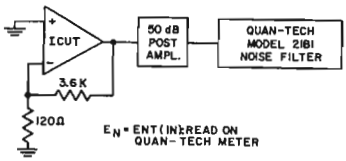


Fig.7—Test block diagram for E_N.

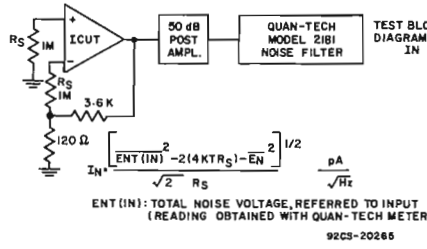


Fig.8—Test block diagram for I_N.

RCA Solid State Division

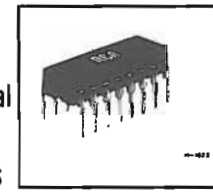
Digital Integrated Circuits

CD2500E
CD2501E
CD2502E
CD2503E

BCD to 7-Segment Decoder-Drivers

Monolithic Silicon

30mA and 80mA/Segment DECODER-DRIVERS For Use With Low-Voltage Digital Display Devices, Lamps, and Relays



RCA CD2500E series 7-Segment Decoder-Drivers are monolithic MSI integrated circuits which decode BCD (8-4-2-1 code) inputs to 7-line outputs representing a decimal number from 0 to 9 on 7-segment incandescent display devices.

RCA CD2500E and CD2501E are 30 mA per-output-line devices designed for use with incandescent display devices such as the RCA DR2000 and DR2010. The CD2500E, in addition to the outputs for the 7-segment display device, has a decimal point output; the CD2501E also has a special-feature, a terminal to provide for ripple blanking output and intensity control input. The ripple blanking output blanks out all non-significant zeroes in the numerical display. The ripple blanking output terminal is also available for use as an intensity control input from an external variable pulse-width control source, as shown in Fig. 7.

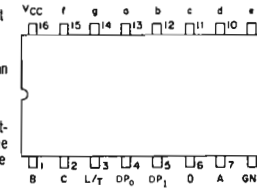
RCA CD2502E and CD2503E are 80 mA-per-line versions of the CD2500E and CD2501E, respectively, and are designed for use with high-current lamps and relays.

RCA CD2500E series devices are supplied in 16-lead dual in-line plastic packages which can be used over the operating temperature range of 0°C to +75°C.

DP_0 = Decimal Point Output
DP_I = Decimal Point Input

DP_I must be supplied from an external source

CD2500E and CD2502E perform the inverter-driver function necessary to energize the decimal point filament in the display device.



92CS-4177

Fig. 1 - CD2500E and CD2502E (with decimal point)

FEATURES:

- High current sinking capability for direct display driving
- Intensity control provision
- BCD inputs are compatible with commercially available DTL & TTL devices
- Lamp test provision
- 5 V power supply
- Clamp diodes on all inputs
- Lamp supply up to +8 volts
- Ripple blanking capability
- Decimal point output
- Over-range detection (automatic blanking of display device when BCD input > 9)

RB_0 = Ripple-Blanking Output & Intensity Control Input
RB_I = Ripple-Blanking Input

92CS-15621

Fig. 2 - CD2501E and CD2503E (with ripple blanking and intensity control provision)

ABSOLUTE MAXIMUM RATINGS at 25° C unless otherwise specified:

Power Supply Voltage:
- Continuous (0° C to + 75° C) . . . . . − 0.5 to + 5.5 V
- Pulsed (duration 1 second) . . . . . − 0.5 to + 8 V

Input Voltage . . . . . − 0.5 to + 5.5 V

Ontput Voltage (open collector transistor) . . − 0.5 to + 8 V

Operating Temperature Range . . . . . 0° C to + 75° C

Storage Temperature Range . . . . . − 65 °C to + 150° C

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . +265° C

ELECTRICAL CHARACTERISTICS at Ambient Temperature (T_A) Indicated

CHARACTERISTICS	SYMBOLS	MEASUREMENT TERMINALS	TEST CONDITIONS		0° C		+ 25° C			+ 75° C		UNITS
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Input High Voltage (Logic 1)	V_{IH}	1, 2, 5, 6, & 7	Input high threshold voltage		2.0	–	2.0	–	–	2.0	–	V
		3	V_{CC} = 4.75 V, I_{IH} = 0 Ground all other inputs		2.4	–	2.4	–	–	2.4	–	V
Input Low Voltage (Logic 0)	V_{IL}	1, 2, 5, 6, & 7	Input low threshold voltage		–	0.85	–	–	0.85	–	0.85	V
		3			–	0.45	–	–	0.45	–	0.45	
Input Forward Current	I_{IL}	1, 2, 5, 6, & 7	V_F = 0.45 V	V_{CC} = 5.25 V	–	– 1.6	–	– 1.0	– 1.6	–	– 1.6	mA
		3 { CD2501E, CD2503E			–	– 10.0	–	–	– 10.0	–	– 10.0	
		3 { CD2500E, CD2502E			–	– 10.4	–	–	– 10.4	–	– 10.4	
		1, 2, 5, 6, & 7	V_F = 0 Terminal 3 only	V_{CC} = 4.75 V	–	– 1.41	–	–	– 1.41	–	– 1.41	mA
		3 { CD2501E, CD2503E			–	– 9.0	–	–	– 9.0	–	– 9.0	
		3 { CD2500E, CD2502E			–	– 9.4	–	–	– 9.4	–	– 9.4	
Input Reverse Current	I_{IH}	1, 2, 5, 6, & 7	V_{CC} = 5.25 V Terminal 3 grounded	V_R = 4.5 V	–	40	–	–	40	–	60	μA
				V_R = 2.4 V	–	40	–	–	40	–	40	
Output Low Voltage	V_{OL}	9 thru 15 { CD2500E, CD2501E and 4 of CD2500E	V_{CC} = 4.75 V, I_{OL} = 30 mA		–	0.40	–	0.30	0.40	–	0.40	V
		4 { CD2501E, CD2503E	V_{CC} = 5.25, I_{OL} = 3.2 mA		–	0.45	–	0.30	0.45	–	0.45	
			V_{CC} = 4.75, I_{OL} = 2.82 mA		–	0.45	–	0.30	0.45	–	0.45	
		9 thru 15 { CD2502E, CD2503E and 4 of CD2502E	V_{CC} = 4.75 V, I_{OL} = 80 mA		–	1.0	–	0.60	1.0	–	1.0	
Output High Voltage	V_{OH}	9 thru 15 – All types and 4 of { CD2500E, CD2502E	V_{CC} = 5 V, I_{OH} = 200 μA		8.0	–	8.0	–	–	8.0	–	V
		4–CD2501E, CD2503E	V_{CC} = 4.75 V, I_{OH} = – 240 μA		2.4	–	2.4	–	–	2.4	–	
Input Capacitance	C_{IN}	1, 2, 5, 6, & 7	V_{CC} = 5.0 V		–	–	–	3	5	–	–	pF
Power Supply Current Drain (Terminal 16)	I_{CC_L}	CD2501E, CD2503E	V_{CC} = 5.0 V (Segment Output Currents = 0)		–	–	–	48	–	–	–	mA
		CD2500E, CD2502E	Terminal 3 Grounded		–	–	–	50	–	–	–	

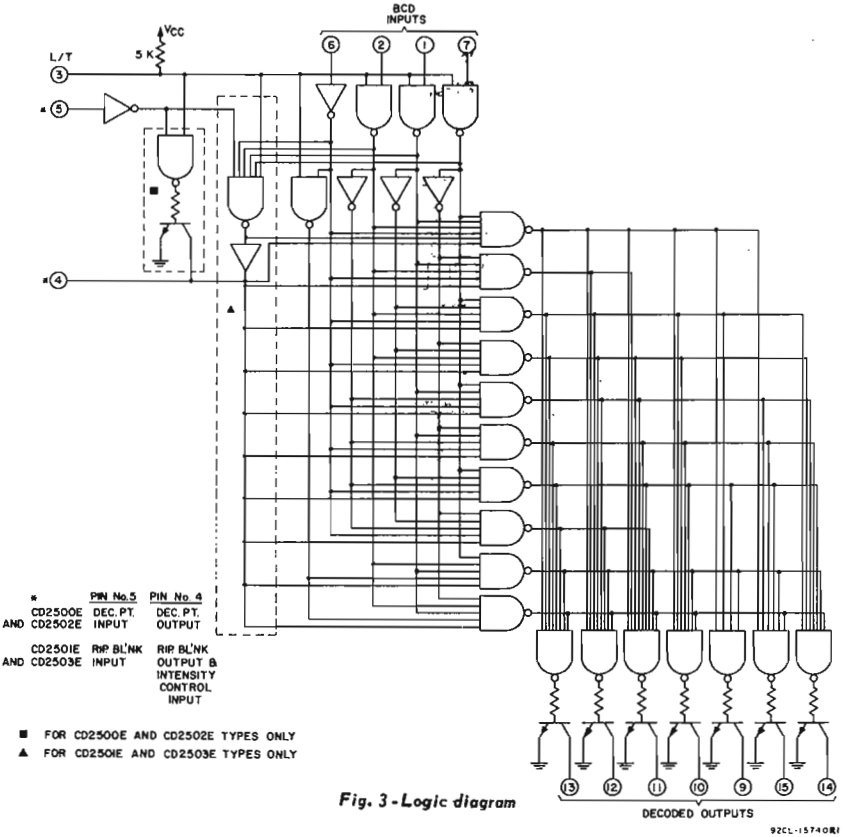
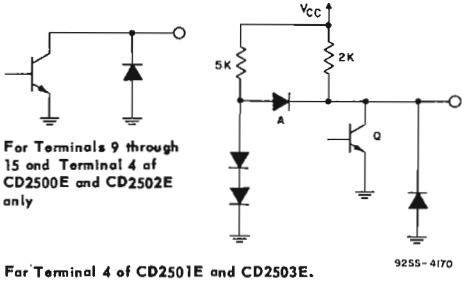


Fig. 3 - Logic diagram



For Terminals 9 through 15 and Terminal 4 of CD2500E and CD2502E only

For Terminal 4 of CD2501E and CD2503E.

Transistor Q is "turned on" when BCD code equals 0 and Terminal 5 is at "0 Level" (Grounded). When BCD code is between 0 and 9, transistor Q is "open". Diode A and transistor are "open" when BCD code is > 9.

Fig. 4 - Equivalent output circuits

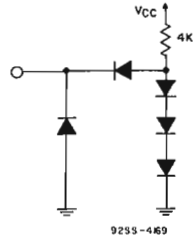


Fig. 5 - Equivalent input circuit for terminals 1, 2, 5, 6 & 7

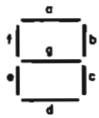
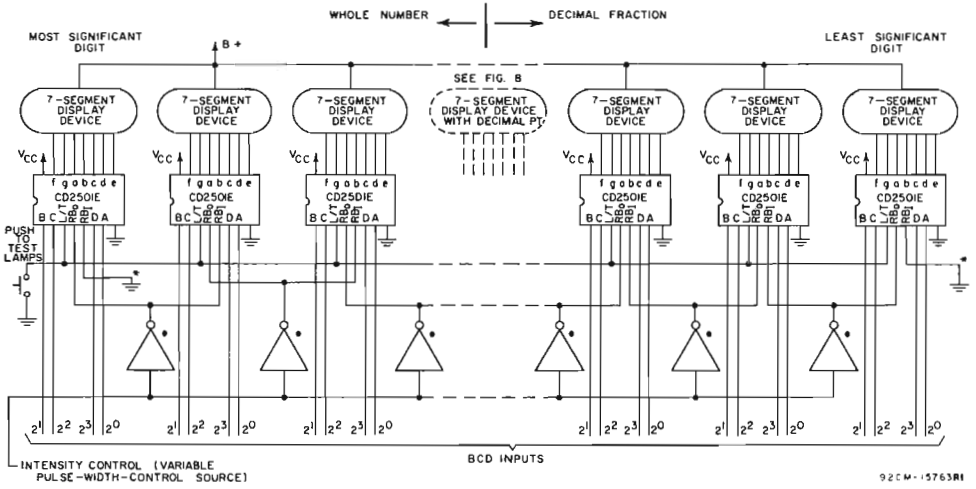


Fig. 6-Digital display device segment designation

TRUTH TABLE

INPUT 0 = Low Level 1 = High Level							OUTPUT 0 = Filament Lit 1 = Filament OUT									TUBE DISPLAY
D	C	B	A	L/T	DP_I	RB_I	a	b	c	d	e	f	g	DP_O	RB_O	
X	X	X	X	0	–	X	0	0	0	0	0	0	0	–	1	8
0	0	0	0	1	–	0	1	1	1	1	1	1	1	–	0	
0	0	0	0	1	–	1	0	0	0	0	0	0	1	–	1	0
0	0	0	1	1	–	X	1	0	0	1	1	1	1	–	1	1
0	0	1	0	1	–	X	0	0	1	0	0	1	0	–	1	2
0	0	1	1	1	–	X	0	0	0	0	1	1	0	–	1	3
0	1	0	0	1	–	X	1	0	0	1	1	0	0	–	1	4
0	1	0	1	1	–	X	0	1	0	0	1	0	0	–	1	5
0	1	1	0	1	–	X	0	1	0	0	0	0	0	–	1	6
0	1	1	1	1	–	X	0	0	0	1	1	1	1	–	1	7
1	0	0	0	1	–	X	0	0	0	0	0	0	0	–	1	8
1	0	0	1	1	–	X	0	0	0	0	1	0	0	–	1	9
1	0	1	0	1	–	X	1	1	1	1	1	1	1	–	1	
1	0	1	1	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	0	0	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	0	1	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	1	0	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	1	1	1	–	X	1	1	1	1	1	1	1	–	1	
–	–	–	–	1	1	–	–	–	–	–	–	–	–	0	–	.
–	–	–	–	1	0	–	–	–	–	–	–	–	–	1	–	
–	–	–	–	0	X	–	–	–	–	–	–	–	–	0	–	.

X = Don't care (0 or 1 entry has no effect)
L/T = Lamp test
RB_I = Ripple Blanking Input
RB_O = Ripple Blanking Output
DP_I = Decimal Point Input
DP_O = Decimal Point Output



• Resistor pull-up output T^2L, DTL, or RTL inverter.

* Suppression of the non-significant zeroes (at both extremes of the display) is accomplished by grounding the RB_1 terminal of the devices associated with the most significant digit of the whole part of the number displayed and the least significant digit of the fractional portion of that number.

Fig. 7 - Typical ripple blanking and intensity control application diagram using RCA CD2501E and display devices DR2000 or equivalents (See Table A)

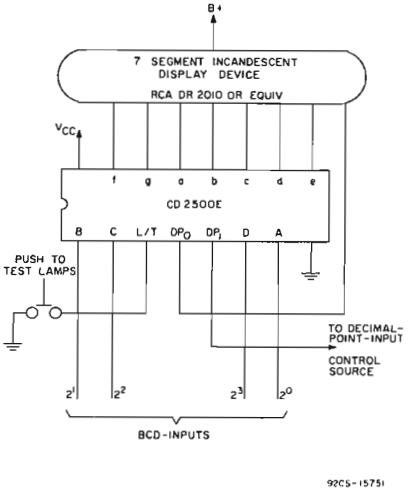


Fig. 8 - Typical decimal point feature application diagram using RCA CD2500E and RCA display device DR2010 (or equivalent)

TABLE A

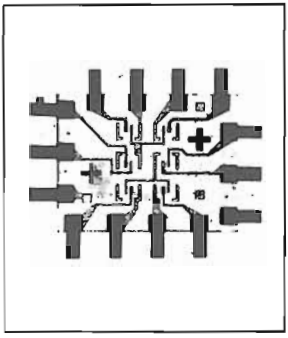
DISPLAY DEVICE TYPE	TYPE OF DISPLAY	CHARACTERISTICS
DR2000		Required Driving Current = 24 ± 2 mA per segment
DR2010	X	0.6" Letter height

RCA
Solid State
Division

Linear Integrated Circuits

Monolithic Silicon

CA741L CA3018L CA3045L CA3083L
CA3015L CA3028AL CA3049L CA3084L
CA3039L CA3054L CA3085L



Beam-Lead Devices for Hybrid Circuit Applications

- Transistor Arrays
- Diode Arrays
- Differential Amplifiers
- Operational Amplifiers
- Voltage Regulators

Features

Assembly

- Simplified repairability
- Use of non-hermetic packages possible
- Silicon nitride passivated
- Platinum silicide ohmic contacts
- Batch handling of chips, batch bonding of beam leads and external lead connections
- Precious metal interconnection metallization
- Precious metal beam leads
- Broad beam leads make interconnect paths less critical; bonds easier to inspect, and defective chips easier to replace
- Batch fabrication techniques provide devices with high reliability at lowest possible cost.

Performance

- Excaptional reliability results from use of sealed-junction beam-lead technology
- Inspectable bonds
- Low-stress, high-strength bonds achieved
- Reliable operation over full military temperature range $-55^{o}C$ to $+125^{o}C$

The beam-lead sealed-junction integrated circuits described in this bulletin are fabricated by a technology which involves the utilization of a passivated layer to seal delicate semiconductor junctions and a multilayered interconnection system of unique design which is stable, highly corrosion-resistant, and readily bondable for attachment to a suitable substrate containing thick or thin film wiring.

Beam Lead identifies a structure in which gold beam leads are extended over the semiconductor chip edges as cantilever beams. Sealed Junction indicates that the integrated circuit chip is completely protected from the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure.

General Considerations

Conventional IC technology has made very substantial contributions to the reliability of solid-state electronics despite the fact that the conventional IC chip is non-hermetic and employs an aluminum-film interconnection system. These considerations have forced the use of hermetic packages or elaborate bulky plastic packages to guard the integrated circuit chip against even modest amounts of humidity. In addition, connection to the aluminum metallization on the chip is customarily accomplished by the use of tiny wires. The reliability of these wired connections to the chip and its external circuit is dependent on human skill and accuracy to a considerable extent.

The culmination of continuing research and development in the quest for IC's having greater reliability, has led to the development of sealed-junction technology for IC fabrication. The beam-lead, sealed-junction device is a truly hermetic IC chip which is impervious to the deteriorating effects of moisture and other potential contaminants. Furthermore, circuit interconnections on and to the chip are accomplished by the use of gold conductors to further enhance reliability. The precious-metal interconnection system on the chip, which is integral with the chip, is, in turn, connected to tiny gold beams (0.003" x 0.006" x 0.0005") which extend over the edge of the chip to serve as leads to external circuit paths and components.

The beam lead integrated circuit chip with its gold leads has ideal mechanical characteristics for use in connection with automated handling methods of attachment to film type wiring on a suitable substrate thus making it possible to achieve a higher order of reliability in the interconnection system than has been achieved heretofore.

A brief resume of the manufacturing process used in producing beam lead IC's is included in the APPENDIX following the OPERATING CONSIDERATIONS.

OPERATING CONSIDERATIONS

When a beam lead device is being bonded to a substrate, certain minimal precautions (listed below), with reference to pattern screening must be taken to prevent stress that can result in breakage, or separation of the conductor paths:

1) Do not mount components within the outside dimension of the bonding tool.
2) Do not use any cross-over or insulation within this dimension.
3) Do not use any resistor terminations within this dimension.
4) Use individual pads for bonding leads wherever feasible.

As in any design, adequate cooling must be considered. Temperature rise in a beam-lead device, when mounted in a particular assembly is a direct result of the dissipation within the device, the distribution of other heat sources within the assembly, and the ability of the assembly to dissipate the total heat generated.

Specific factors which govern the heat flow within such assemblies are:

1. Beam-lead width and thickness
2. Number of beam leads
3. Thermal characteristics of the substrate
4. Thermal characteristics of the ambient surrounding the beam-lead device.

Because of these factors it is, therefore, impractical to specify thermal ratings for beam-lead device assemblies. In consideration of these factors, it is recommended that the chip temperature be checked by direct measurement to avoid exceeding a maximum chip junction temperature of 150°C.

TERMINAL LAYOUT DIAGRAMS

RCA beam lead devices will normally be designed utilizing the outline shown in Fig. 1 viewed with the metallization down.

The resistance values included on the schematic diagrams are typical values and have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs.

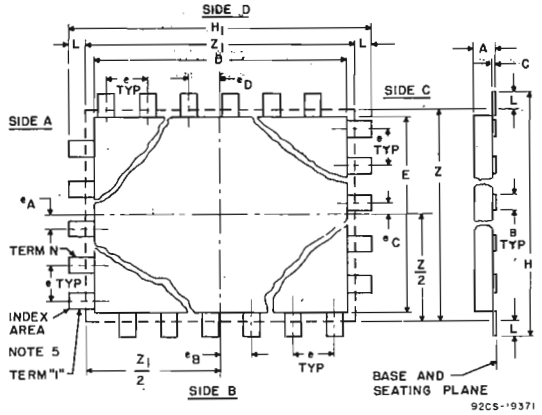
RCA reserves the right to make any changes in the resistance values provided such changes do not adversely affect the published performance characteristics of the device.

APPENDIX

Beam-Lead Manufacturing Processes

An integral passivation layer of silicon nitride protects the beam-lead device from the deteriorating effects of both moisture and contaminants. Low-resistance ohmic contacts to the device junctions are made with platinum silicide which is an extremely stable, non-corrosive intermetallic compound. Gold is used for both the chip interconnections and for the cantilevered beams because it provides high conductivity, is corrosion-resistant, and is readily bondable to a wide variety of substrates and materials. This combination of metallurgically stable components offers the user a chip structure having excellent reliability as compared with the performance of aluminum metallization used in conventional IC designs.

As indicated in the preceding paragraphs, beam-lead technology encompasses a passivating (sealant) layer, a multilayered metal system, and uniquely designed metallization. The metallization consists of a contact of platinum silicide and a layered structure of titanium, platinum, and gold. The metallized pattern which is brought out to the grid, and the subsequent processing are designed to produce a chip in which the attaching leads extend over the edge of the chip. The processing procedure involves the removal of the silicon and the oxide in the grid to leave the beams cantilevered over



SYMBOL	14-LEAD VARIATIONS				16-LEAD VARIATIONS				18-LEAD VARIATIONS				22-LEAD VARIATIONS				NOTES
	INCHES		MILLIMETERS		INCHES		MILLIMETERS		INCHES		MILLIMETERS		INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
A	.002	.010	.051	.254	.002	.010	.051	.254	.002	.010	.051	.254	.002	.010	.051	.254	
B	.0020	.0045	.0510	.1140	.0020	.0045	.0510	.1140	.0020	.0045	.0510	.1140	.0020	.0045	.0510	.1140	5
C	.0004	.0006	.0102	.0152	.0004	.0006	.0102	.0152	.0004	.0006	.0102	.0152	.0004	.0006	.0102	.0152	
D	–	.045	–	1.14	–	.045	–	1.14	–	.055	–	1.39	–	.065	–	1.65	
E	–	.035	–	.889	–	.045	–	1.14	–	.045	–	1.14	–	.055	–	1.39	
e	.010 TP		.2540TP		.010 TP		.254 TP		.010 TP		.254 TP		.010 TP		.254 TP		4
e_A	.0025TP		.0635TP		.0075TP		.191 TP		.0075TP		.1905TP		.0025TP		.0635TP		2,4
e_B	.0075TP		.1905TP		.0075TP		.191 TP		.0025TP		.0635TP		.0075TP		.1905TP		2,4
e_C	.0025TP		.0635TP		.0075TP		.191 TP		.0075TP		.1905TP		.0025TP		.0635TP		2,4
e_D	.0075TP		.1905TP		.0075TP		.191 TP		.0025TP		.0635TP		.0075TP		.1905TP		2,4
H	.042	.049	1.07	1.25	.052	.059	1.321	1.498	.052	.059	1.32	1.49	.062	.069	1.58	1.75	
H_1	.052	.059	1.32	1.49	.052	.059	1.321	1.498	.062	.069	1.58	1.75	.072	.079	1.83	2.00	
L	.0035	.0070	.0889	.1770	.0035	.0070	.0889	.1770	.0035	.0070	.0889	.1770	.0035	.0070	.0889	.1770	
Z	.035Bsc		.889Bsc		.045Bsc		1.143 Bsc		.045Bsc		1 14Bsc		.0558sc		1.398sc		4
Z_1	.045Bsc		1.14Bsc		.045Bsc		1.14 3 Bsc		.0558sc		1 398sc		.065Bsc		1.65Bsc		4
N	14		14		16		16		18		18		22		22		6
N_A	3		3		4		4		4		4		5		5		3
N_B	4		4		4		4		5		5		6		6		3
N_C	3		3		4		4		4		4		5		5		3
N_D	4		4		4		4		5		5		6		6		3

NOTES

1. Refer to Rules for Dimensioning Peripheral Lead Outlines.
2. e_A is basic distance from centerline of Z to centerline of first adjacent counter-clockwise beam position, e_B is basic distance from centerline of first adjacent counter-clockwise beam position, etc. Beam position located by e_A, e_B etc. lies at beam pattern if N_A etc. odd; at first counter-clockwise beam position from pattern if N_A etc. even.
3. N_A is the maximum quantity of lead positions on side "A", N_B on side "B" etc. Picture represents case where N = 22, $N_A = N_C = 5$ and $N_B = N_D = 6$. Applicable number of lead positions, both on each side and total, are as tabulated for each variation.
4. Leads shall be held within .001 total of True Position (TP) at Least Material Condition (LMC) and within .002 total of TP at Maximum Material Condition (MMC). Both location requirements to be checked at Z and Z_1 limits.
5. Number one lead position is counter-clockwise end lead position on a side of minimum width. This index lead shall be distinctively marked if existing; if not existing the first clockwise lead shall be so marked. Any projection shall not extend more than .002" over B maximum nor any notch less than .001 under B minimum.
6. N is the maximum quantity of lead positions.

Fig. 1— Terminal layout for all beam-lead devices. See data bulletins for specific information on individual devices. Millimeter dimensions in chart above and shown in parentheses on the terminal layouts for each beam-lead type are derived from the basic inch dimensions as indicated.

the edge of the chip and available for easy attachment to a package or substrates.

RCA's beam lead technology consists of the following processes:

a) deposition of silicon nitride
b) contact openings
c) deposition and formation of conducting paths (contacts and interconnections)
d) circuit separation
e) bonding

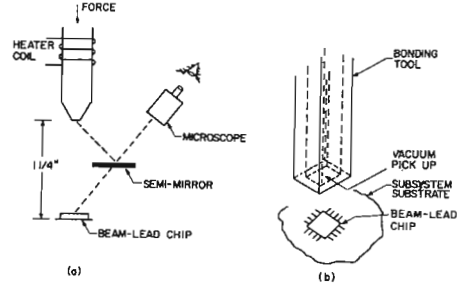
A brief description of these processes follows.

deposition of silicon nitride
Silicon nitride which functions as the passivating (sealant) layer is deposited over the surface of the wafer following the diffusion and oxidation steps required to form the individual components of the device.

contact openings
After the entire wafer has been covered with the protective layer of silicon nitride, appropriate windows are opened both in this and the previously formed oxide layer to permit contact with the junction areas of the individual components.

deposition of contacts and interconnections
To integrate the individual components into the circuits, the exposed terminal areas are interconnected with gold leads formed by electroplating. The gold leads are underlaid with titanium, and platinum in that order, over a platinum silicide layer in the contact openings to attain a low-resistance ohmic contact to the silicon. Two electroplating steps are used to form both the gold metallization network and the gold beam leads by means of which appropriate circuit terminals can be connected to external electrical contacts.

circuit separation
A thinning and etching technique is next used to separate the completed circuit chip from the wafer in which they are formed. This separation involves removal of the silicon from the grids between the chips by a very precise chemical etching process which physically separates the circuits from each other but leaves them firmly held in a matrix position. In this position, the individual circuits can be evaluated by an automatic test set operating in conjunction with an automatic probe set.



beam-lead, bonding (See Fig. 2)
The actual bonding of the beam leads to a metallized package or a substrate is performed by a thermocompression technique as follows:

A bonding tool is used to pick up the chip and bond it to the subsystem substrate metallization. The chip and the bonding tool are aligned through the use of a semi-mirror shown in Fig. 2(a). The bonding tool is lowered to the chip. The chip is held firmly by the vacuum [inside the bonding tool, see Fig. 2(b)] and transferred to the bonding station. Another alignment is made [see Fig. 2(a)] by viewing the chip in the tool (through the semi-mirror) and the subsystem substrate metallization. The bonding tool and the chip are then lowered to the subsystem substrate where the heated substrate and the heated bonding tool develop an interface temperature of 300°C between the beam leads and the substrate. Simultaneously, a force is applied to the bonding tool which deforms the ends of the beam leads and completes the thermocompression bond. The bonding time is 2 to 3 seconds.

Any faulty chips can be rebonded. The most significant advantages of the beam lead technology are in this bonding process--

1. Manufacturing the silicon chip beam leads as an integral part of the device eliminates the necessity of bonding to the chip and immediately reduces the number of bonds to be made for an equivalent interconnection.
2. Furthermore, since each lead is an integral part of the contact and not a mechanically-made connection, the reliability of the circuit is greatly enhanced.
3. In addition, the single metal system gold-to-gold employed between contacts and leads not only obviates a reliability factor often associated with bonds with contacts made between dissimilar metals, but also insures a bond completely free from corrosion.
4. And finally, all bonds for a single chip can be made simultaneously providing both technical and economic advantages.

REFERENCES

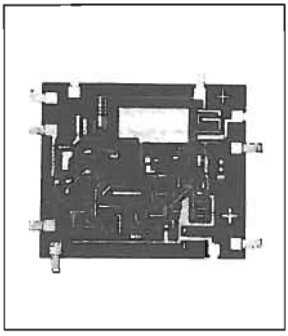
1. The Western Electric Engineer, Dec. 1967.

Fig. 2-- a) Allgnment to pick up chip and to bond chip to subsystem substrate: force is used only to bond chip;
b) detail of bonding tool to show vacuum pick up.

Linear Integrated Circuits

Monolithic Silicon

CA741L



Beam-Lead Operational Amplifier

High-Gain Operational Amplifier With Internal Phase Compensation

FOR MILITARY, INDUSTRIAL AND CONSUMER APPLICATIONS

Applications

- Comparator
- Integrator or differentiator
- Summing amplifier
- DC amplifier
- Multivibrator
- Narrow-band or band-pass filter

RCA CA741L is the beam-lead version of the family of CA741, general-purpose high-gain, monolithic operational amplifiers. The CA741L features internal phase compensation, provides output short-circuit protection, and latch-free operation. This type also features large common mode and differential mode signal ranges and has a low offset voltage and nulling capability. The CA741L consists of a differential-input amplifier with an effectively double-ended output that drives a gain and level-shifting stage having a complementary emitter-follower output.

Features

- No external phase compensation required.
- Open-loop voltage gain: 50,000 min.
- Input bias current: 500 nA max.
- Input offset current: 200 nA max.
- Input offset voltage: 5 mV max.
- Operation over the full military temperature range: -55 to +125°C

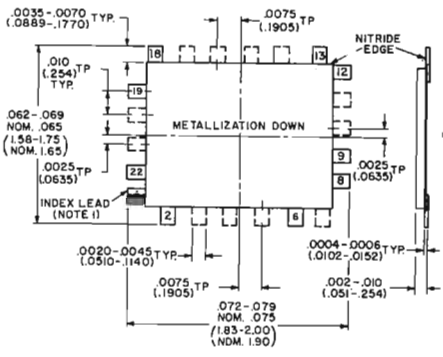


Fig. 1-1— Terminal layout for CA741L (22-lead configuration)

CAUTION: Although RCA-CA741L is electrically similar to CA741T, it is not a pin-for-pin replacement.

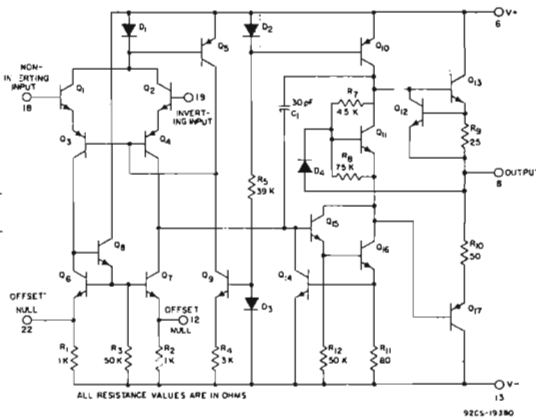


Fig. 1-2— Schematic diagram of CA741L

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DC Supply Voltage (between V^+ and V^- terminals) . . . . . 44 V
Differential Input Voltage . . . . . ±30 V
DC Input Voltage* . . . . . ±15 V
Output Short-Circuit Duration . . . . . Indefinite
Voltage between Offset Null and V^- . . . . . ±0.5 V
Temperature Range:
Operating . . . . . −55 to +125°C
Storage . . . . . −65 to +150°C

*If Supply Voltage is less then ±15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

ELECTRICAL CHARACTERISTICS
For Equipment Design

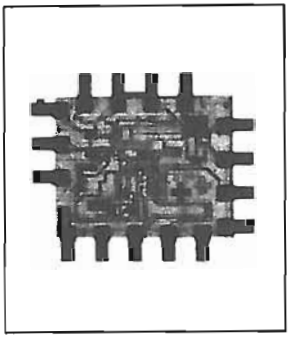
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS			UNITS
		SUPPLY VOLTS: $V^+ = 15$, $V^- = -15$	AMBIENT TEMPERATURE (T_A)	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{IO}	$R_S \leq 10$ kΩ	25°C	–	1	5	mV
			-55 to +125°C	–	1	6	
Input Offset Current	I_{IO}		25°C	–	20	200	nA
			-55°C	–	85	500	
			+125°C	–	7	200	
Input Bias Current	I_I		25°C	–	80	500	nA
			-55°C	–	300	15000	
			+125°C	–	30	500	
Input Resistance	R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C	50,000	200,000	–	
			-55 to +125°C	25,000	–	–	
Common-Mode Input Voltage Range	V_{ICR}		25°C	–	–	–	V
			-55 to +125°C	±12	±13	–	
Common-Mode Rejection Ratio	C_{MRR}	$R_S \leq$ 10 kΩ	25°C	–	–	–	dB
			-55 to +125°C	70	90	–	
Supply Voltage Rejection Ratio	V_{RR}	$R_S \leq$ 10 kΩ	25°C	–	–	–	μV/V
			-55 to +125°C	–	30	150	
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq$ 10 kΩ	25°C	–	–	–	V
			-55 to +125°C	±12	±14	–	
		$R_L \geq$ 2 kΩ	25°C	–	–	–	
			-55 to +125°C	±10	±13	–	
Supply Current			25°C	–	1.7	2.8	mA
			-55°C	–	2	3.3	
			+125°C	–	1.5	2.5	
Device Dissipation	P_D		25°C	–	50	85	mW
			-55°C	–	60	100	
			+125°C	–	45	75	

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA, Commercial Engineering, Harrison, N. J. 07029.

Linear Integrated Circuits

Monolithic Silicon

CA3015L



Beam-Lead Operational Amplifier

Applications

- Narrow-Band and Bandpass Amplifier
- Operational Functions
- Feedback Amplifier
- DC and Video Amplifier
- Multivibrator
- Oscillator
- Comparator
- Servo Driver
- Scaling Adder
- Balanced Modulator-Driver

The RCA CA3015L is the beam-lead version of the CA3015 operational amplifier family. The beam leads of this device are formed as an integral part of the IC chip during the batch fabrication process.

The CA3015L is particularly suited for applications in hybrid circuits where hermetic packaging, low cost, and reliable operation are prime considerations.

For applications of the CA3015 family of operational amplifiers see the companion Application Notes, ICAN-5290 "Integrated Circuit Operational Amplifiers", ICAN-5213 "Application of the RCA-CA3015, CA3016 Integrated Circuit Operational Amplifiers," and ICAN-5015 "Application of the RCA-CA3008, CA3010 Integrated Circuit Operational Amplifiers".

Features

■ Open-Loop Voltage Gain		70	dB	typ.
■ Common-Mode Rejection Ratio		103	dB	typ.
■ Output Impedance		92	Ω	typ.
■ Input Offset Voltage		1	mV	typ.
■ Static Device Dissipation at	±12V	175	mW	typ.
	± 6V	30	mW	typ.
	± 3V	7	mW	typ.

■ Operation over the full military temperature range: −55 to +125°C

CAUTION: ALTHOUGH RCA-CA3015L is electrically similar to CA3015, it is not a pin-for-pin replacement.

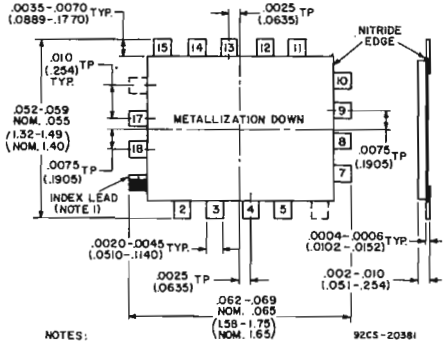


Fig. 2-1— Terminal layout for CA3015L (18 lead configuration).

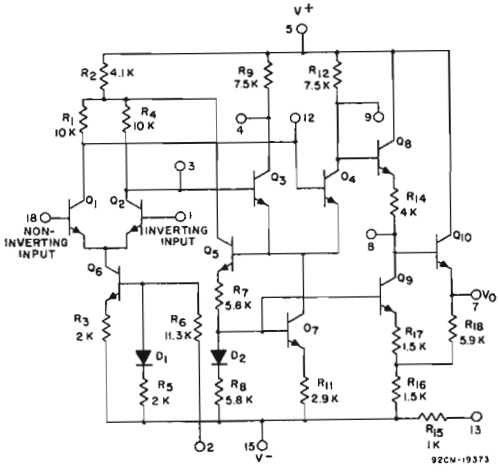


Fig. 2-2— Schematic diagram of CA3015L

MAXIMUM RATINGS,
ABSOLUTE-MAXIMUM VALUES.

OPERATING TEMPERATURE RANGE .....-55°C to +125°C
STORAGE TEMPERATURE RANGE .....-65° to +150°C
SIGNAL VOLTAGE ..... −8 V to +1 V

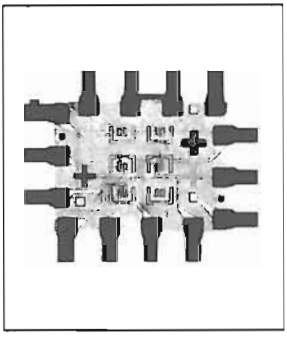
ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOL	LIMITS			UNITS
		MIN.	TYP.	MAX.	
STATIC CHARACTERISTICS: V^+ = +12 V, V^- = -12 V					
Input Offset Voltage	V_{IO}	–	1.37	5	mV
Input Offset Current	I_{IO}	–	1.07	5	μA
Input Bias Current	I_I	–	9.6	24	μA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$	–	0.096	0.5	mV/V
Negative	$\Delta V_{IO}/\Delta V^-$	–	0.156	0.5	
Device Dissipation	P_D	–	175	–	mW
DYNAMIC CHARACTERISTICS:					
Open-Loop Differential Voltage Gain	A_{OL}	66	70	–	dB
Common-Mode Rejection Ratio	CMRR	80	103	–	dB
Maximum Output-Voltage Swing	V_O(P-P)	12	14	–	V_{P-P}
Input Impedance	Z_{IN}	5	7.8	–	kΩ
Output Impedance	Z_{OUT}	–	92	–	Ω
Common-Mode Input-Voltage Range	V_{ICR}	– –	+0.65 -8	– –	V

Linear Integrated Circuits

Monolithic Silicon

CA3018L



Beam-Lead General-Purpose Transistor Array

Two Isolated Transistors and a Darlington-Connected Transistor Pair

FOR LOW-POWER APPLICATIONS AT FREQUENCIES FROM DC THROUGH THE VHF RANGE

The CA3018L is a beam-lead version of the RCA CA3018 and consists of four general purpose silicon n-p-n transistors on a common monolithic substrate. The beam leads of this device are formed as an integral part of the IC chip during the batch fabrication process.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The CA3018L is particularly suited for applications in hybrid circuits where hermetic packaging, low costs, and reliable operation are prime considerations. For applications of the general purpose transistors see RCA Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated-Circuit Transistor Array".

Applications

- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Features

- Matched monolithic general purpose transistors
- h_{FE} matched ±10%
- V_{BE} matched ±5 mV
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure — 3.4 dB typical at 1 kHz
- Operation over the full military temperature range: -55 to +125°C

CAUTION: Although RCA-CA3018L is electrically similar to CA3018, it is not a pin-for-pin replacement.

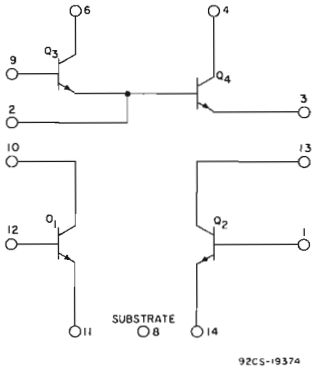
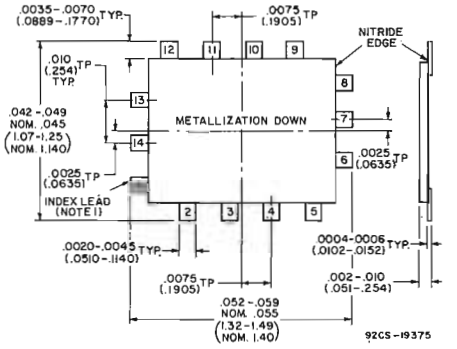


Fig. 3-1— Schematic diagram of CA3018L



NOTES:
1. INDEX CONFIGURATION ON BEAM NO.1 OPTIONAL, PROVIDED LEAD MAX. IS NOT INCREASED MORE THAN .002
2. LEADS AT TRUE POSITION (TP) WITHIN .002 TOTAL (REF. USANS Y14.5-1966)
3. SILICON MUST NOT EXTEND BEYOND NITRIDE OVER A BEAM.

Fig. 3-2— Terminal layout for CA3018L (14-lead configuration)

MAXIMUM RATINGS, *Absolute-Maximum Values, at $T_A = 25^oC$*

The following ratings apply for each transistor in the device:

Temperature Range:
- Operating ..... -55 to +125°C
- Storage ..... -65 to +150°C

Collector-to-Emitter Voltage, V_{CEO} ..... 15 V
Collector-to-Base Voltage, V_{CBO} ..... 20 V
Collector-to-Substrate Voltage, V_{CIO}* ..... 20 V
Emitter-to-Base Voltage, V_{EBO} ..... 5 V
Collector Current, I_C ..... 50 mA

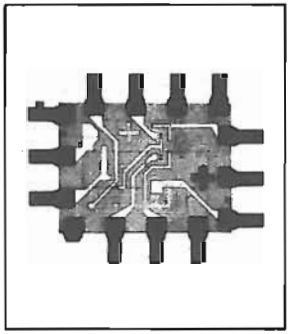
*The collector of each transistor of CA3018L is isolated from the substrate by an integral diode. *The substrate (terminal 8) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$ FOR EACH TRANSISTOR	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC CHARACTERISTICS						
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10V, I_E = 0$	–	0.002	100	nA
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V, I_B = 0$	–	–	5	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	15	24	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A, I_E = 0$	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A, I_C = 0$	5	7	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A, I_{CI} = 0$	20	60	–	V
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1$ mA, $I_C = 10$ mA	–	0.23	–	V
Static Forward Current Transfer Ratio	h_{FE}	$V_{CE} = 3V$, $I_C = 10$mA $I_C = 1$mA $I_C = 10\mu A$	– 30 –	100 100 54	– – –	– – –
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		$V_{CE} = 3V, I_{C1} = I_{C2} = 1$ mA	0.9	0.97	–	–
Static Forward Current Transfer Ratio Darlington Pair (Q_3 and Q_4)	h_{FED}	$V_{CE} = 3V, I_C = 1$ mA	1500	5400	–	–
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$ $I_E = 1$ mA $I_E = 10$mA	– –	0.715 0.800	– –	V
Input Offset Voltage	$\lvert V_{BE_1} - V_{BE_2} \rvert$	$V_{CE} = 3V, I_E = 1$ mA	–	0.48	5	mV
Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2	$\frac{\lvert \Delta V_{BE} \rvert}{\Delta T}$	$V_{CE} = 3V, I_E = 1$ mA	–	-1.9	–	mV/°C
Base (Q_3)-to-Emitter (Q_4) Voltage Darlington Pair	$V_{BED}(V_{9-1})$	$V_{CE} = 3$ V $I_E = 10$ mA $I_E = 1$ mA	– –	1.46 1.32	– –	V
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair - Q_3, Q_4	$\frac{\lvert \Delta V_{BED} \rvert}{\Delta T}$	$V_{CE} = 3V, I_E = 1$ mA	–	4.4	–	mV/°C
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert V_{BE_1} - V_{BE_2} \rvert}{\Delta T}$	$V_{CC} = +6V, V_{EE} = -6V$, $I_{C_1} = I_{C_2} = 1$ mA	–	1	–	μV/°C

Linear Integrated Circuits

Monolithic Silicon

CA3028AL



Beam-Lead Differential/Cascode Amplifier

FOR COMMUNICATIONS AND INDUSTRIAL EQUIPMENT AT FREQUENCIES FROM DC to 120 MHz

Applications

- RF and IF Amplifiers (Differential or Cascode)
- DC, Audio, and Sense Amplifiers
- Converter in the Commercial FM Band
- Oscillator • Mixer • Limiter

Features

- Controlled for input bias current
- Balanced differential amplifier configuration with controlled constant-current source to provide unexcelled versatility
- Single- and dual-ended operation
- Operation from dc to 120 MHz
- Balanced-AGC capability
- Wide operating-current range
- Operation over the full military temperature range: -55 to +125°C

RCA CA3028AL is the beam-lead version of the CA3028A family of differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from dc to 120 MHz. The beam leads of this device are formed as an integral part of the IC chip during the batch fabrication process.

The CA3028AL is particularly suited for applications in hybrid circuits where hermetic packaging, low cost, and reliable operation are prime considerations.

For applications of the CA3028AL see the companion Application Note ICAN-5337 "Application of the RCA CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges".

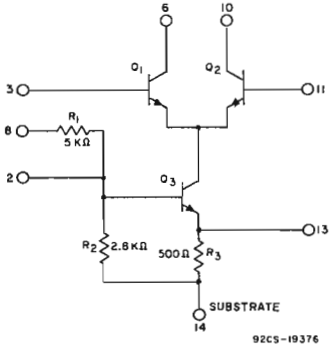
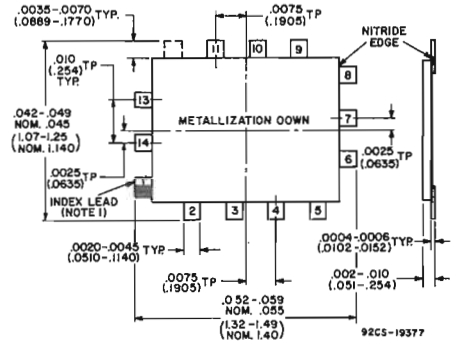


Fig. 4-1— Schematic diagram of CA3028AL



NOTES:
1. INDEX CONFIGURATION ON BEAM NO.1 OPTIONAL, PROVIDED LEAD MAX. IS NOT INCREASED MORE THAN .002
2. LEADS AT TRUE POSITION (TP) WITHIN .002 TOTAL (REF. USAS Y14.5-1966)
3. SILICON MUST NOT EXTEND BEYOND NITRIDE OVER A BEAM.

Fig. 4-2— Terminal layout for CA3028AL (14-lead configuration)

CAUTION: Although RCA-CA3028AL is electrically similar to CA3028A, it is not a pin-for-pin replacement.

MAXIMUM RATINGS, *Absolute-Maximum Ratings at* $T_A = 25^oC$

TEMPERATURE RANGE:

Operating. . . . . -65°C to +125°C
Storage . . . . . -65°C to +150°C

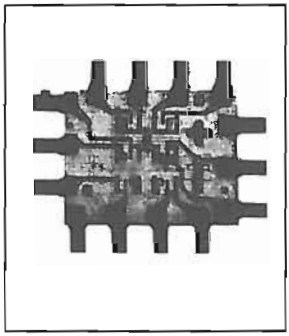
ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS		LIMITS			UNITS
				MIN.	TYP.	MAX.	
STATIC CHARACTERISTICS							
		V^+	V^-				
Input Bias Current	I_I	6V 12V	6V 12V	– –	16.6 36	70 106	μA
Quiescent Operating Current	I_6 or I_{10}	6V 12V	6V 12V	0.8 2	1.25 3.3	2 5	mA
Input Current (Term. No. 8)	I_8	6V 12V	6V 12V	0.5 1	0.85 1.65	1 2.1	mA
Device Dissipation	P_T	6V 12V	6V 12V	24 120	36 175	54 260	mW

Linear Integrated Circuits

Monolithic Silicon

CA3039L



Beam-Lead Diode Array

6 Matched Ultra-Fast Low-Capacitance Diodes

FOR APPLICATIONS IN COMMUNICATIONS AND SWITCHING SYSTEMS

Applications

- Balanced modulators or demodulators
- Ring modulators
- High-speed diode gates
- Analog switches

RCA CA3039L is the beam-lead version of the CA3039 which consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. The beam leads of the device are formed as an integral part of the IC chip during the batch fabrication process.

CA3039L is particularly suited for applications in hybrid circuits where hermetic packaging, low cost and reliable operation are prime considerations.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a dc potential which is significantly more negative (with respect to the active diodes) than the peek signal applied.

Features

- Excellent reverse recovery time: 1 ns typ.
- Matched monolithic construction: V_F matched ±5 mV
- Low diode capacitance: C_D = 0.65 pF typ. at V_R = −2 V
- Operation over the full military temperature range: −55 to +125°C

CAUTION: Although RCA-CA3039L is electrically similar to CA3039, it is not a pin-for-pin replacement.

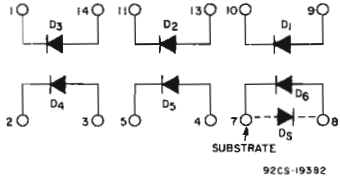
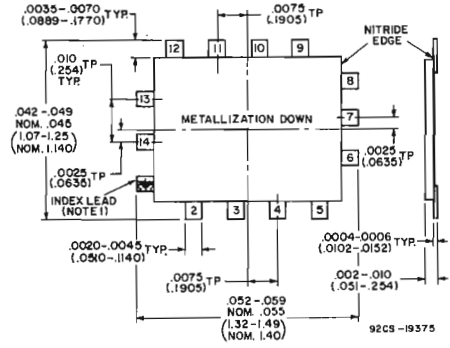


Fig. 5-1— Schematic diagram of CA3039L



NOTES:
1. INDEX CONFIGURATION ON BEAM NO.1 OPTIONAL, PROVIDED LEAD MAX. IS NOT INCREASED MORE THAN .002
2. LEADS AT TRUE POSITION (TP) WITHIN .002 TOTAL (REF. USAMS Y14.5-1966)
3. SILICON MUST NOT EXTEND BEYOND NITRIDE OVER A BEAM.

Fig. 5-2— Terminal layout for CA3039L (14-lead configuration)

MAXIMUM RATINGS, *Absolute-Maximum Ratings at* $T_A = 25^oC$

Peak Inverse Voltage V_{RM} for: D_1-D_5 ..... 5V
D_6 ..... 0.5V

TEMPERATURE RANGE:
Operating ..... -55 to +125°C
Storage ..... -65 to +150°C

Peak Diode-to-Substrate Voltage, V_{DI}
for D_1-D_5 (term. 3, 4, 9, 13 or 14 to term. 7) +20, -1 V
DC Forward Current, I_F ..... 25 mA
Peak Recurrent Forward Current I_{FRM} ..... 100 mA
Peak Forward Surge Current I_{FSM} ..... 100 mA

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$

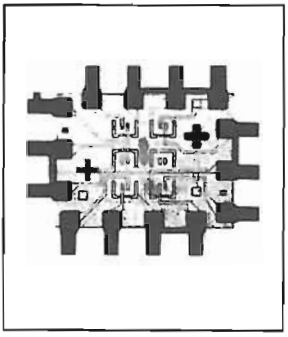
Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
DC Forward Voltage Drop	V_F	I_F = 50 μA	–	0.65	0.69	V
		1 mA	–	0.73	0.78	
		3 mA	–	0.76	0.80	
		10 mA	–	0.81	0.90	
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = -10 μA	5	7	–	V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = -10 μA	20	–	–	V
DC Reverse (Leakage) Current	I_R	V_R = -4V	–	0.016	100	nA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = -10V	–	0.022	100	nA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	–	0.5	5	mV
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA	–	1	–	μV/°C
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	–	-1.9	–	mV/°C
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA	–	0.65	–	V
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	–	1	–	ns
Diode Capacitance	C_D	V_R = -2 V, I_F = 0	–	0.65	–	pF
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF

Linear Integrated Circuits

Monolithic Silicon

CA3045L



Beam-Lead General-Purpose N-P-N Transistor Array

Three Isolated Transistors and One Differentially Connected Transistor Pair.

FOR LOW-POWER APPLICATIONS AT FREQUENCIES FROM DC THROUGH THE VHF RANGE

Applications

- General use in various types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Features

- Two matched transistor pairs: V_{BE} matched ±5 mV, Input offset current 2 μA max. at I_C = 1 mA
- 5 general-purpose monolithic transistors
- Operation from DC to more than 120 MHz
- Wide operating current range
- h_{FE} (each transistor)=100 typ. at V_{CE}=3 V, I_C=1 mA
- Low-noise figure: 3.2 dB typ. at 1 kHz
- Operation over the full military temperature range: -55 to +125°C

RCA CA3045L is a beam-lead version of the CA3045 and contains an array of general-purpose transistors for use in signal-level applications at frequencies up to more than 120 MHz. The beam leads of this device are formed as an integral part of the IC chip during the batch fabrication process.

The CA3045L is particularly suited for use in hybrid type construction where compactness, hermeticity, ultra-reliability, and low cost are prime requirements. For suggested applications of transistor arrays, see RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array".

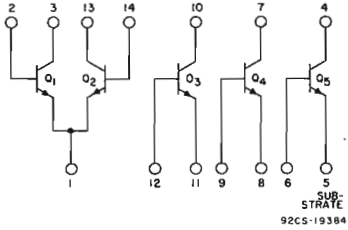
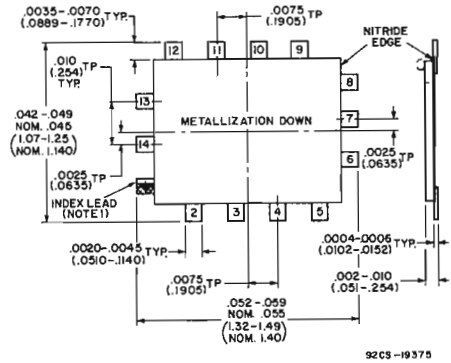


Fig. 6-1— Schematic diagram of CA3045L



NOTES:

1. INDEX CONFIGURATION ON BEAM NO.1 OPTIONAL, PROVIDED LEAD MAX. IS NOT INCREASED MORE THAN .002
2. LEADS AT TRUE POSITION (TP) WITHIN .002 TOTAL (REF. USASNI Y14.5-1966)
3. SILICON MUST NOT EXTEND BEYOND NITRIDE OVER A BEAM.

Fig. 6-2— Terminal layout for CA3045L (14-lead configuration)

CAUTION: Although RCA-CA3045L is electrically similar to CA3045, it is not a pin-for-pin replacement.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

Collector-to-Emitter Voltage, V_{CEO} . . . . . 15 V
Collector-to-Base Voltage, V_{CBO} . . . . . 20 V
Collector-to-Substrate Voltage, V_{CIO}* . . . . . 20 V
Emitter-to-Base Voltage, V_{EBO} . . . . . 5 V
Collector Current, I_C . . . . . 50 mA

Temperature Range:
Operating . . . . . -55 to +125°C
Storage . . . . . -65 to +150°C

*The collector of each transistor is isolated from the substrate by an integral diode. *The substrate (terminal 5) must be more negative than all collectors to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$

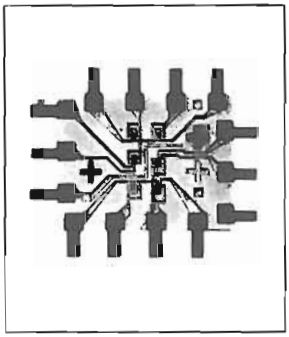
Characteristics apply for each transistors

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
STATIC CHARACTERISTICS						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\,\mu A$, $I_E = 0$	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\,\mu A$, $I_{CI} = 0$	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\,\mu A$, $I_C = 0$	5	7	–	V
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	–	0.002	40	nA
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	–		0.5	μA
Static Forward Current Transfer Ratio (Static Beta)	h_{FE}	$V_{CE} = 3$V, $I_C = 10$ mA	–	100	–	–
		$V_{CE} = 3$V, $I_C = 1$ mA	40	100	–	–
		$V_{CE} = 3$V, $I_C = 10\,\mu A$	–	54	–	–
Input Offset Current for Matched Pair Q_1 and Q_2	$\lvert I_{IO_1} - I_{IO_2} \rvert$	$V_{CE} = 3$V, $I_C = 1$ mA	–	0.3	2	μA
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3$V, $I_E = 1$ mA	–	0.715	–	V
		$V_{CE} = 3$V, $I_E = 10$ mA	–	0.800	–	V
Magnitude of Input Offset Voltage for Differential Pair	$\lvert V_{IO_1} - V_{IO_2} \rvert$	$V_{CE} = 3$V, $I_C = 1$ mA	–	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors	$\lvert V_{IO_3} - V_{IO_4} \rvert$, $\lvert V_{IO_4} - V_{IO_5} \rvert$, $\lvert V_{IO_5} - V_{IO_3} \rvert$	$V_{CE} = 3$V, $I_C = 1$ mA	–	0.45	5	mV
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	$V_{CE} = 3$V, $I_C = 1$ mA	–	1.1	–	$\mu V/^oC$
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 3$V, $I_C = 1$ mA	–	−1.9	–	$mV/^oC$
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1$ mA, $I_C = 10$ mA	–	0.23	–	V

Linear Integrated Circuits

Monolithic Silicon

CA3049L



Beam-Lead Dual Independent Differential Amplifiers

For Low-Power Applications at Frequencies up to 500 MHz

Applications

- VHF amplifiers
- VHF mixers
- Multifunction combinations — RF/Mixer/Oscillator; Converter/IF
- IF amplifiers (differential and/or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascade limiters
- Synchronous detectors
- Balanced mixers
- Synthesizers
- Balanced (push-pull) cascode amplifiers
- Sense amplifiers

CA3049L is the beam-lead version of the CA3049 and consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general-purpose high-frequency devices which exhibit a value of f_T in excess of 1000 MHz. These features make the CA3049L useful to 500 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The CA3049L is particularly suited for applications in hybrid circuits where hermetic packaging, low cost, and reliable operation are prime considerations.

The monolithic construction of the CA3049L provides close electrical and thermal matching of the amplifiers. This feature makes this device particularly useful in dual-channel applications where matched performance of the two channels is required.

Features

- Power Gain 23 dB (typ.) at 200 MHz
- Noise Figure 4.6 dB (typ.) at 200 MHz
- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Full military temperature range capability — −55°C to +125°C

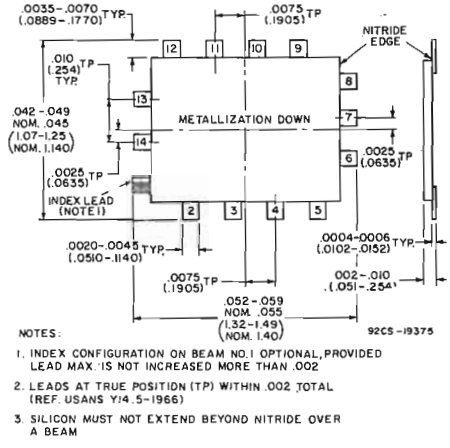


Fig. 7-2—Terminal layout for CA3049L (14-lead configuration)

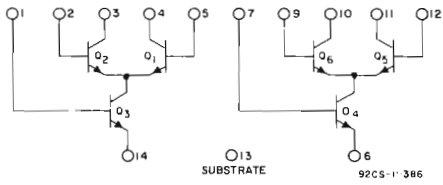


Fig. 7-1— Schematic diagram of CA3049L

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device.

Although RCA-CA3049L is electrically similar to CA3049, it is not a pin-for-pin replacement.

MAXIMUM RATINGS, *Absolute-Maximum Values, at $T_A = 25°C$*

Temperature Range:

Operating	-55 to +125	°C
Storage	-65 to +150	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049L is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

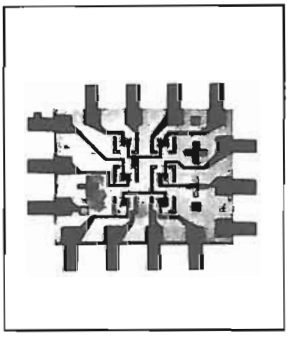
ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CA3049L LIMITS			
			MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS (for each transistor)						
Input Bias Current	I_{IB}	$V_{CE} = 3$ V, $I_C = 1$ mA	–	10	33	μA
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	–	–	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	15	–	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10$ μA, $I_E = 0$	20	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10$ μA, $I_{CI} = 0$	20	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10$ μA, $I_C = 0$	5	–	–	V

Linear Integrated Circuits

Monolithic Silicon

CA3054L



Beam-Lead Dual Independent Differential Amplifiers

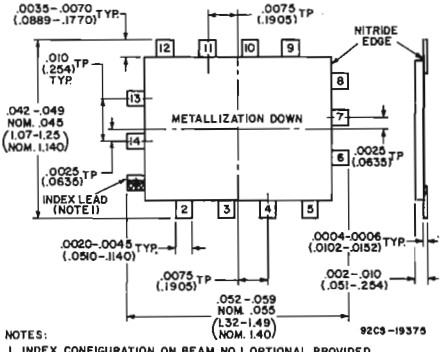
FOR LOW-POWER APPLICATIONS AT FREQUENCIES FROM DC TO 120 MHz

Applications

- Dual sense amplifiers
- Dual Schmitt triggers
- Multifunction combinations — RF/Mixer/Oscillators; Converter/IF
- IF amplifiers (differential and/or cascode)
- Product detectors
- Doubly-balanced modulators and demodulators
- Balanced quadrature detectors
- Cascade limiters
- Synchronous detectors
- Pairs of balanced mixers
- Synthesizer mixers
- Balanced (push-pull) cascode amplifiers

The RCA CA3054L is the beam-lead version of the CA3054, and consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The beam leads of this device are formed as an integral part of the IC chip during the batch fabrication process.

The CA3054L is particularly suited for applications in hybrid circuits where hermetic packaging, low cost, and reliable operation are prime considerations.



NOTES:
1. INDEX CONFIGURATION ON BEAM NO.1 OPTIONAL, PROVIDED LEAD MAX. IS NOT INCREASED MORE THAN .002
2. LEADS AT TRUE POSITION (TP) WITHIN .002 TOTAL (REF. USAS Y14.5-1966)
3. SILICON MUST NOT EXTEND BEYOND NITRIDE OVER A BEAM.

Fig. 8-1— Terminal layout for CA3054L (14-lead configuration)

CAUTION: Although RCA-CA3054L is electrically similar to CA3054, it is not a pin-for-pin replacement.

Features

- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Maximum input offset voltage — ±5 mV
- Operation over the full military temperature range: -55 to +125°C

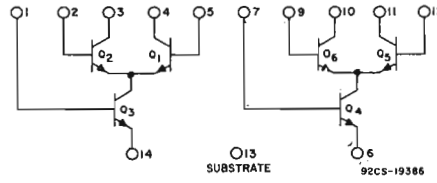


Fig. 8-2— Schematic diagram of CA3054L

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device.

MAXIMUM RATINGS, *Absolute-Maximum Values, at* $T_A = 25^oC$

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO} . . . . . 15 V
Collector-to-Base Voltage, V_{CBO} . . . . . 20 V
Collector-to-Substrate Voltage, V_{CIO}* . . . . . 20 V
Emitter-to-Base Voltage, V_{EBO} . . . . . 5 V
Collector Current, I_C . . . . . 50 mA
Temperature Range:
Operating . . . . . -55 to +125°C
Storage . . . . . -65 to +150°C

*The collector of each transistor of the CA3054L is isolated from the substrate by an integral diode. *The substrate must be connected to e voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.*

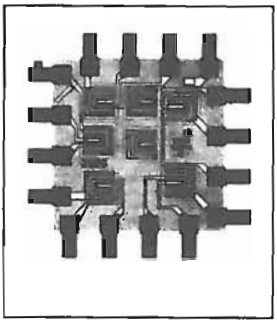
ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC CHARACTERISTICS						
For Each Differential Amplifier:						
Input Offset Voltage	V_{IO}	V_{CB} = 3 V $I_{E(Q3)} = I_{E(Q4)}$ = 2 mA	–	0.45	5	mV
Input Offset Current	I_{IO}		–	0.3	2	μA
Input Bias Current	I_I		–	10	24	μA
Quiescent Operating Current Ratio	$\frac{I_{C(Q_1)}}{I_{C(Q_2)}}$ or $\frac{I_{C(Q_5)}}{I_{C(Q_6)}}$		–	0.98 to 1.02	–	–
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\Delta\lvert V_{IO}\rvert}{\Delta T}$		–	1.1	–	μV/°C
For Each Transistor:						
DC Base-to-Emitter Voltage	V_{BE}	V_{CB} = 3 V, I_C = 50 μA	–	0.630	0.700	V
		V_{CB} = 3 V, I_C = 1 mA	–	0.715	0.800	V
		V_{CB} = 3 V, I_C = 3 mA	–	0.750	0.850	
		V_{CB} = 3 V, I_C = 10 mA	–	0.800	0.900	
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3V, I_C = 1 mA	–	-1.9	–	mV/°C
Collector-Cutoff Current	I_{CBO}	V_{CB} = 3V, I_E = 0	–	0.002	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10μA, I_E = 0	20	60	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10μA, I_{CI} = 0	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0	5	7	–	V

Linear Integrated Circuits

Monolithic Silicon

CA3083L



General-Purpose High-Current N-P-N Transistor Array

Applications

- Signal processing and switching systems operating from DC to VHF
- Lamp and relay driver
- Differential amplifier
- Temperature-compensated amplifier
- Thyristor firing
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for suggested applications

RCA-CA3083L is the beam-lead version of the CA3083. It consists of a versatile array of five high-current (to 100 mA) n-p-n transistors on a common monolithic substrate. Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design.

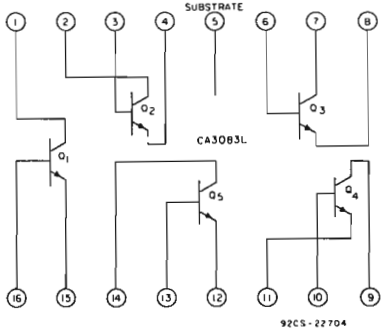


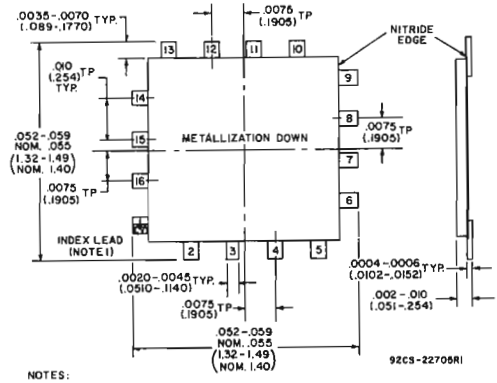
Fig. 9-1– Schematic diagram of CA3083L.

CAUTION: Although RCA-CA3083L is electrically similar to CA3083, it is not a pin-for-pin replacement.

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device.

Features

- High I_C: 100 mA max.
- Low V_{CEsat} (at 50 mA): 0.4 V typ.
- Transistor pair (Q1 and Q2):
  V_{IO} (ΔV_{BE}): 1.2 mV typ.
  I_{IO} 0.7 μA typ.
- 5 independent transistors plus separate substrate connection
- Operation over the full military temperature range:
  −55 to +125°C



NOTES:

1. INDEX CONFIGURATION ON BEAM NO.1 OPTIONAL, PROVIDED LEAD MAX. IS NOT INCREASED MORE THAN .002
2. LEADS AT TRUE POSITION (TP) WITHIN .002 TOTAL (REF. USANS Y14.5-1966)
3. SILICON MUST NOT EXTEND BEYOND NITRIDE OVER A BEAM.

Fig. 9-2– Terminal layout for CA3083L (16-lead configuration).

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Ambient Temperature Range:

Operating	−55 to +125	°C
Storage	−65 to + 150	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3083L is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

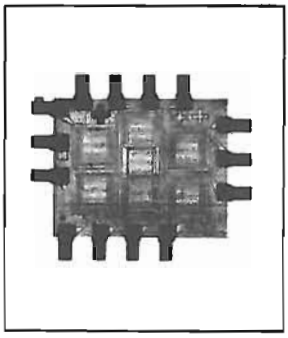
ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	40	76	–	
		V_{CE} = 3V, I_C = 50mA	40	75	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	0.65	0.74	0.85	V

Linear Integrated Circuits

Monolithic Silicon

CA3084L



Beam-Lead General-Purpose P-N-P Transistor Array

Applications

- General use in signal processing systems having low-power and low-frequency requirements
- Differential amplifiers
- Temperature compensated amplifiers
- Active loads for differential amplifiers using n-p-n transistors
- Complementary uses with RCA n-p-n transistor arrays

RCA CA3084L is the beam lead version of the CA3084, a general-purpose silicon p-n-p transistor array incorporating two independent transistors, a Darlington circuit, and a current-mirror pair with a shared diode. The beam leads of this device are formed as an integral part of the IC chip during the batch fabrication process.

The CA3084L is particularly suited for applications in hybrid circuits where hermetic packaging, low cost, and reliable operation are prime considerations.

The two independent transistors in the array may be used in a variety of circuit applications. The Darlington pair may be used as the equivalent of a single high-beta transistor. The current-mirror pair is well suited for constant-current applications and can also be used as the active loads in a differential amplifier which uses n-p-n transistors.

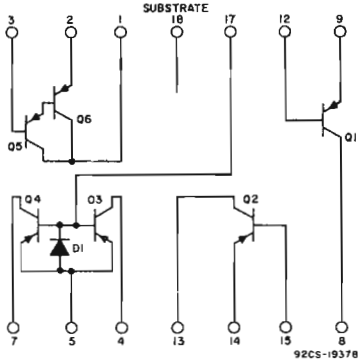
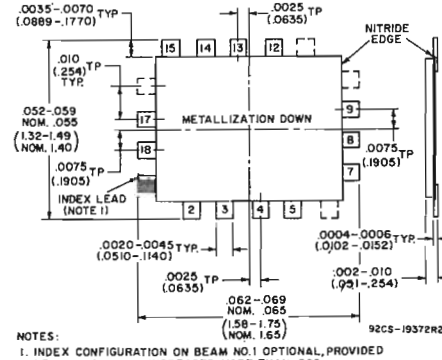


Fig. 10-1– Schematic diagram of CA3084L.

CAUTION: Substrate must be maintained negative with respect to all collector terminals of this device.

Features

- A Darlington circuit (Q5 and Q6)
- A current-mirror pair with diode (Q3, Q4, and D1)
- Matched transistor pair (Q1 and Q2)
  V_{IO} (V_{BE} matched): ±6.0 mV max.
  I_{IO} (at 100 μA): ±0.6 μA
- Wide operating current range
- Low noise figure – 3.2 dB typ. at 1 kHz
- Operation over the full military temperature range: -55 to +125°C



NOTES:

1. INDEX CONFIGURATION ON BEAM NO.1 OPTIONAL, PROVIDED LEAD MAX. 'IS NOT INCREASED MORE THAN .002
2. LEADS AT TRUE POSITION (TP) WITHIN .002 TOTAL (REF. USANS Y14.5-1966)
3. SILICON MUST NOT EXTEND BEYOND NITRIDE OVER A BEAM.

Fig. 10-2– Terminal layout for CA3084L (18-lead configuration)

CAUTION: Although RCA-CA3084L is electrically similar to CA3084, it is not a pin-for-pin replacement.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CEO}) . . . . . −40 V
Ambient Temperature Range:
Operating . . . . . -55° to +125°C
Storage . . . . . -65 to +150°C
Collector-to-Base Voltage (V_{CBO}) . . . . . −40V
Base-to-Substrate Voltage (V_{BIO})* . . . . . −40 V.
Emitter-to-Base Voltage (V_{EBO}) . . . . . −40 V
Collector Current (I_C) . . . . . −10 mA

*The base of each transistor of the CA3084L is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any base voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal 18 should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.*

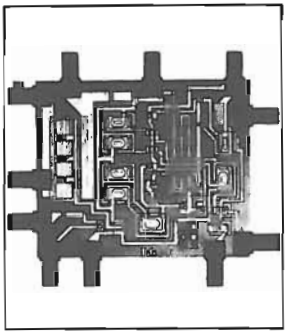
ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
For Each Transistor:						
Collector-Cutoff Current	I_{CBO}	V_{CB} = −10V, I_E = 0	—	-0.055	-100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	—	-0.12	-100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_{CE} = -100μA, I_B = 0	-40	-70	—	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_{CB} = -100μA, I_E = 0	-40	-80	—	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_{EB} = -100μA, I_C = 0	-40	-100	—	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	I_{EI} = 100μA	-40	-100	—	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_E = 1mA, I_B = 100μA	—	-0.125	-0.25	V
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = -10V	-0.50	-0.59	-0.68	V
DC Forward-Current Transfer Ratio	h_{FE}		15	40	—	
For Transistors Q1 and Q2 (As a Differential Amplifier):						
Magnitude of Input Offset Voltage	$\lvert V_{IO}\rvert$	I_E = 100μA, V_{CE} = -10V	—	0.422	6	mV
Input Offset Current	I_{IO}		-0.6	0	0.6	μA
For Transistors Q3 and Q4 (Current-Mirror Configuration):						
Collector Current Normalized	I_C/I_{17}	V_{CE} = -5V, V_{CIO} = -5V	0.85	1.00	1.15	—
Magnitude of Collector Current Ratio	$\lvert I_{C(Q3)}/I_{C(Q4)}\rvert$	Term. 5 = Gnd. I_{17} = -100μA	0.90	1.00	1.10	
For Transistors Q5 and Q6 (Darlington Configuration):						
Collector-Cutoff Current	I_{CEO}	V_{CE} = -10V, I_B = 0	—	—	-1.0	μA
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = -10V	0.92	1.07	1.20	V
DC Forward-Current Transfer Ratio	h_{FE}		100	1230	—	

Linear Integrated Circuits

Monolithic Silicon

CA3085L



Positive Voltage Regulator

Applications

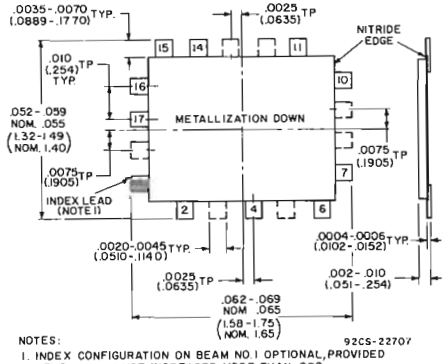
- Shunt voltage regulator
- Current regulator
- Switching voltage regulator
- High-current voltage regulator
- Combination positive and negative voltage regulator
- Dual tracking regulator
- Operation over the full military temperature range: −55 to +125°C

RCA-CA3085L is the beam-lead version of the CA3085. It is designed specifically for service as a voltage regulator at output voltages ranging from 1.8 to 26 volts at currents up to 12 mA without the use of external pass transistors. However the CA3085L can provide voltage regulation at load currents greater than 100 mA with the use of suitable external pass transistors. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

Features

- Excellent temperature coefficient
- Input and output short-circuit protection
- Load and line regulation: 0.025%
- Adjustable output voltage

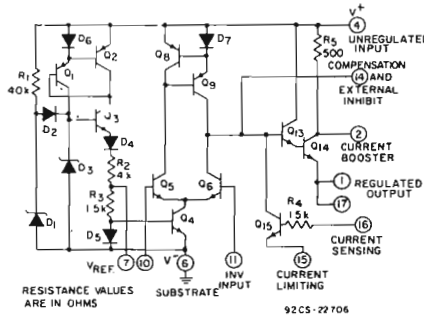
It should be noted that the CA3085L chip has eleven active circuit-access terminals, whereas the CA3085 Series packaged units have only eight access terminals. The additional terminals in the CA3085L provide greater flexibility in circuit applications.



NOTES:

1. INDEX CONFIGURATION ON BEAM NO.1 OPTIONAL, PROVIDED LEAD MAX. IS NOT INCREASED MORE THAN .002
2. LEADS AT TRUE POSITION (TP) WITHIN .002 TOTAL (REF. USANS Y14.5-1966)
3. SILICON MUST NOT EXTEND BEYOND NITRIDE OVER A BEAM.

Fig. 11-1— Terminal layout for CA3085L (18-lead configuration).



Caution: Although RCA-CA3085L is electrically similar to the CA3085, it is not a pin-for-pin replacement.

Fig. 11-2—Schematic diagram of CA3085L.

MAXIMUM RATINGS, *Absolute-Maximum Values, at* $T_A = 25^oC$

Temperature Range:

Operating ..... −55 to +125°C

Storage ..... −65 to +150°C

Unregulated Input Voltage ..... 30 V

Maximum Voltage Ratings:
The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 14 and horizontal Terminal No. 1 and 17 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERMINAL No.	7	10	11	14	15	16	1&17	2	4	6
7	–	*		*						+10 0
10	–	–	+5 −5			*				
11	–	–	–				*			*
14	–	–	–	–	+3 −10	+10 −1	+3 −10			+30 0
15	–	–	–	–	–	+5 −1				*
16	–	–	–	–	–	–	+3 −10	*	*	*
1&17	–	–	–	–	–	–	–	+10 −30	0 −30	+30 0
2	–	–	–	–	–	–	–	–	–	+30 0
4	–	–	–	–	–	–	–	–	–	+30 0
6	–	–	–	–	–	–	–	–	–	Substrate

* Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
7	10	1
10	1	-0.1
11	1	−0.1
14	1	−1
15	0.1	10
16	—	—
1&17	20	150
2	150	60
4	150	60
6	—	—

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $T_A = 25^oC$ (Unless indicated otherwise)		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.
Reference Voltage	V_{REF}	$V^+_{IN} = 15$ V		1.4	1.6	1.8
Quiescent Regulator Current	$I_{quiescent}$	$V^+_{IN} = 30$ V		–	3.3	4.5
Input Voltage Range	V_{IN} (range)	–		7.5	–	30
Maximum Output Voltage	V_O (max.)	$V^+_{IN} = 30$ $R_L = 365\ \Omega$, Term. No. 6 to Gnd.		26	27	–
Minimum Output Voltage	V_O (min.)	$V^+_{IN} = 30$ V		–	1.6	1.8
Input-Output Voltage Differential	V_{IN}-V_{OUT}	–		4	–	28
Limiting Current	I_{LIM}	$V^+_{IN} = 16$ V, $V^+_{OUT} = 10$ V $R_{SCP}^* = 6\ \Omega$		–	96	120
Load Regulation●	–	$I_L = 1$ to 12 mA, $R_{SCP} = 0$		–	0.003	0.1
Line Regulation▲	–	$I_L = 1$ mA, $R_{SCP} = 0$		–	0.025	0.1
		$I_L = 1$ mA, $R_{SCP} = 0$ $T_A = 0^oC$ to $+70^oC$		–	0.04	0.15
Equivalent Noise Output Voltage	V_{NOISE}	V^+_{IN}=25 V	$C_{REF} = 0$	–	0.5	–
			$C_{REF} = 0.22\ \mu F$	–	0.3	–
Ripple Rejection	–	V^+_{IN}=25 V f = 1 kHz	$C_{REF} = 0$	–	50	–
			$C_{REF} = 2\ \mu F$	–	56	–
Output Resistance	r_O	$V^+_{IN} = 25$ V, f = 1 kHz		–	0.075	1.1
Temperature Coefficient of Reference and Output Voltages	ΔV_{REF}, ΔV_O	$I_L = 0$, $V_{REF} = 1.6$ V		–	0.0035	–
Load Transient Recovery Time: Turn On	t_{ON}	$V^+_{IN} = 25$ V, +50 mA Step		–	1	–
Turn Off	t_{OFF}	$V^+_{IN} = 25$ V, −50 mA Step		–	3	–
Line Transient Recovery Time: Turn On	t_{ON}	V^+_{IN}=25 V, f=1 kHz, 2 V Step		–	0.8	–
Turn Off	t_{OFF}			–	0.4	–

*R_{SCP}: Short-circuit protection resistance

●Load Regulation $= \dfrac{\Delta V_{OUT}}{V_{OUT}\ (initial)} \times 100\%$

▲Line Regulation $= \dfrac{(\Delta V_{OUT})}{[V_{OUT}\ (initial)]\ (\Delta V_{IN})} \times 100\%$

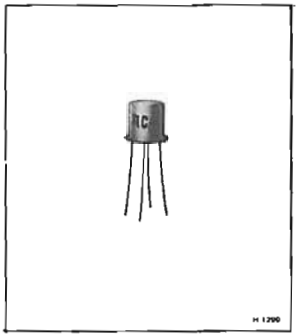
Technical Data-DMOS Devices

RCA
Solid State
Division

MOS Field-Effect Transistors

N-Channel Depletion Types

3N128
3N143



Silicon MOS Transistors

For Amplifier, Mixer, & Oscillator Applications in Military & Industrial VHF Communications Equipment Operating up to 250 MHz

Applications

- VHF amplifiers, mixers, converters and if-amplifiers in communication receivers.
- High-impedance timing circuits
- Detectors, oscillators, frequency multipliers, phase splitters, pulse stretchers and current limiters
- Electrometer amplifiers
- Voltage-controlled attenuators
- High impedance differential amplifiers

RCA-3N128 and 3N143 are N-channel depletion-type silicon insulated-gate field-effect transistors utilizing the MOS* construction. The 3N128 is intended primarily for VHF amplifier service in military and industrial applications. It also is extremely well suited for use in dc and low-frequency amplifier applications requiring a transistor having high power gain, very high input impedance, and low gate leakage.

The 3N143 is designed for use as a VHF mixer and oscillator. Because of their improved transfer characteristic and increased dynamic range the 3N128 and 3N143 provide substantially better cross-modulation performance in linear amplifier applications than conventional (bipolar) transistors and are free from diode-current loading common to junction type FET's. These transistors are hermetically sealed in JEDEC TO-72 metal packages.

Application data for RCA-3N128, including biasing requirements, basic circuit configurations, selection of optimum operating point, and methods for automatic gain control are given in RCA Application Note AN-3193, "Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor".

* Metal-Oxide -Semiconductor.

Performance Features

- Large dynamic range
- Greatly reduces spurious responses in rceiver front ends
- Permits use of vacuum-tube biasing techniques
- Excellent thermal stability
- Superior crossmodulation capability

Device Features

- Low noise figure (3N128) – 3.5 dB typ. at 200 MHz
- High VHF amplifier gain (3N128) – 16 dB typ. at 200 MHz
- Low input capacitance – 5.5 pF typ.
- High transconductance – 7500 μmho typ.
- High input resistance – 10^{14} Ω typ.
- High conversion gain (3N143, mixer) – 13.5 dB typ. at 200 MHz

Maximum Ratings, *Absolute-Maximum Values at* T_A = 25° C:

*DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 V
*DRAIN-TO-GATE VOLTAGE, V_{DG}	+20 V
*GATE-TO-SOURCE VOLTAGE, V_{GS}:	
Continuous dc	+1, -8 V
Peak ac	±15 V
*DRAIN CURRENT, I_D	50 mA
*TRANSISTOR DISSIPATION, P_T:	
At Ambient up to 25°C	330 mW
Temperatures above 25°	Derate 2.2 mW/°C
*AMBIENT TEMPERATURE RANGE:	
Storage and Operating	-65 to +175°C
*LEAD TEMPERATURE (During soldering):	
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265 °C

*In accordance with Jedec Registration Data Format JS9-RDF11B.

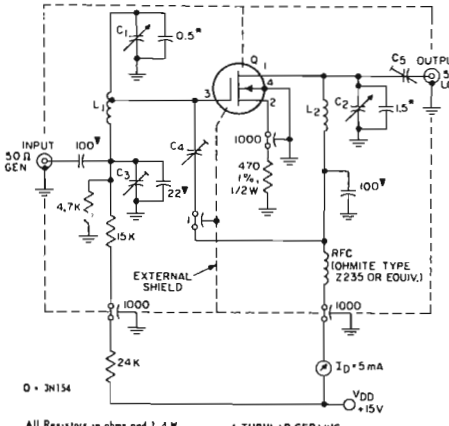
11-67

ELECTRICAL CHARACTERISTICS: (At T_A = 25°C)

Measured with Substrate Connected to Source Unless Otherwise Specified.

	CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS 3N128 MIN.	3N128 TYP.	3N128 MAX.	3N143 MIN.	3N143 TYP.	3N143 MAX.	UNITS
*	Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = −8 V T_A = 25°C	–	0.1	50	–	0.1	1000	pA
			V_{DS} = 0, V_{GS} = −8 V T_A = 125°C	–	–	5	–	–	200	nA
*	Zero-Bias Drain Current	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	5	15	25	5	15	30	mA
*	Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{DS} = 20 V, V_{GS} = −8 V	–	–	50	–	–	50	μA
*	Gate-to-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 50 μA	−0.5	−3	−8	−0.5	−3	−8	V
*	Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5,000	7,500	12,000	5,000	7,500	12,000	μmho
*	Drain-to-Source Channel Resistance	$r_{DS(on)}$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	–	200	–	–	200	–	Ω
*	Small-Signal Short-Circuit Reverse Transfer Capacitance▲	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.15	0.25	0.35	0.12	0.25	0.38	pF
*	Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	–	5.5	7	–	5.5	7	pF
			Common-Source Configuration							
*	Input Admittance	Y_{is}	f = 200 MHz	–	0.4 + J7.3	–	–	–	–	mmho
*	Forward Transfer Admittance	Y_{ss}	V_{os} = 15 Volts	–	7 − J2	–	–	–	–	mmho
*	Output Admittance	Y_{os}	I_D = 5 mA	–	0.28 + J1.8	–	–	–	–	mmho
*	Maximum Available Power Gain	MAG	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz		21	–	–	–	–	dB
*	Insertion Power Gain (Fixed Neutralization) See Fig. 1	G_{PS}		13.5	16	–	–	–	–	dB
	Power Gain (Conversion (See Fig. 3)	$G_{PS(c)}$	V_{DS} = 15 V, I_O = 1 mA, f_{in} = 200 MHz, f_{out} = 30 MHz	–	–	–	10	13.5	–	dB
	Noise Figure (See Fig. 1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	–	3.5	5	–	–	–	–

*In accordance with JEDEC Registration Data Format JS9-RDF-11B.
▲Three-Terminal Measurement: Source Returned to Guard Terminal.



All Resistors in ohms and 1/4 W unless otherwise specified
All Capacitors in pF

* TUBULAR CERAMIC
* DISC CERAMIC

92CS-14892R1

C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig. 1 - Test circuit used to measure 200-MHz maximum usable power gain and noise figure for 3N128

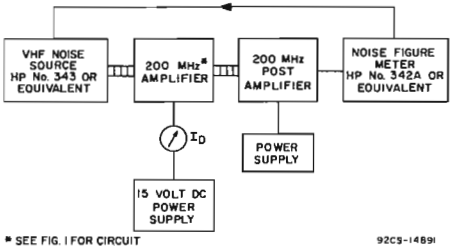


Fig. 2 - Noise figure measurement setup for 3N128

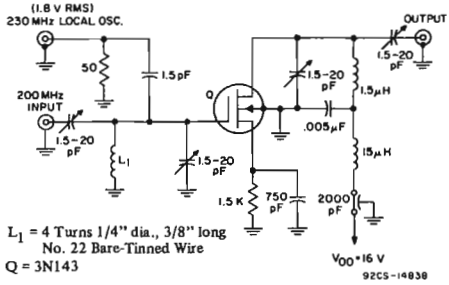


Fig. 3 - Conversion power gain test circuit for 3N143

Typical Characteristics for Types 3N128 and 3N143

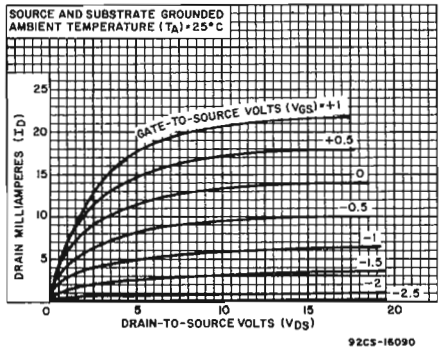


Fig. 4 - Drain current vs. drain-to-source voltage

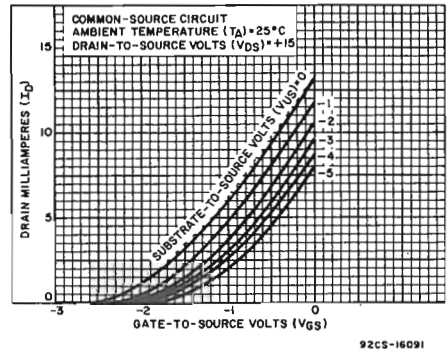


Fig. 5 - Drain current vs. gate-to-source voltage (V_{GS})

Typical Y-Parameters for Types 3N128 and 3N143

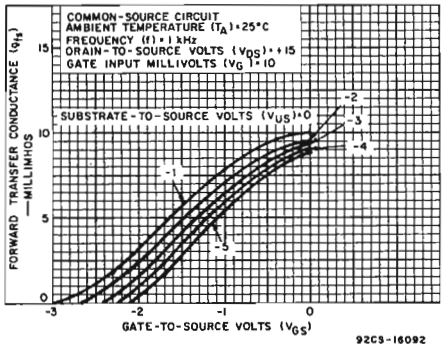


Fig. 6 - Forward transconductance vs. gate bias voltage

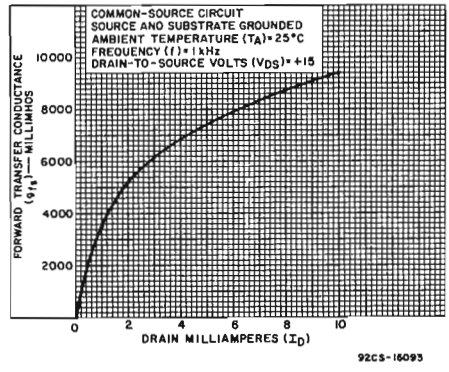


Fig. 7 - Forward transconductance vs. drain current

Typical Y-Parameters for Types 3N128 and 3N143

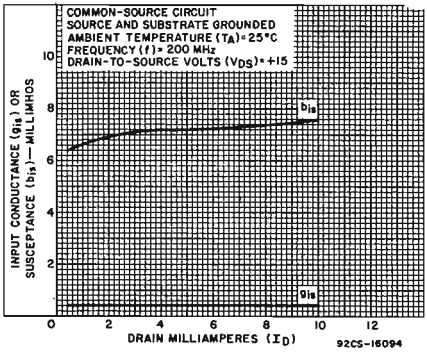


Fig. 8 - Input admittance vs. drain current

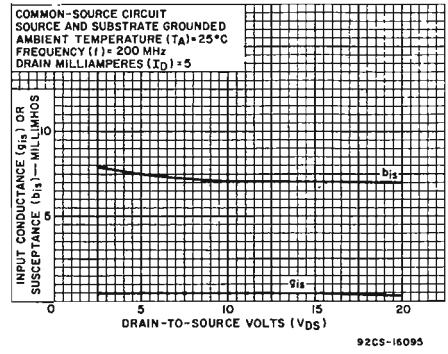


Fig. 9 - Input admittance vs. drain-to-source voltage

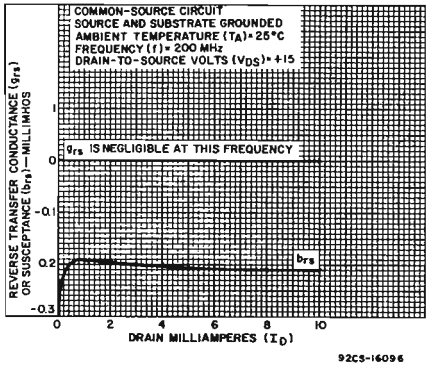


Fig. 10 - Reverse transadmittance vs. drain current

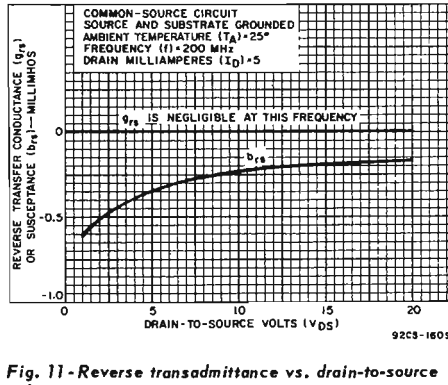


Fig. 11 - Reverse transadmittance vs. drain-to-source voltage

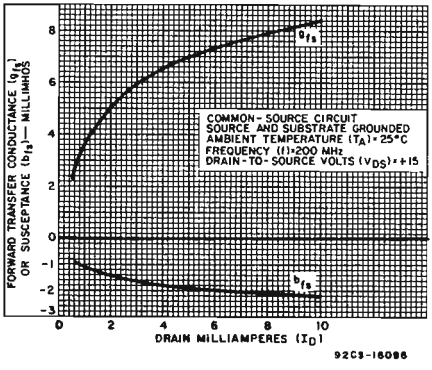


Fig. 12 - Forward transadmittance vs. drain current

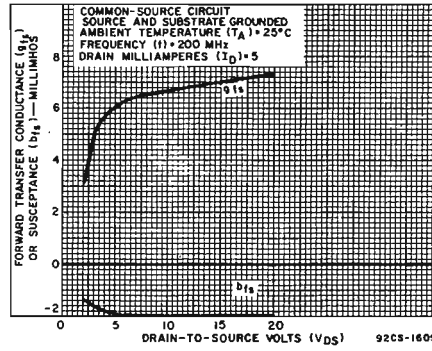


Fig. 13 - Forward transadmittance vs. drain-to-source voltage

Typical Characteristics for Types 3N128 and 3N143

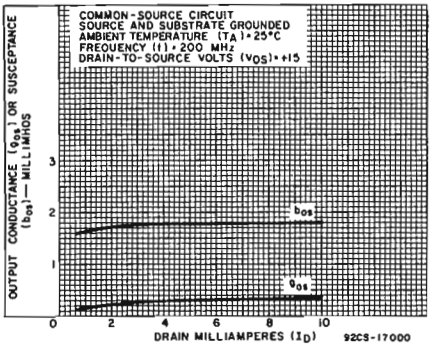


Fig. 14 - Output admittance vs. drain current

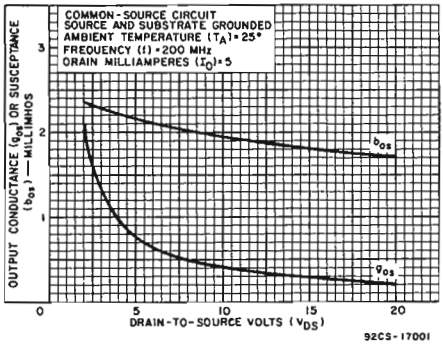


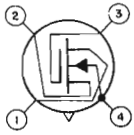
Fig. 15 - Output admittance vs. drain-to-source voltage

OPERATING CONSIDERATIONS

The flexible leads of the 3N128 and 3N143 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the devices against high electric fields.

This device should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent danage to the device.

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

RCA Solid State Division

MOS Field-Effect Transistors

N-Channel Depletion Type

3N138

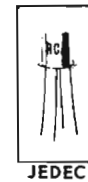
Applications

- Servo Amplifiers
- Telemetry Amplifiers
- Computer Operational Amplifiers
- Sampling Circuits
- Electrometer Amplifiers

Features

- excellent thermal stability
- zero inherent offset voltage
- low leakage current: 10 pA max.
- low "on" resistance — $r_{DS}(on) = 240\Omega$ typ. ($V_{GS} = 0V$)
- high "off" resistance — $R_{DS}(off) = 10^{10}\Omega$ typ.
- low feedback capacitance — $C_{rss} = 0.18pF$ typ.
- low input capacitance — $C_{iss} = 3pF$ typ.

SILICON INSULATED-GATE FIELD-EFFECT TRANSISTOR N-Channel Depletion Type



JEDEC TO-72

For Critical Chopper Applications and Multiplex Service up to 60 MHz: in Military Communications, Navigation, and Instrumentation Equipment in Industrial Instrumentation and Control Circuits

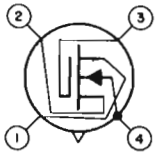
RCA-3N138 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is intended primarily for critical chopper and multiplex applications up to 60MHz.

The insulated gate provides a very high value of input resistance (10^{14} ohms typ.) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N138 also features extremely low feed-through capacitance (0.18pF typ.) and zero inherent offset voltage.

The 3N138 is hermetically sealed in the JEDEC TO-72 package and features a gate metallization that covers the entire source-to-drain channel.

* Metal-Oxide-Semiconductor.

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

Maximum Ratings, Absolute-Maximum Values:

(Substrate connected to source unless otherwise specified)

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+35 max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+35, −0.3 max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+35, −0.3 max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	±10 max.	V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max.	V
PEAK VOLTAGE, GATE-TO-ALL OTHER TERMINALS: V_{GS}, V_{GD}, V_{GB}, non-repetitive	±45 max.	V
DRAIN CURRENT, I_D (Pulse duration 20 ms, duty factor ≤ 0.10)	50 max.	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330 max.	mW
above 25°C	Derate linearly at 2.2 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage	−65 to +150	°C
Operating	−65 to +125	°C
LEAD TEMPERATURE (During Soldering): At distances ≥ 1/32" to seating surface for 10 seconds max.	265 max.	°C

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, Unless Otherwise Specified. Substrate Connected to Source.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Type 3N138			UNITS
			Min.	Typ.	Max.	
Gate-Leakage Current	I_{GSS}	$V_{GS} = \pm 10$, $V_{DS} = 0$, $T_A = 25°C$ $V_{GS} = \pm 10$, $V_{DS} = 0$, $T_A = 125°C$	— —	0.1 20	10 200	pA pA
Drain-to-Source "ON" Resistance	$r_{DS}(on)$	$V_{GS} = 0$, $V_{DS} = 0$, f = 1 KHz, $T_A = 25°C$ $V_{GS} = +10$, $V_{DS} = 0$, f = 1 KHz, $T_A = 25°C$ $V_{GS} = 0$, $V_{DS} = 0$, f = 1 KHz, $T_A = 125°C$	— — —	240 135 350	350 — —	Ω Ω Ω
Drain-to-Source "OFF" Resistance	$R_{DS}(off)$	$V_{GS} = -10$, $V_{DS} = +1$	2×10^8	10^{10}	—	Ω
Drain-to-Source Cutoff Current	$I_{D}(off)$	$V_{GS} = -10$, $V_{DS} = +1$, $T_A = 25°C$ $V_{GS} = -10$, $V_{DS} = +1$, $T_A = 125°C$	— —	0.01 0.01	5 0.5	nA μA
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	$V_{GS} = -10$, $V_{DS} = 0$, f = 1 MHz	—	0.25	0.4	pF
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	$V_{GS} = -10$, $V_{DS} = 0$, f = 1 MHz	—	3	5	pF
Zero-Gate-Bias Forward Transconductance	g_{fo}	$V_{DS} = 12$, $I_D = 5$ mA	—	6000	—	μmho
Offset Voltage	V_O	$V_{GS} = \pm 10$, $V_{DS} = 0$	—	0*	—	V

* In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. There errors may be minimized by the use of solder having a low thermal e.m.f. such as Leeds & Northrup No.107-1.0.1, or equivalent.

OPERATING CONSIDERATIONS

The flexible leads of the 3N138 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields.

This device should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the device.

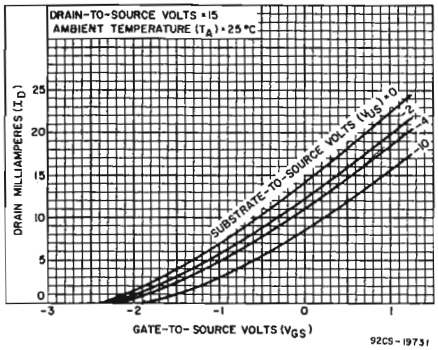


Fig. 1 — Drain Current vs Gate-to-Source Voltage

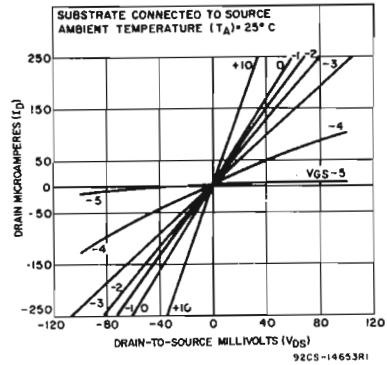


Fig. 2 — Low-Level Drain Current vs Drain-to-Source Voltage

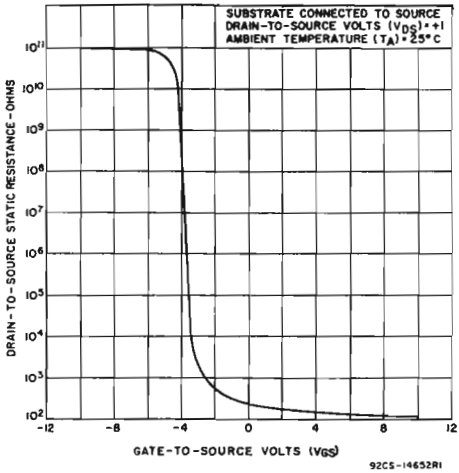


Fig. 3 — Drain-to-Source Static Resistance vs Gate-to-Source Voltage

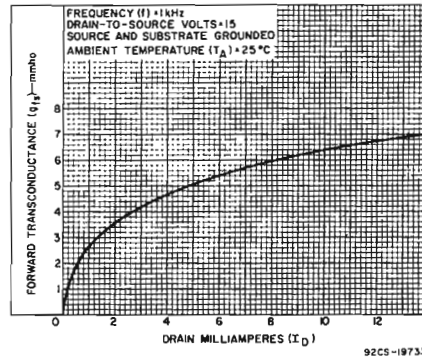


Fig. 4 — 1 KHz forward transconductance vs drain current

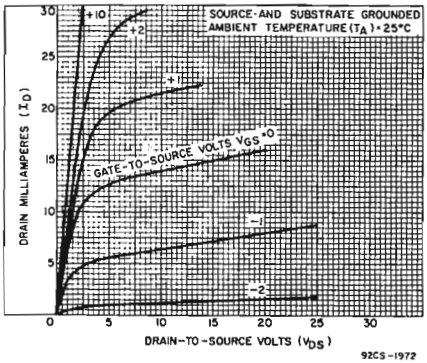


Fig. 5 — Drain Current vs Drain Voltage

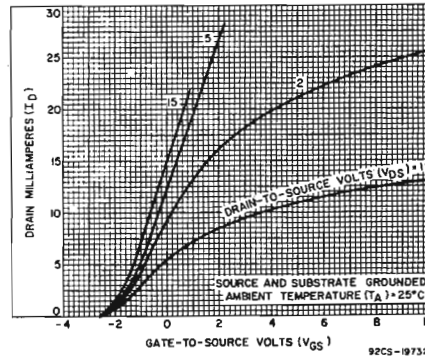


Fig. 6 — Drain Current vs Gate-to-Source Voltage

RCA Solid State Division

MOS Field-Effect Transistors

N-Channel Depletion Type

3N139

RCA 3N139 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is a general purpose transistor especially suited for audio, video, and rf applications, and for wide-band amplifier designs. The insulated gate provides a very high input resistance (10^{14} Ω typ.) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N139 also has a high transconductance, a low value of input capacitance (3 pF typ.), and a very low feedback capacitance (0.19 pF typ.).

The 3N139 is hermetically sealed in the standard 4-lead JEDEC TO-72 package.

Maximum Ratings, *Absolute-Maximum Values:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+35 max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+35, -0.3 max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+35, -0.3 max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	±10 max.	V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max.	V
PEAK VOLTAGE, GATE-TO-ALL OTHER TERMINALS; V_{GS}, V_{GD}, V_{GB}, non-repetitive	±42 max.	V
DRAIN CURRENT, I_D	50 max.	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
above 25°C	Derate linearly at 2.2 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distance not closer than 1/32 inch to seating surface for 10 seconds max.	265 max.	°C

* Metal-Oxide-Semiconductor

SILICON MOS TRANSISTOR

For Audio, Video, and RF Amplifier Applications

JEDEC TO-72

in Military Communications, Instrumentation, & Navigation Equipment

in Mobile and Fixed Communication Equipment

in Industrial Instrumentation and Control Circuits

FEATURES

- high input resistance $R_{GS} = 10^{14}$ Ω typ.
- low input capacitance $C_{iss} = 3$ pF typ.
- low feed back capacitance $C_{rss} = 0.2$ pF typ.
- low gate leakage current $I_{GSS} = 0.1$ nA typ.
- high drain-to-source voltage: +35 max. V

ELECTRICAL CHARACTERISTICS, at T_A = 25° C Unless Otherwise Specified. Bulk (Substrate) Connected to Source

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS			UNITS
		FREQUENCY f	DC DRAIN-TO-SOURCE VOLTAGE V_{DS}	DC GATE-TO-SOURCE VOLTAGE V_{GS}	DC DRAIN CURRENT I_D				
		MHz	V	V	mA	Min.	Typ.	Max.	
Drain-to-Source Cutoff Current	$I_{D(OFF)}$		15	−8		—	—	50	μA
Zero-Bias Drain Current*	I_{DSS}		15	0		5	15	25	mA
Gate Reverse Current	I_{GSS}	T_A = 25°C	0	±10		—	—	1	nA
		T_A = 100°C	0	±10		—	—	100	nA
Gate-to-Source Cutoff Voltage	$V_{GS(OFF)}$		15		0.05	−2	−4	−6	V
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15		5	0.05	0.2	0.4	pF
Input Resistance	r_{is}	100	15		5		12	—	kΩ
Input Capacitance	C_{iss}	100	15		5	—	3	10	pF
Output Resistance	r_{os}	100	15		5		6	—	kΩ
Output Capacitance	C_{oss}	100	15		5	—	1.4	—	pF
Forward Transconductance	g_{fs}	1 kHz	15		5		5	—	mmho

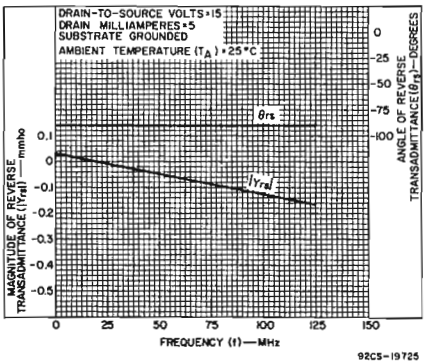


Fig. 1 – Reverse Transadmittance vs Frequency

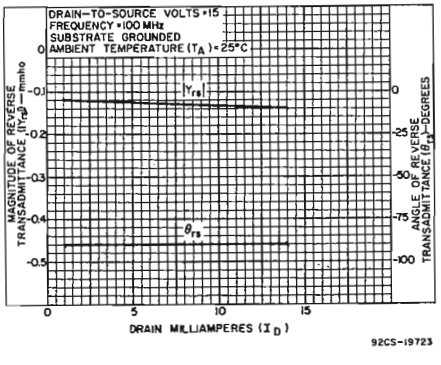


Fig. 2 – Reverse Transadmittance vs Drain Current

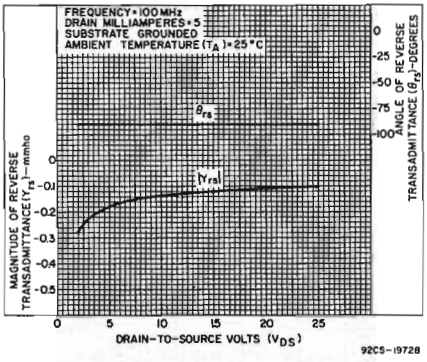


Fig. 3 — Reverse Transadmittance vs Drain-Source Voltage

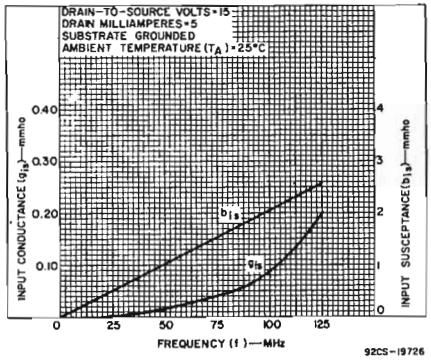


Fig. 4 — Input Admittance vs Frequency

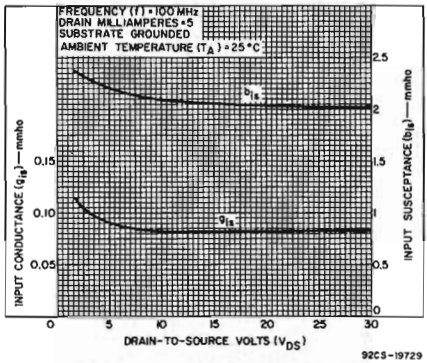


Fig. 5 — Input Admittance vs Drain-Source Voltage

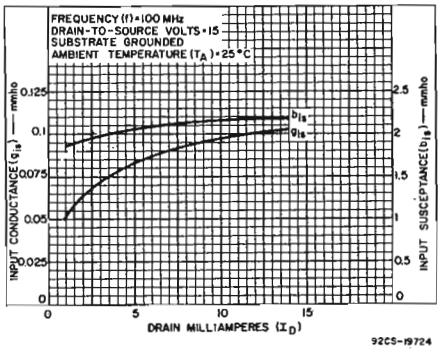


Fig. 6 — Input Admittance vs Drain Current

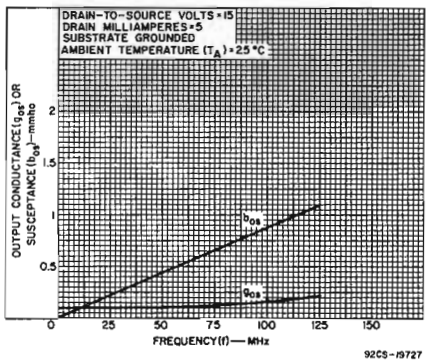


Fig. 7 — Output Conductance vs Frequency

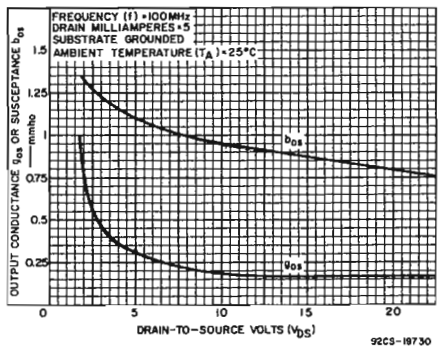


Fig. 8 — Output Admittance vs Drain-Source Voltage

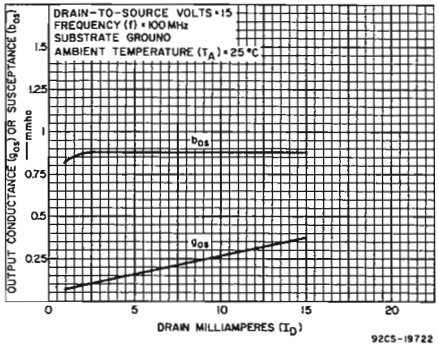


Fig. 9 – Output Admittance vs Drain Current

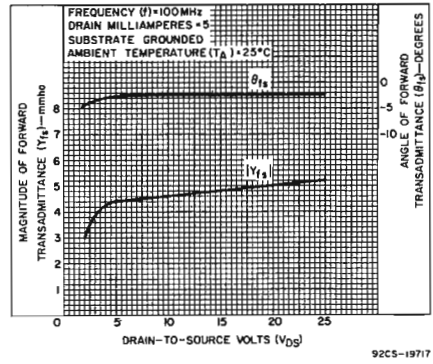


Fig. 10 – Forward Transadmittance vs Drain-Source Voltage

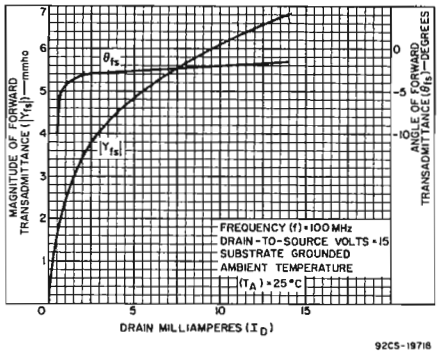


Fig. 11 – Forward Transadmittance vs Drain Current

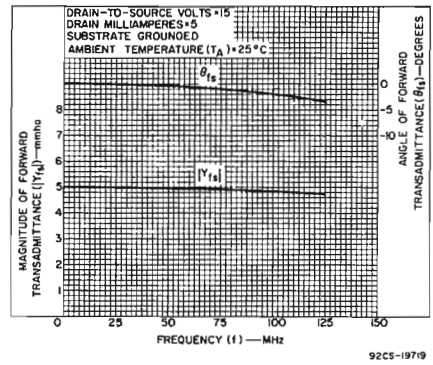


Fig. 12 – Forward Transadmittance vs Frequency

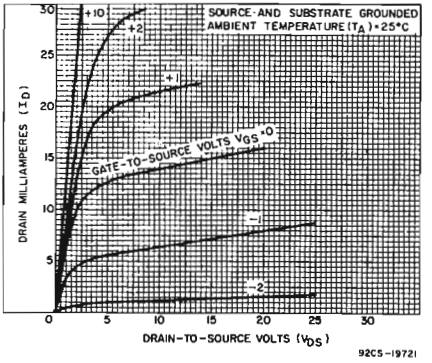


Fig. 13 – Drain Current vs Drain Voltage

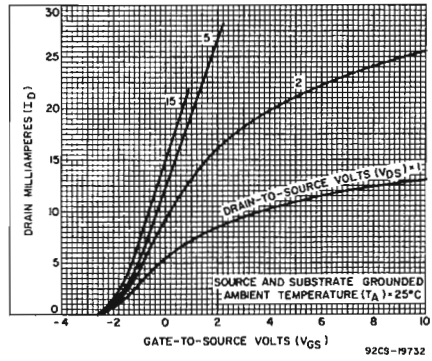


Fig. 14 – Drain Current vs Gate-to-Source Voltage

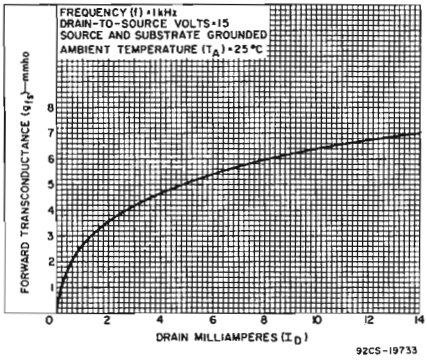


Fig. 15 – 1 KHz forward transconductance vs drain current

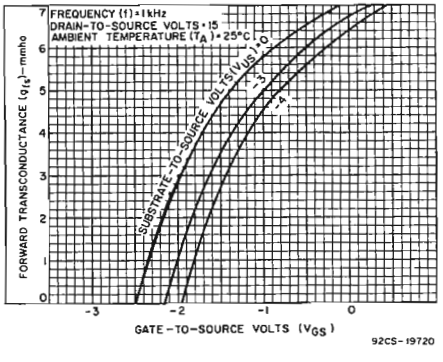
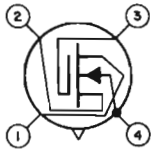


Fig. 16 – 1 KHz forward transconductance vs gate-to-source voltage

TERMINAL ARRANGEMENT



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

RCA Solid State Division

MOS Field-Effect Transistors

N-Channel Depletion Types

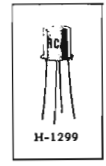
3N140

3N141

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTORS

N-Channel Depletion Types

For Military and Industrial Amplifier and Mixer Applications Up to 300 MHz



JEDEC TO-72

RCA-3N140 and 3N141* are n-channel silicon, depletion type, dual insulated-gate, field-effect transistors utilizing the MOS** construction. They have exceptional characteristics for rf-amplifier and mixer applications at frequencies up to 300 MHz. These transistors feature a series arrangement of two separate channels, each channel having an independent control gate.

The 3N140, used in a common-source configuration in which gate No.2 is ac grounded, reduces oscillator feedthrough to the antenna thereby minimizing oscillator radiation. The 3N141 provides excellent isolation between the oscillator and rf signals because each of the two signal frequencies being mixed has its own control element.

The mixing function performed by the 3N141 is unique in that the signal applied to gate No.2 is used to modulate the input-gate (gate No.1) transfer characteristic. This technique is superior to conventional "square law" mixing, which can only be accomplished in the nonlinear region of the device transfer characteristic.

The use of the 3N141 as described provides high useful conversion gains at all vhf frequencies, and the reduction in spurious responses is substantial and easily obtainable in simple circuits.

The 3N140 and 3N141 are hermetically sealed in metal JEDEC TO-72 packages.

* Formerly Dev. Nos. TA2644 and TA7274, respectively.

** Metal-Oxide-Semiconductor.

Maximum Ratings, *Absolute-Maximum Values, at* $T_A = 25^oC$

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	0 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-8 to +1	V
Peak ac	-8 to +20	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-8 to 40% of V_{DS}	V
Peak ac	-8 to +20	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
DRAIN CURRENT, I_D		
(Pulsed): Pulse duration $\leq$ 20 ms, duty factor $\leq$ 0.15	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	400	mW
At ambient temperatures above 25°C	derate linearly at 2.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances $\geq$ 1/32 inch from seating surface for 10 seconds max.	265	°C

APPLICATIONS

- RF amplifier and mixer in military and industrial communications equipment
- aircraft and marine vehicular receivers
- CATV and MATV equipment
- telemetry and multiplex equipment

PERFORMANCE FEATURES

- wide dynamic range permits large-signal handling before overload
- dual-gate permits simplified agc circuitry
- virtually no agc power required
- greatly reduces spurious responses in fm receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability
- superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's

DEVICE FEATURES

- low gate leakage currents – – I_{G1SS} & I_{G2SS} = 1 nA max. at $T_A = 25^oC$
- high forward transconductance – – g_{fs} = 6000 μmho min.
- high unneutralized RF power gain – – G_{ps} = 16 dB min. at 200 MHz
- low VHF noise figure – – 4.5 dB max. at 200 MHz

ELECTRICAL CHARACTERISTICS, at T_A = 25°C Unless Otherwise Specified. Common-Source Circuit.

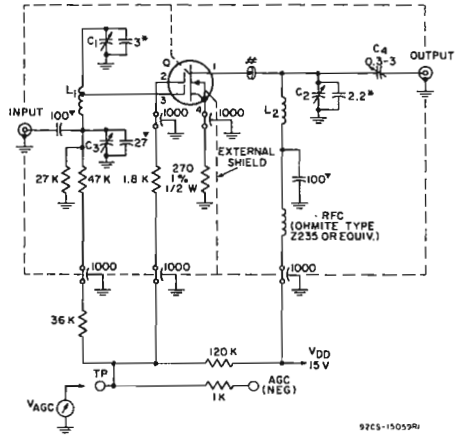
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS
			TYPE 3N140 RF AMPLIFIER			TYPE 3N141 MIXER			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Gate No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +16V, I_D = 200 μA V_{G2S} = +4V	-	-2	-4	-	-2	-4	V
Gate No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +16V, I_D = 200 μA V_{G1S} = 0	-	-2	-4	-	-2	-4	V
Gate No.1 Leakage Current	I_{G1SS}	V_{G1S} = -20V, V_{G2S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	-	-	1	nA
		V_{G1S} = +1V, V_{G2S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	-	-	1	nA
		V_{G1S} = -20V, V_{G2S} = 0 V_{DS} = 0, T_A = 125°C	-	-	0.2	-	-	0.2	μA
Gate No.2 Leakage Current	I_{G2SS}	V_{G2S} = -20V, V_{G1S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	-	-	1	nA
		V_{G2S} = +1V V_{DS} = 0, V_{G1S} = 0, T_A = 25°C	-	-	1	-	-	1	nA
		V_{G2S} = -20V, V_{G1S} = 0 V_{DS} = 0, T_A = 125°C	-	-	0.2	-	-	0.2	μA
Zero-Bias Drain Current	I_{DSS}*	V_{DD} = +14V, V_{G1S} = 0, V_{G2S} = +4	5	18	30	5	18	30	mA
Forward Transconductance (Gate No.1 to Drain)	g_{fs}	V_{DD} = +14V, I_D = 10 mA V_{G2S} = +4V, f = 1 kHz	6000	10000	18000	6000	10000	18000	μmho
Cutoff Forward Transconductance (Gate No.1 to Drain)	$g_{fs(off)}$	V_{DD} = +14V, V_{G1S} = -0.5V V_{G2S} = -2V, f = 1 kHz	-	-	100	-	-	-	μmho
Small-Signal, Short-Circuit Input Capacitance[b]	C_{iss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	3	5.5	7	3	5.5	7	pF
Small-Signal, Short-Circuit Reverse Transfer Capacitance (Drain to Gate No.1)[▲]	C_{rss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	0.01	0.02	0.03	0.01	0.02	0.03	pF
Small-Signal Short-Circuit Output Capacitance	C_{oss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	-	2.2	-	-	2.2	-	pF
Power Gain (See Fig.1 for Measurement Circuit)	G_{ps}	V_{DD} = +15V, R_S = 270Ω f = 200 MHz, R_G = 50Ω	16	18	-	-	-	-	dB
Conversion Power Gain (See Fig.2 for Measurement Circuit)	G_{psc}	V_{DD} = +15V, R_S = 120Ω, f_{IN} = 200 MHz, f_{OUT} = 30 MHz Oscillator injection voltage● = 2.5 V (rms)	-	-	-	13	17	-	dB
Measured Noise Figure (See Fig.1 for Measurement Circuit)	NF	V_{DD} = +15V, R_S = 270Ω f = 200 MHz, R_G = 50Ω	-	3.5	4.5	-	-	-	dB

* Pusle test: Pulse duration ≤ 20 ms, duty factor ≤ 0.15.

[b] Capacitance between Gate No.1 and all other terminals.

[▲] Three-Terminal Measurement with Gate No.2 and Source Returned to Guard Terminal.

● Measured from gate No.2 to source.



Q = 3N140.

▼ Disc ceramic.

* Tubular ceramic.

Ferrite bead (1/2 used); Indiana General No. H1742C-(A-147), F-1157-1-H

All resistors in ohms

All capacitors in pF

C_1, C_2: 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

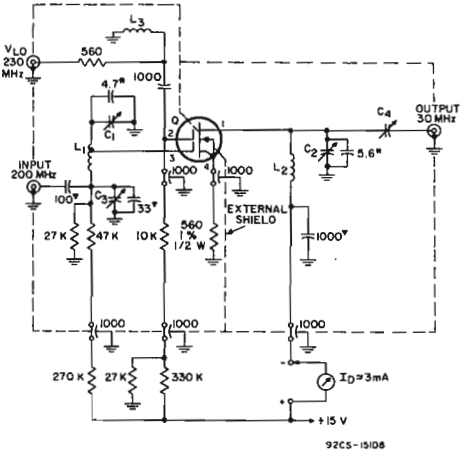
C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07 ±0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - 200 MHz power gain and noise figure test circuit for type 3N140.



Q = 3N141.

▼ Disc ceramic.

* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1, C_2: 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07 ±0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Ohmite Z-144 RF choke or equivalent.

L_3: J.W. Miller Co. #4580 0.1 μH RF choke or equivalent.

Note: If 50Ω meter is used in place of sweep detector, a low pass filter must be provided to eliminate local oscillator voltage from load.

Fig.2 - Conversion power gain test circuit for type 3N141.

OPERATING CONSIDERATIONS

The flexible leads of the 3N140 and 3N141 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the devices against high electric fields.

These devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TYPICAL CHARACTERISTICS FOR TYPES 3N140, 3N141

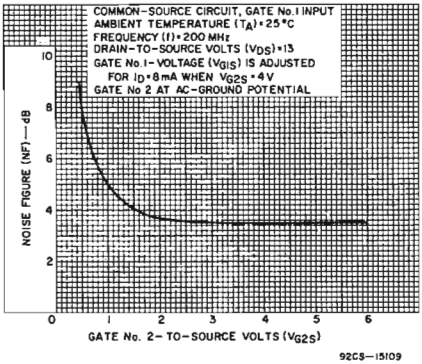


Fig.3 - NF vs V_{G2S}.

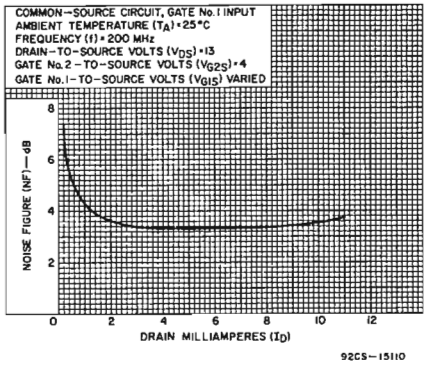


Fig.4 - NF vs I_D.

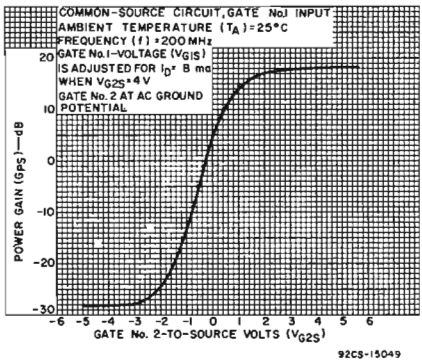


Fig.5 - G_{PS} vs V_{G2S} (For 3N140).

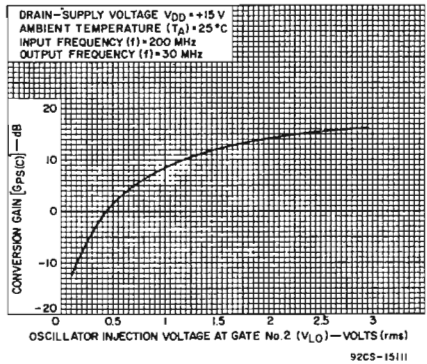


Fig.6 - $G_{PS(C)}$ vs V_{LO} (For 3N141).

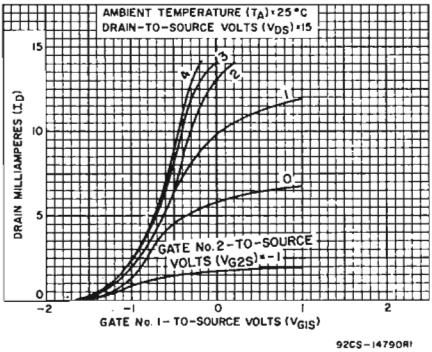


Fig.7 - I_D vs V_{G1S}.

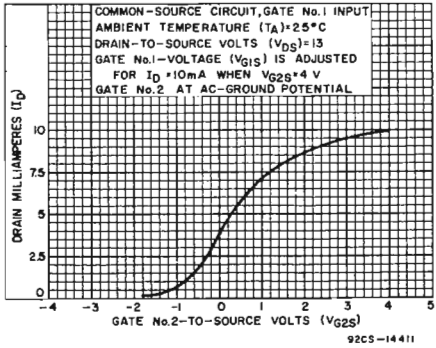


Fig.8 - I_D vs V_{G2S}.

TYPICAL CHARACTERISTICS FOR TYPES 3N140, 3N141

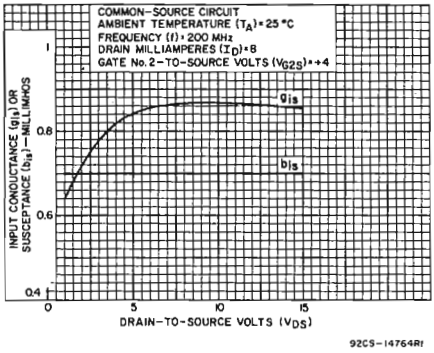


Fig.9 - y_{is} vs V_{DS}.

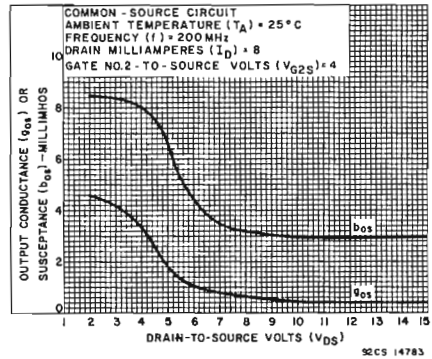


Fig.10 - y_{os} vs V_{DS}.

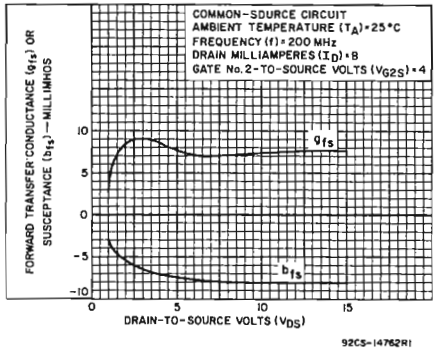


Fig.11 - y_{fs} vs V_{DS}.

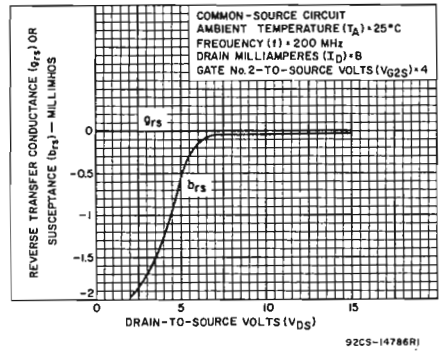


Fig.12 - y_{rs} vs V_{DS}.

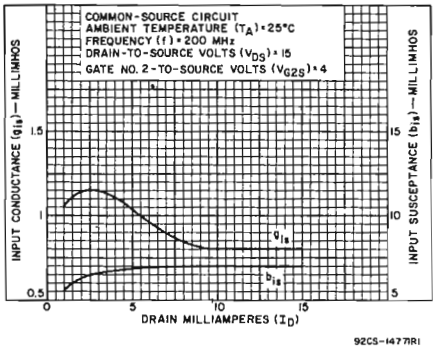


Fig.13 - y_{is} vs I_D.

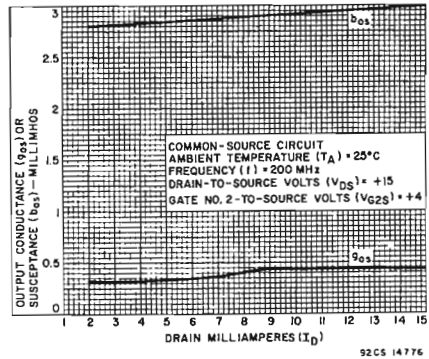


Fig.14 - y_{os} vs I_D.

TYPICAL CHARACTERISTICS FOR TYPES 3N140, 3N141

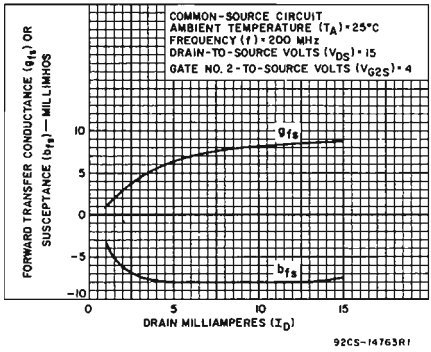


Fig.15 - y_{fs} vs I_D.

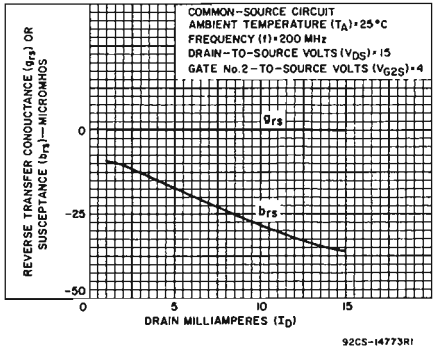


Fig.16 - y_{rs} vs I_D.

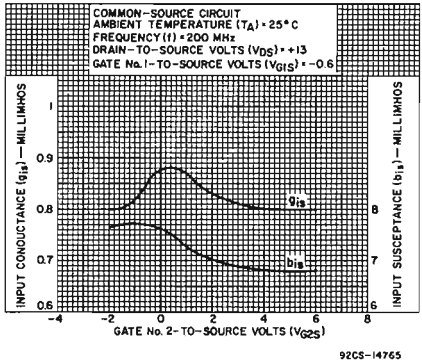


Fig.17 - y_{is} vs V_{G2S}.

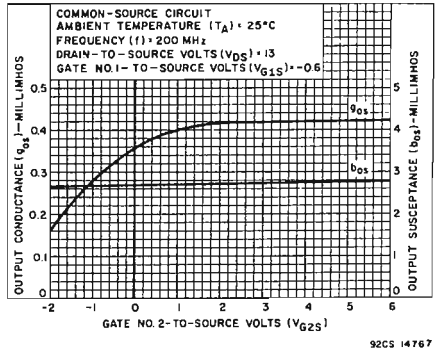


Fig.18 - y_{os} vs V_{G2S}.

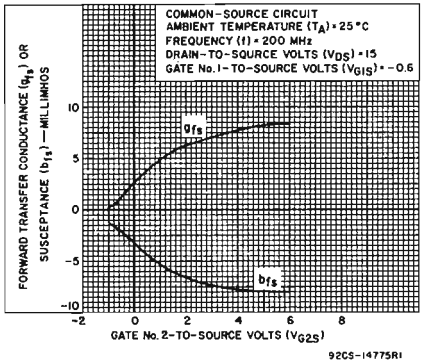


Fig.19 - y_{fs} vs V_{G2S}.

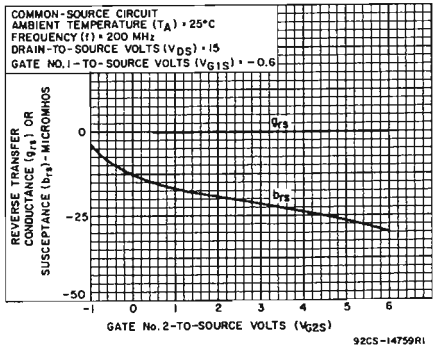


Fig.20 - y_{rs} vs V_{G2S}.

TYPICAL CHARACTERISTICS FOR TYPES 3N140, 3N141

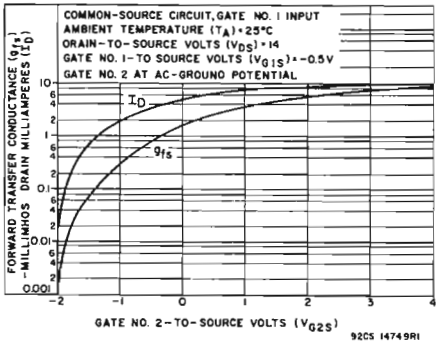


Fig.21 - g_{fs} and I_D vs V_{G2S}.

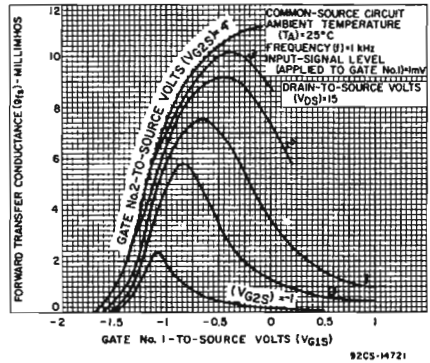


Fig.22 - g_{fs} vs V_{G1S}.

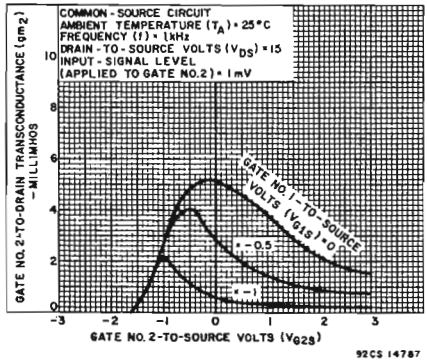
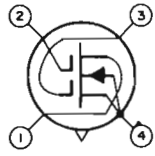


Fig.23 - g_{fs2} vs V_{G2S}.

TERMINAL DIAGRAM



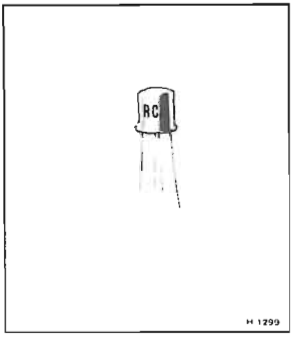
LEAD 1 - DRAIN
LEAD 2 - GATE No.2
LEAD 3 - GATE No.1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

RCA
Solid State
Division

MOS Field-Effect Transistors

N-Channel Depletion Type

3N142



Silicon MOS Transistor

For Industrial and Military Applications to 175 MHz

Applications

- RF amplifier, Mixer, and Oscillator in:
  CB and Mobile Communication Receivers
  Aircraft and Marine Receivers
  CATV and MATV Equipment
- Industrial Control Circuits
- Variable Attenuators
- Current Limiters
- Instrumentation Equipment
- High-Impedance Timing Circuits

The-3N142 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type utilizing the MOS■ construction.

The-3N142 is intended primarily for use as the rf amplifier in FM receivers and general amplifier applications at frequencies up to 175 MHz.

The wide dynamic range of the 3N142 reduces cross-modulation effects in AM receivers and minimizes the generation of spurious responses in FM receivers.

■ Metal-Oxide-Semiconductor

Performance Features

- Large dynamic range
- Enhanced signal-handling capability for low cross-modulation
- Dual-polarity gate permits positive and negative swing without degradation of input impedance
- Reduced spurious responses in FM receivers
- Permits use of vacuum-tube biasing techniques
- Excellent thermal stability for critical oscillator designs

Device Features

- High input resistance – 1000 megohms
- Low feedback capacitance – 0.35 pF max.
- Low noise figure – 2.5 dB typ.
- High useful power gain – neutralized – 16 dB min. at 100 MHz
- Hermetically sealed TO – 72 metal package

Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25°C$

*DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	V
*DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
*GATE-TO-SOURCE VOLTAGE, V_{GS}:		
Continuous	+1 to −8	V
Peak ac	±15	V
*DRAIN CURRENT, I_D	50	mA
*TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	Derate at 2.2 mW/°C	
*AMBIENT TEMPERATURE RANGE:		
Storage	−65 to +175	°C
Operating	−65 to +175	°C
*LEAD TEMPERATURE (During Soldering): At distances ≥ 1/32" from seating surface for 10 seconds max.	265	°C

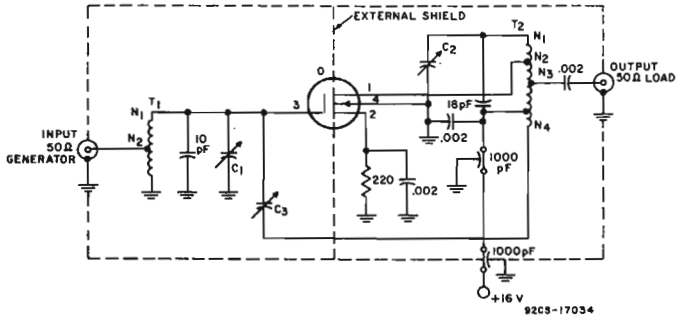
*In accordance with JEDEC Regiatration Data Format JS-9 RDF11-B

ELECTRICAL CHARACTERISTICS: (At T_A = 25° C)

Measured with Substrate Connected to Source Unless Otherwise Specified.

	CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
*	Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8 V, T_A = 25° C	-	0.0001	1	nA
			V_{DS} = 0, V_{GS} = -8 V, T_A = 125° C	-	-	200	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 25° C	-	0.0001	1	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 125° C	-	-	200	nA
*	Zero-Bias Drain Current**	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	5	15	25	mA
*	Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{DS} = 20 V, V_{GS} = -8 V	-	-	50	μA
*	Gate-to-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 50 μA	-0.5	-3	-8	V
*	Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7500	12,000	μmho
*	Drain-to-Source Channel Resistance	$r_{DS(on)}$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	-	200	-	Ω
*	Small-Signal Short-Circuit Reverse Transfer Capacitance‡	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.10	0.22	0.35	pF
*	Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	5.5	7	pF
*	Input Admittance	Y_{is}	Common Source Configuration f = 100 MHz V_{DS} = 15V I_D = 5 mA	-	0.155+J3.45	-	mmho
*	Forward Transfer Admittance	Y_{fs}		-	7.5-J0.9	-	mmho
*	Output Admittance	Y_{os}		-	0.21+J0.9	-	mmho
*	Maximum Available Power Gain	MAG	V_{DS} = 15 V, I_D = 5 mA, f = 100 MHz	-	26	-	dB
	Maximum Usable Power Gain (Fixed Neutralization)	MUG		-	17	-	
*	Insertion Power Gain** (Fixed Neutralization)	G_{ps}		16	-	-	dB
*	Noise Figure**	NF	V_{DS} = 15 V, I_D = 5 mA, f = 100 MHz	-	2.5	4	dB

* In accordance with JEDEC Registration Data Format JS-9 RDF-11B ‡ Three-Terminal Measurement: Source Returned to Guard Terminal
**See Fig. 1



T_1 N_1 = 6 Turns #20 Tinned Copper Wire; ¼" I.D. ½" Long
Q_o = 205, N_1/N_2 = 4.85

T_2 $N_1 + N_4$ = 6¾ Turns #20 Tinned Copper Wire ¼" I.D. 9/16" Long
Q_o = 190 N_1/N_2 = 1.9 N_1/N_3 = 12.3 N_1/N_4 = 8

C_1 = 10 pF Variable Air Capacitor (Hammarlund Mac-10 or Equivalent)
C_2 = 5 pF Variable Air Capacitor (Hammarlund Mac-5 or Equivalent)
C_3 = 0.7-3 pF Piston-Type Variable Air Capacitor (Erie 535C or Equivalent)
Q = 3N142

Fig. 1 - Test Set Up for 100 MHz Insertion Power Gain and Noise Figure

TYPICAL CHARACTERISTICS

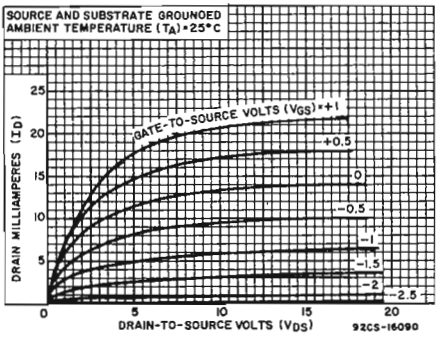


Fig. 2 - Drain Current vs Drain-to-Source Voltage.

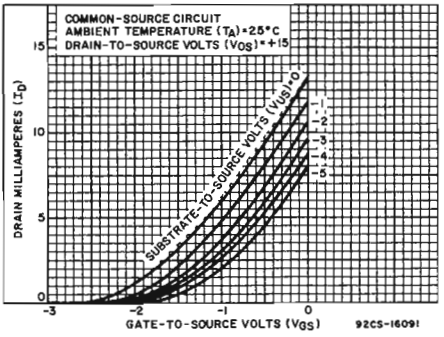


Fig. 3 - Drain Current vs Gate-to-Source Voltage (V_{gs}).

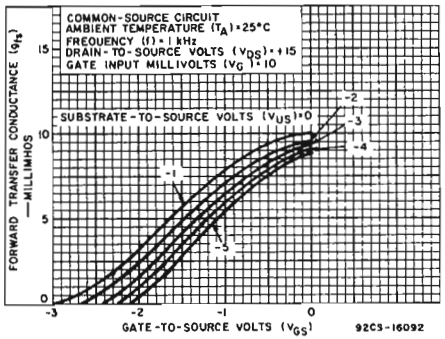


Fig. 4 - Forward Transconductance vs Gate Bias Voltage.

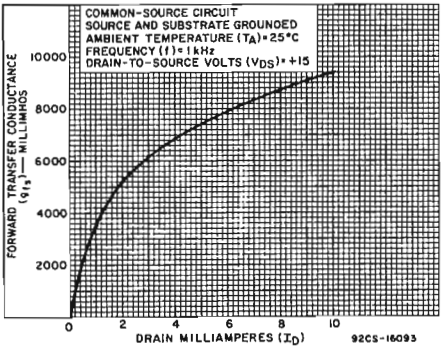


Fig. 5 - Forward Transconductance vs Drain Current.

TYPICAL y PARAMETER CHARACTERISTICS

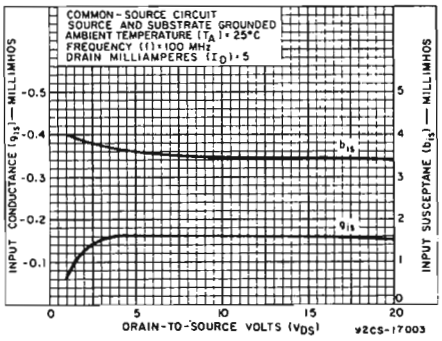


Fig. 6 - Input Admittance vs. Drain-to-Source Voltage

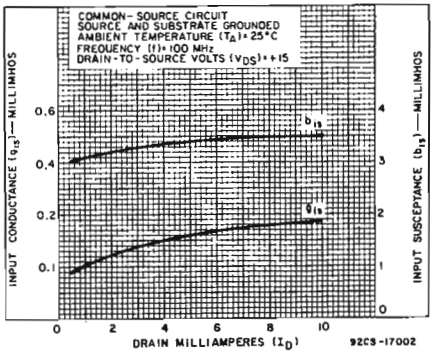


Fig. 7 - Input Admittance vs. Drain Current

TYPICAL y PARAMETER CHARACTERISTICS (Cont'd)

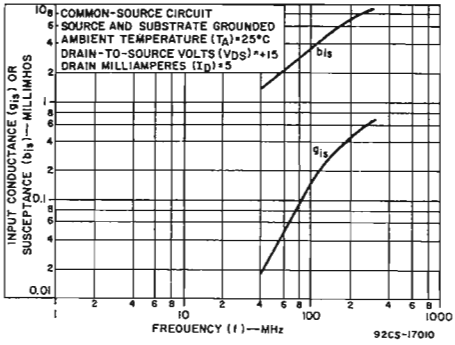


Fig. 8 - Input Admittance vs. Frequency

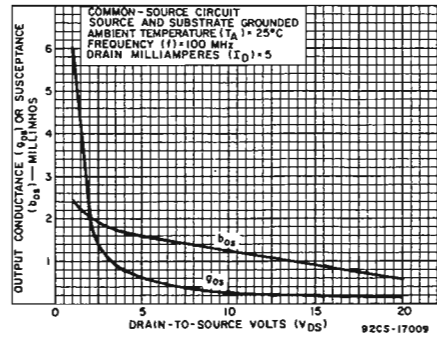


Fig. 9 - Output Admittance vs. Drain-to-Source Voltage

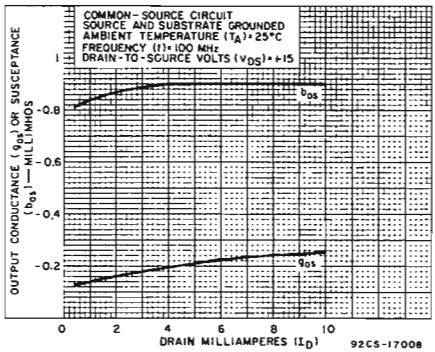


Fig. 10 - Output Admittance vs. Drain Current

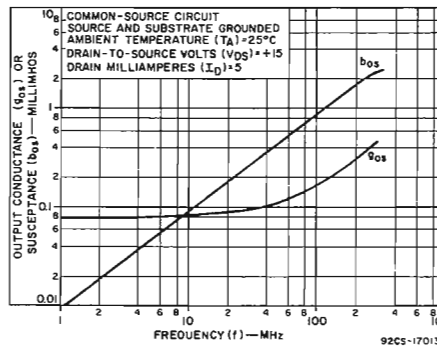


Fig. 11 - Output Admittance vs. Frequency

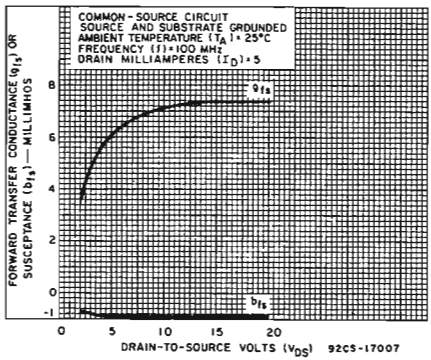


Fig. 12 - Forward Transadmittance vs. Drain-to-Source Voltage

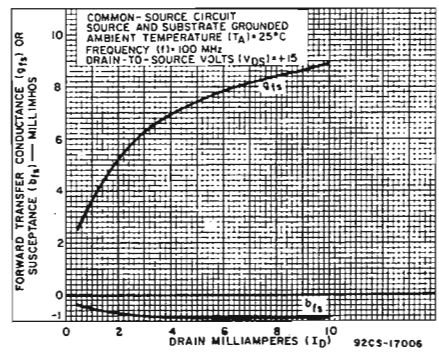


Fig. 13 - Forward Transadmittance vs. Drain Current

TYPICAL y PARAMETER CHARACTERISTICS

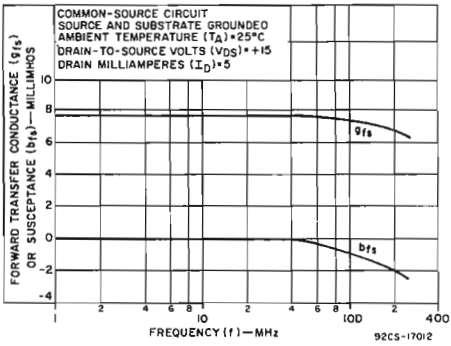


Fig. 14 - Forward Transadmittance vs. Frequency

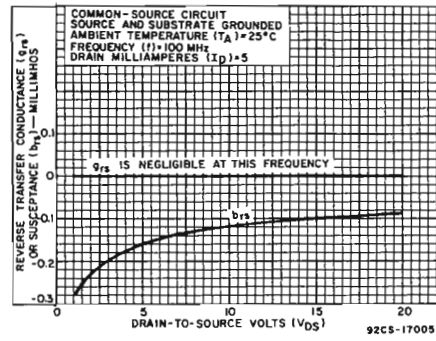


Fig. 15 - Reverse Transadmittance vs. Drain-to-Source Voltage

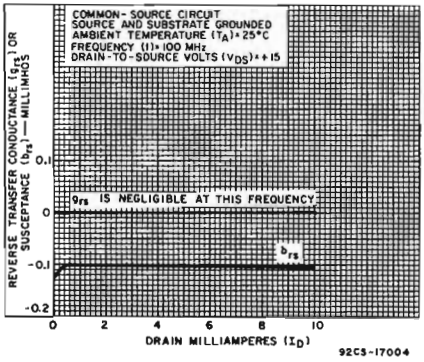


Fig. 16 - Reverse Transadmittance vs. Drain Current

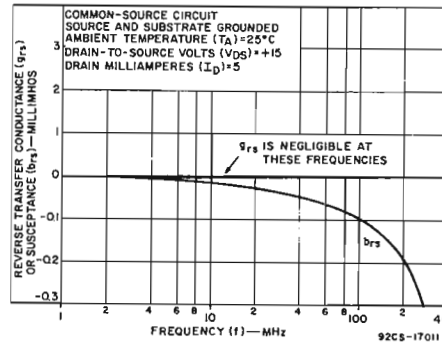
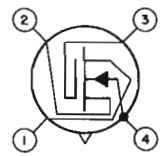


Fig. 17 - Reverse Transadmittance vs. Frequency

TERMINAL DIAGRAM



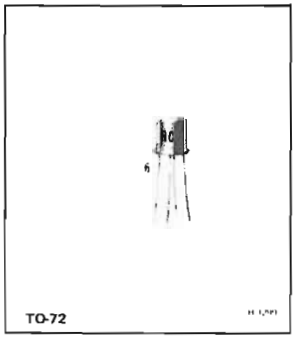
LEAD 1 - DRAIN
LEAD 2 - SOURCE
LEAD 3 - INSULATED GATE
LEAD 4 - BULK (SUBSTRATE) AND CASE

RCA
Solid State
Division

MOS Field-Effect Transistors

N-Channel Depletion Type

3N152



Silicon MOS Transistor

For Low-Noise RF Applications in Military & Industrial VHF Communications Equipment Operating up to 250 MHz

RCA-3N152 is an N-channel depletion-type silicon insulated gate field-effect transistor utilizing the MOS■ construction. It is intended primarily for VHF amplifier applications up to 250 MHz in military and industrial equipment.

Because of its improved transfer characteristic and exceptionally wide dynamic range, the 3N152 with the substrate in the reversed bias mode can provide substantially better cross-modulation performance in linear amplifier applications than conventional bipolar transistors. The insulated gate with its extremely low reverse (leakage) current eliminates the problem of diode-current loading of the input circuit under strong input conditions, which is common to junction-type FET's. These features in addition to low feedback capacitance permit the design of circuits providing superior high-frequency operation and high gain without neutralization. The 3N152 utilizes full-gate construction and is hermetically sealed in a JEDEC TO-72 metal package.

■ Metal-Oxide-Semiconductor.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

* DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 max.	V
* DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
* GATE-TO-SOURCE VOLTAGE, V_{GS}:		
* CONTINUOUS (dc)	+1, -8 max.	V
* PEAK ac	±15 max.	V
* DRAIN CURRENT, I_D	50 max.	mA
TRANSISTOR DISSIPATION:		
At ambient temperatures up to 25°C	330 max.	mW
At ambient temperatures above 25°C	derate at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
* LEAD TEMPERATURE (During Soldering):		
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265 max.	°C

* In accordance with Jedec Registration Data Format JS-9 RDF 11-B.

Features

- Low gate leakage current — I_{GSS} = 0.1 pA typ.
- Low feedback capacitance — C_{rss} = 0.25 pF typ.
- High forward transconductance — g_{fs} = 7500 μmho typ.
- High vhf power gain — G_{PS} = 16 dB typ. at 200 MHz
- Low vhf noise figure — NF = 2.5 dB typ. at 200 MHz
- Exceptionally good cross-modulation characteristics

Performance

- Large dynamic range
- Greatly reduced spurious responses
- Permits use of vacuum-tube biasing techniques
- Excellent thermal stability
- Superior cross-modulation performance and greater dynamic range than bipolar transistors

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$

Measured with Substrate Connected to Source Unless Otherwise Specified

	CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS 3N152 Min.	Typ.	Max.	UNITS
*	Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8V, T_A = 25°C	-	0.0001	1	nA
			V_{DS} = 0, V_{GS} = -8 V, T_A = 125°C	-	-	200	nA
*	Zero-Bias Drain Current	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	5	15	30	mA
	Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{DS} = 20 V, V_{GS} = -8V	-	-	50	µA
*	Gate-to-Source-Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 50 µA	-0.5	-3	-8	V
*	Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7500	12,000	µmho
	Drain-to-Source Channel Resistance	$r_{DS(on)}$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	-	200	-	Ω
*	Small-Signal Short-Circuit Reverse Transfer Capacitance▲	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.15	0.25	0.35	pF
	Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	5.5	7	pF
	Input Admittance	Y_{is}	Common Source Configuration f = 200 MHz	-	0.4 + J7.3	-	mmho
	Forward Transfer Admittance	Y_{fs}	V_{DS} = 15 V,	-	7-J2	-	mmho
	Output Admittance	Y_{os}	I_D = 5 mA	-	0.28 + J1.8	-	mmho
	Power Gain Maximum Available Gain	MAG		-	21	-	dB
	Insertion Power Gain (Fixed Neutralization) See Fig.1	G_{PS}	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	14.5	16	-	dB
	Noise Figure (See Figs. 1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	2.5	3.5	dB

▲ Three-Terminal Measurement. Source Returned to Guard Terminal.

* In accordance with JEDEC Registration Data Format JS-9 RDF-11B.

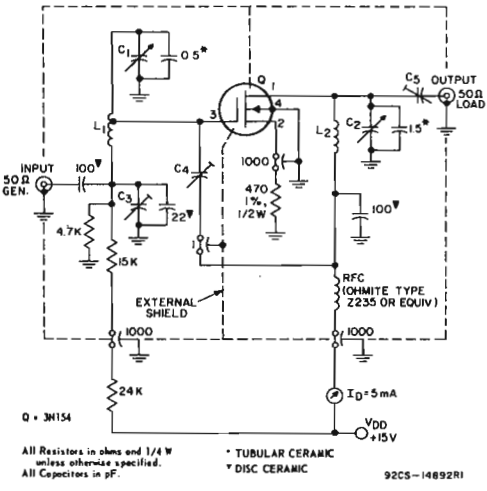


Fig. 1 - Test circuit used to measure 200-MHz maximum usable power gain and noise Figure.

C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap

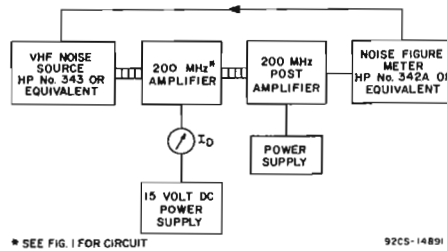


Fig. 2 - Noise figure measurement setup.

TEST SETUP AND TYPICAL CHARACTERISTICS

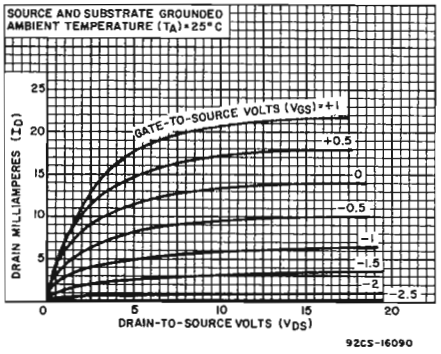


Fig. 3 - Drain Current vs Drain-to-Source Voltage.

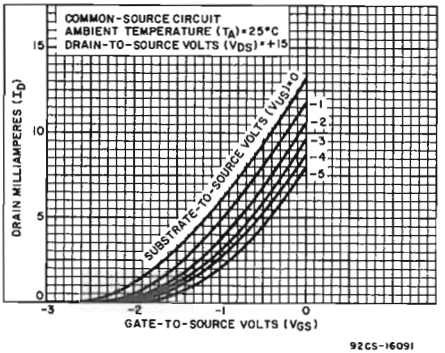


Fig. 4 - Drain Current vs Gate-to-Source Voltage .

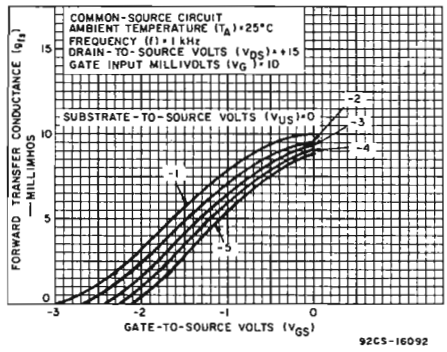


Fig. 5 - Forward Transconductance vs Gate Bias Voltage.

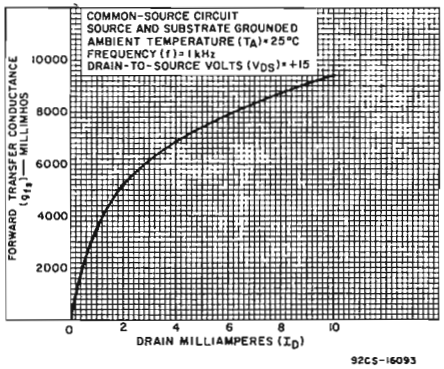


Fig. 6 - Forward Transconductance vs Drain Current.

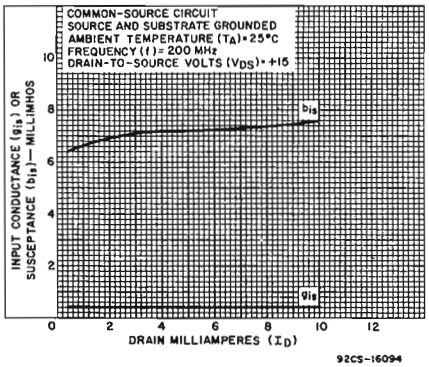


Fig. 7 - Input Admittance vs Drain Current.

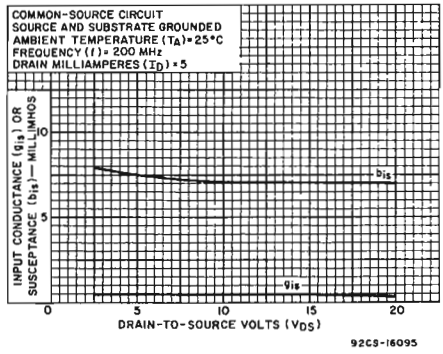


***Fig. 8** - Input Admittance vs Drain-to-Source Voltage.*

TYPICAL 200 MHz COMMON-SOURCE ADMITTANCE (Y) COMPONENTS

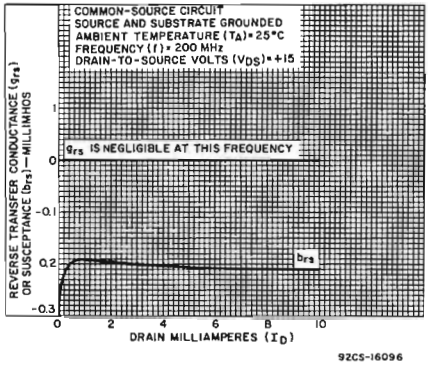


Fig. 9 - Reverse Transadmittance vs Drain Current.

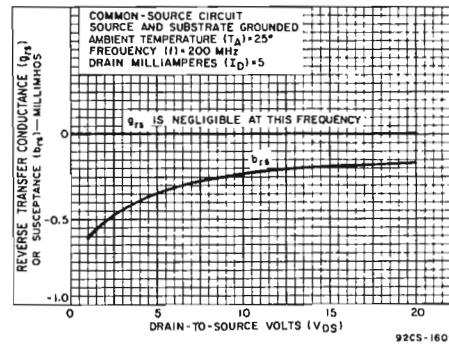


Fig. 10 - Reverse Transadmittance vs Drain-to-Source Voltage.

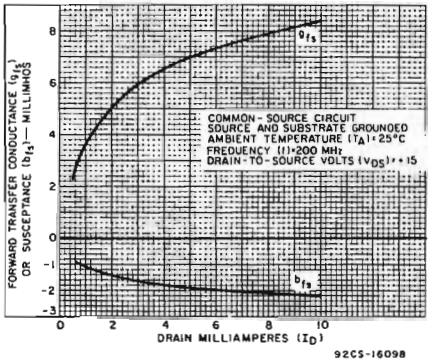


Fig. 11 - Forward Transadmittance vs Drain Current.

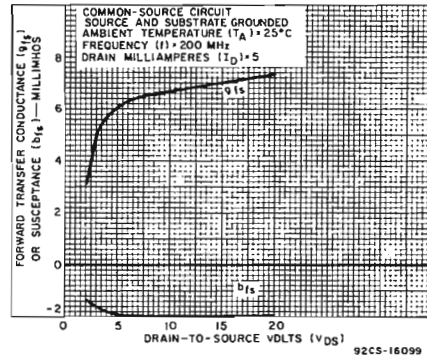


Fig. 12 - Forward Transadmittance vs Drain-to-Source Voltage.

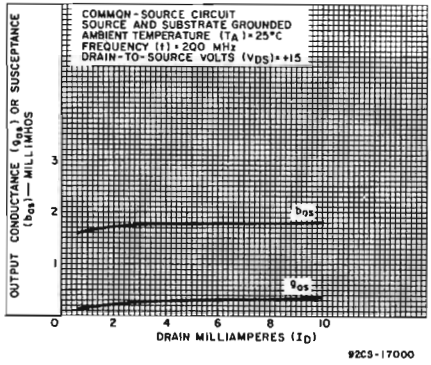


Fig. 13 - Output Admittance vs Drain Current.

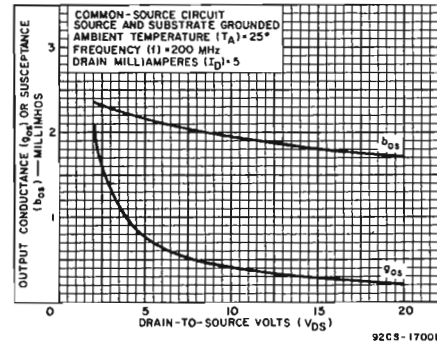


Fig. 14 - Output Admittance vs Drain-to-Source Voltage.

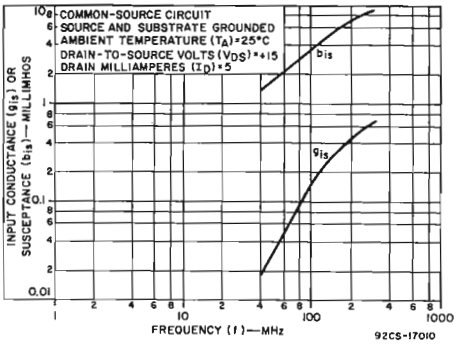


Fig. 15 - Input Admittance vs Frequency.

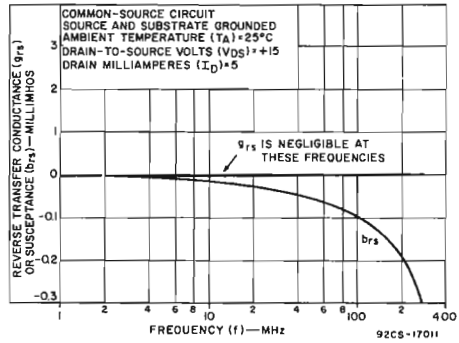


Fig. 16 - Reverse Transadmittance vs Frequency.

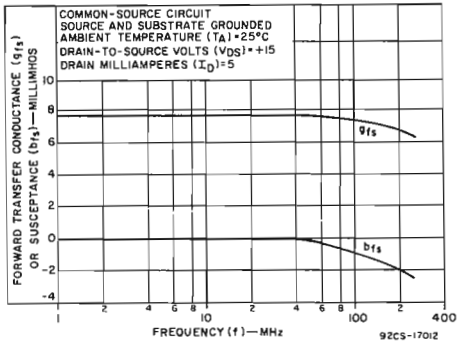


Fig. 17 - Forward Transadmittance vs Frequency.

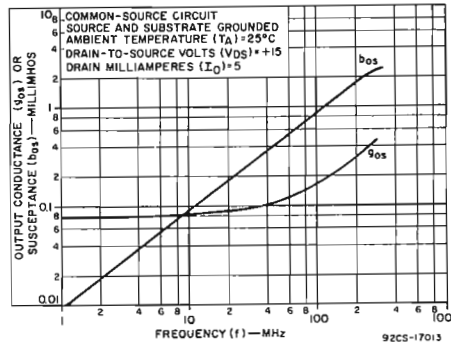


Fig. 18 - Output Admittance vs Frequency.

RCA Solid State Division

MOS Field-Effect Transistors

N-Channel Depletion Type

3N153

RCA 3N153 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is intended primarily for critical chopper and multiplex applications up to 60 MHz.

The insulated gate provides a very high value of input resistance (10^{10} ohms typ) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N153 also features extremely low feedback capacitance (0.34 pF typ) and virtually zero inherent offset voltage.

This transistor features a Terminal Arrangement in which the gate and source connections are interchanged to provide maximum isolation between the output (drain) and the input (gate) terminals. Although this new basing configuration does not appreciably change the measured device feedback capacitance, it permits the use of external inter-terminal shields to reduce the feedback due to external capacitances, particularly on printed circuit boards. This feature makes it possible to minimize feedthrough capacitance.

The 3N153 is hermetically sealed in the JEDEC TO-72 package and features a gate metallization that covers the entire source-to-drain channel.

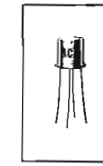
* Metal-Oxide-Semiconductor

Maximum Ratings, *Absolute-Maximum Values:*

(Substrate connected to source unless otherwise specified)

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+20, -0.3 max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+20, -0.3 max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	+6, -8 max.	V
PEAK GATE-TO-SOURCE VOLTAGE, v_{GS}	±14 max.	V
DRAIN CURRENT, I_D (Pulse duration 20 ms, duty factor ≤ 0.10)	50 max.	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures from -65 to +25°C	400 max.	mW
above 25°C	derate linearly at 2.67	mW/°C
AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distance ≥ 1/32" to seating surface for 10 seconds max.	265 max.	°C

SILICON INSULATED GATE FIELD-EFFECT TRANSISTOR

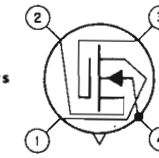


JEDEC TO-72

APPLICATIONS

- Choppers
- Multiplexers
- Servo Amplifiers
- Computer Operational Amplifiers
- Sampling Circuits
- Electrometer Amplifiers

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

FEATURES

- excellent thermal stability
- virtually zero inherent offset voltage
- low leakage current: 50 pA max.
- low "on" resistance — $r_{DS(on)}$ = 200 Ω typ.
- high "off" resistance — $R_{DS(off)}$ = 10^{10} Ω typ.
- low feedback capacitance — C_{rss} = 0.34 pF typ.
- low input capacitance — C_{iss} = 6 pF typ.

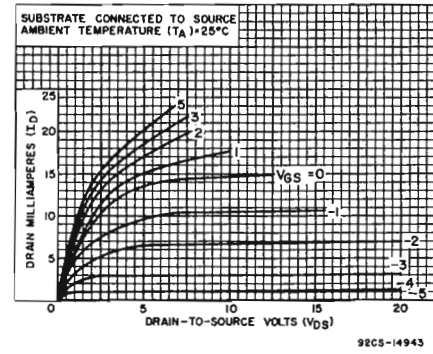


Fig.1 - Drain current vs. drain-to-source voltage.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, Unless Otherwise Specified. Substrate Connected to Source.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Type 3N153			UNITS
			Min.	Typ.	Max.	
Gate-Leakage Current	I_{GSS}	V_{GS} = +6,-8V; V_{DS} = 0V; T_A = 25°C V_{GS} = +6,-8V; V_{DS} = 0V; T_A = 125°C	- -	0.1 -	50 1	pA nA
Static Drain-to-Source "ON" Resistance	$r_{DS(on)}$	V_{GS} = 0V, V_{DS} = 0V	-	200	300	Ω
Drain-to-Source "OFF" Resistance	$R_{DS(off)}$	V_{GS} = -8V, V_{DS} = +1V	10^9	10^{10}	-	Ω
Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{GS} = -8V, V_{DS} = +1V, T_A = 25°C V_{GS} = -8V, V_{DS} = +1V, T_A = 125°C	- -	0.1 0.1	1 1	nA μA
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	V_{GS} = -8V, V_{DS} = 0V, f = 1 MHz V_{DS} = 15V, I_D = 5 mA, f = 1 MHz	- -	0.34 0.25	0.5 0.38	pF pF
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	V_{GS} = -8V, V_{DS} = 0V, f = 1 MHz	-	6	8	pF
Small-Signal, Drain-to-Source Capacitance	C_{ds}	V_{DS} = 0V, V_{GS} = -8V, f = 1 MHz	-	-	3	pF
Zero-Gate-Bias Forward Transconductance	g_{fs}	V_{GS} = 0V, V_{DS} = +15V	-	10,000	-	μmho
Offset Voltage	V_o	V_{GS} = +6,-8V; V_{DS} = 0V	-	0*	-	V

* In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No.107-1.0.1, or equivalent.

OPERATING CONSIDERATIONS

The flexible leads of the 3N153 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields.

This device should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the device.

TYPICAL CHARACTERISTICS

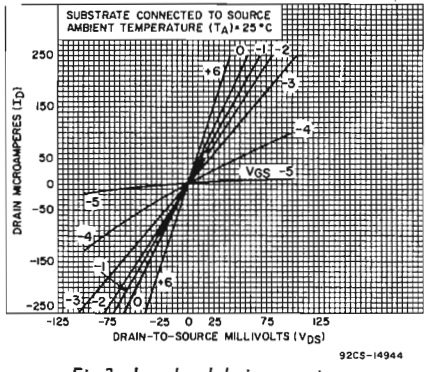


Fig.2 - Low-level drain current vs. drain-to-source voltage.

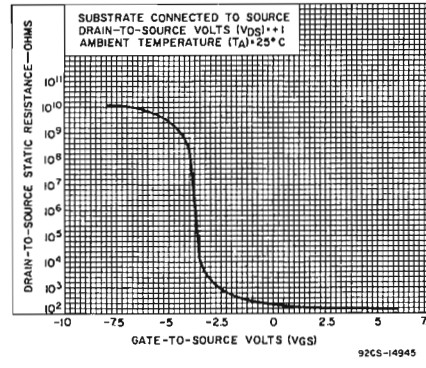


Fig.3 - Drain-to-source static resistance vs. gate-to-source voltage.

RCA
Solid State Division

MOS Field-Effect Transistor

N-Channel Depletion Type

3N154

TO-72

Silicon MOS Transistor

For Critical Amplifier Applications in Military & Industrial VHF Communications Equipment Operating up to 250 MHz

Device Feature:

- Closely controlled I_{DSS} — 10 to 25 mA
- Low gate leakage current — I_{GSS} = 0.1 pA typ.
- Low feedback capacitance — C_{rss} = 0.25 pF typ.
- High forward transconductance — g_{fs} = 7500 μmho typ.
- High vhf power gain — G_{PS} = 16 dB typ. at 200 MHz
- Low vhf noise figure — NF = 3.5 dB typ. at 200 MHz
- Exceptionally good cross-modulation characteristics

RCA 3N154 is an n-channel depletion-type silicon insulated-gate field-effect transistor utilizing the MOS■ construction. It is intended primarily for vhf amplifier applications up to 250 MHz in military and industrial equipment.

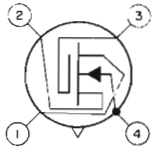
Because of its improved transfer characteristic and exceptionally wide dynamic range, the 3N154 can provide substantially better crossmodulation performance in linear amplifier applications than conventional bipolar transistors. The extremely low gate leakage current eliminates diode-current loading of the input circuit under strong signal conditions, a problem which is common to junction-type FET's. These features, in addition to low feedback capacitance, permit the design of circuits providing superior high-frequency operation and high gain without neutralization. The 3N154 utilizes full-gate construction and is hermetically sealed in a JEDEC TO-72 metal package.

■ Metal-Oxide-Semiconductor

Performance Features

- Large dynamic range
- Greatly reduced spurious responses
- Permits use of vacuum-tube biasing techniques
- Excellent thermal stability
- Superior cross-modulation performance and greater dynamic range than bipolar transistors

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25^oC$:

*DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	V
*DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
*GATE-TO-SOURCE VOLTAGE, V_{GS}:		
* CONTINUOUS (dc)	+1, -8	V
* PEAK ac	±15	V
*DRAIN CURRENT, I_D▲	50	mA
*TRANSISTOR DISSIPATION:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate at 2.2	mW/°C
*AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265	°C

In accordance with JEDEC Registration Data Format JS9-RDF-11B

▲ Pulsed:
Pulse duration ≤ 20 ms
Duty factor ≤ 0.15

ELECTRICAL CHARACTERISTICS: (At T_A = 25° C)

Measured with Substrate Connected to Source Unless Otherwise Specified.

	CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS 3N154 Min.	Typ.	Max.	UNITS
*	Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8 V, T_A = 25° C	-	0.0001	0.05	nA
			V_{DS} = 0, V_{GS} = -8 V, T_A = 125° C	-	-	5	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 25° C	-	0.0001	0.05	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 125° C	-	-	5	nA
*	Zero-Bias Drain Current	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	10	15	25	mA
	Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{DS} = 20 V, V_{GS} = -8 V	-	-	50	μA
*	Gate-to-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 50 μA	-0.5	-3	-8	V
	Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7500	12,000	μmho
	Drain-to-Source Channel Resistance	$r_{DS(on)}$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	-	200	-	Ω
*	Small-Signal Short-Circuit Reverse Transfer Capacitance	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.15	0.25	0.35	pF
	Small-Signal Short-Circuit Input Capacitance ▲	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	5.5	7	pF
	Input Admittance	Y_{is}	Common Source Configuration f = 200 MHz, V_{DS} = 15 V, I_D = 5 mA	-	0.4 + J7.3	-	mmho
	Forward Transfer Admittance	Y_{fs}		-	7 − J2	-	mmho
	Output Admittance	Y_{os}		-	0.28 + J1.8	-	mmho
	Maximum Available Power Gain	MAG	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	21	-	dB
*	Insertion Power Gain (Fixed Neutralization) (see Fig. 1)	G_{PS}		13.5	16	-	dB
*	Noise Figure (see Figs.1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	3.5	5	dB

* In Accordance with JEDEC Registration Data Format JS-9 RDF-11B

▲ Three-Terminal Measurement: Source Returned to Guard Terminal

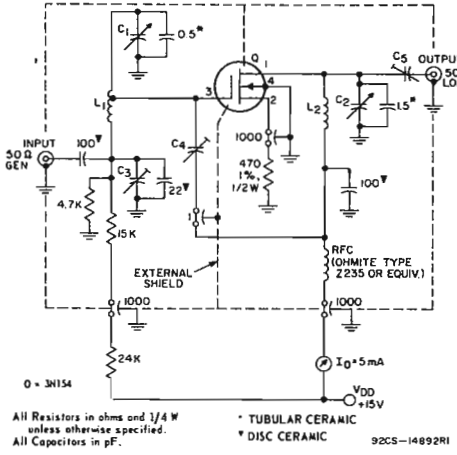


Fig. 1 - Test circuit used to measure 200-MHz maximum usable power gain and noise figure

C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

Q = 3N154

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

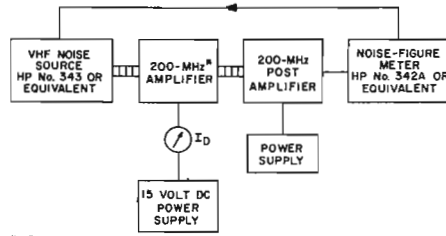


Fig. 2 - Noise figure measurement setup

TYPICAL CHARACTERISTICS

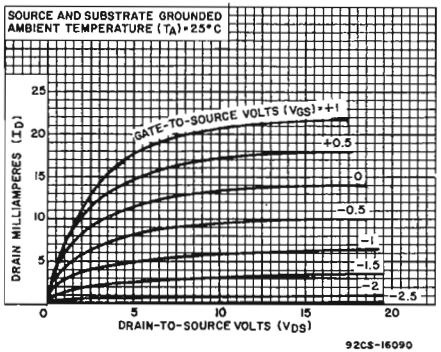


Fig. 3 - Drain current vs drain-to-source voltage

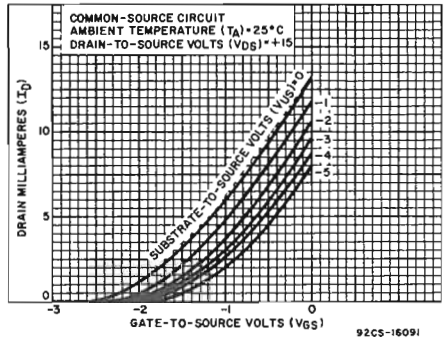


Fig. 4 - Drain current vs gate-to-source voltage

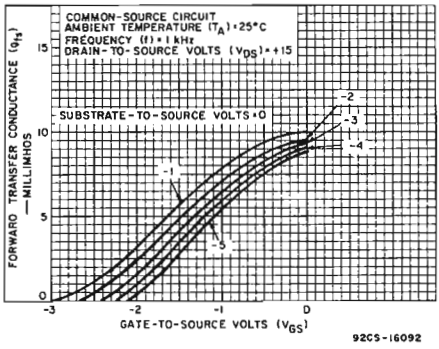


Fig. 5 - Forward transconductance vs gate-to-source voltage

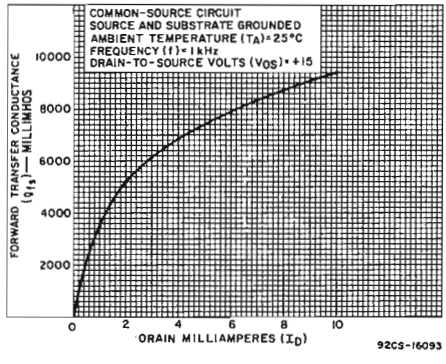


Fig. 6 - Forward transconductance vs drain current

TYPICAL 200 MHz COMMON-SOURCE ADMITTANCE (Y) COMPONENTS

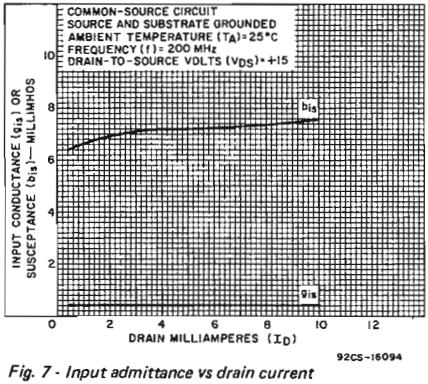


Fig. 7 - Input admittance vs drain current

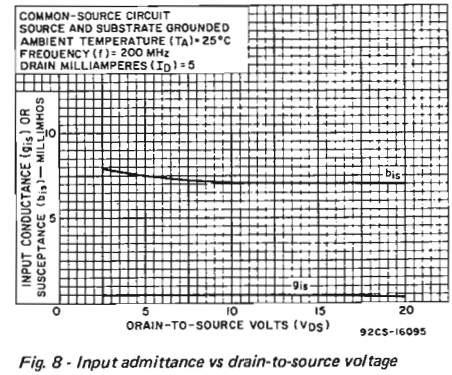


Fig. 8 - Input admittance vs drain-to-source voltage

TYPICAL 200 MHz COMMON-SOURCE ADMITTANCE (Y) COMPONENTS

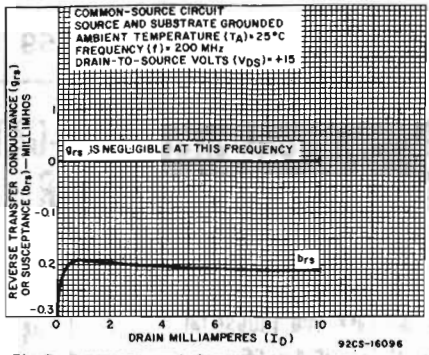


Fig. 9 - Reverse transadmittance vs drain current

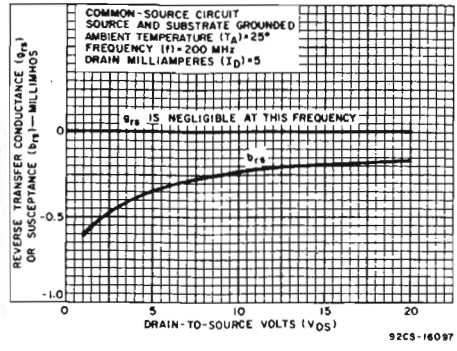


Fig. 10 - Reverse transadmittance vs drain-to-source voltage

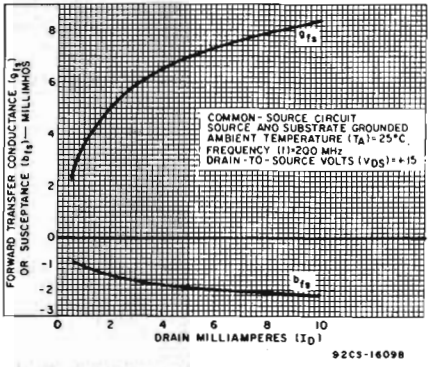


Fig. 11 - Forward transadmittance vs drain current

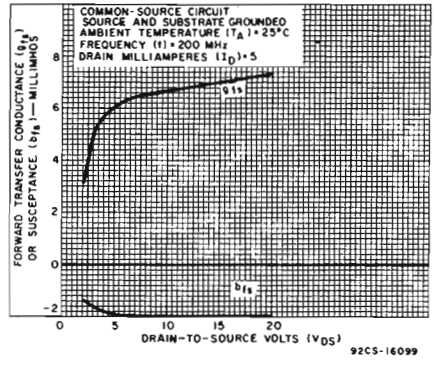


Fig. 12 - Forward transadmittance vs drain-to-source- voltage

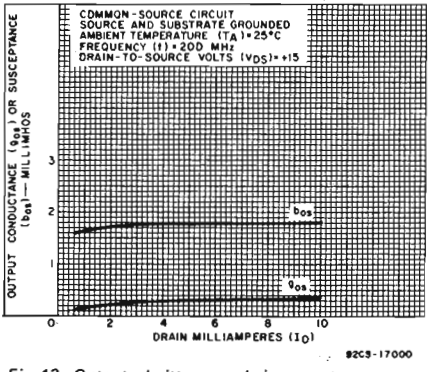


Fig. 13 - Output admittance vs drain current

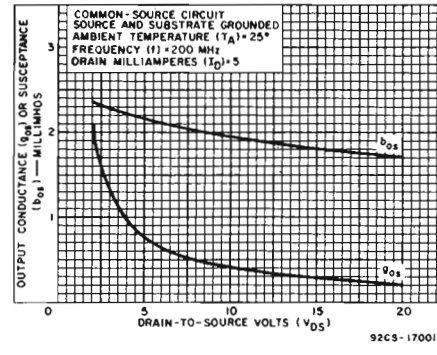


Fig. 14 - Output admittance vs drain-to-source voltage

RCA
Solid State Division

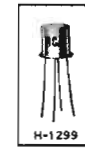
MOS Field-Effect Transistors

N-Channel Depletion Type

3N159

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTOR N-Channel Depletion Type

For Military and Industrial Low-Noise RF-Amplifier Applications Up to 300 MHz



TO-72

The 3N159 is an n-channel silicon, depletion type, dual insulated-gate, field-effect transistor utilizing the MOS** construction. It has exceptional characteristics for rf-amplifier applications at frequencies up to 300 MHz. This transistor features a series arrangement of two separate channels, each channel having an independent control gate.

Type 3N159 has an exceptionally low-noise figure, which makes this type particularly suitable for critical vhf applications. When used in a common-source configuration in which gate No.2 is ac grounded, this device reduces oscillator feedthrough to the antenna thereby minimizing oscillator radiation.

The 3N159 is hermetically sealed in the metal JEDEC TO-72 package.

** Metal-Oxide-Semiconductor.

Maximum Ratings, *Absolute-Maximum Values:*
at T_A = 25°C

DRAIN-TO-SOURCE VOLTAGE, V_{DS} . . . . . 0 to +20 V

GATE-No.1-TO-SOURCE VOLTAGE, V_{G1S}:
- Continuous (dc) . . . . . -8 to +1 V
- Peak ac . . . . . -8 to +20 V

GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:
- Continuous (dc) . . . . . -8 to 40% of V_{DS} V
- Peak ac . . . . . -8 to +20 V

DRAIN-TO-GATE VOLTAGE:
V_{DG1} or V_{DG2} . . . . . +20 V

DRAIN CURRENT, I_D
- Pulsed: Pulse duration ≤ 20 ms, duty factor ≤ 0.15 . . . . . 50 mA

TRANSISTOR DISSIPATION, P_T:
- At ambient temperatures up to 25°C . . . . . 400 mW
- above 25°C . . . . . derate linearly at 2.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Storage and Operating . . . . . -65 to +175 °C

LEAD TEMPERATURE (During soldering):
- At distances ≥ 1/32 inch from seating surface for 10 seconds max. . . . . 265 °C

APPLICATIONS

- RF amplifier in military and industrial communications equipment
- aircraft, marine and vehicular receivers
- CATV and MATV equipment
- telemetry and multiplex equipment

PERFORMANCE FEATURES

- wide dynamic range permits large-signal handling before overload
- dual-gate permits simplified agc circuitry
- virtually no agc power required
- greatly reduces spurious responses in FM receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability
- superior crass-modulatian performance and greater dynamic range than bipolar or single-gate field-effect transistors

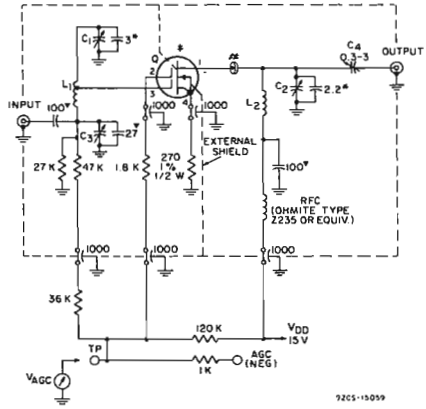
DEVICE FEATURES

- low gate leakage currents — — I_{G1SS} & I_{G2SS} = 1 nA max.
- high forward transconductance — — g_{fs} = 7000 μmho min.
- high unneutralized RF power gain — — G_{ps} = 16 dB min. at 200 MHz
- low vhf noise figure — — NF = 3.5 dB max. at 200 MHz

ELECTRICAL CHARACTERISTICS, at T_A = 25°C unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS 3N159			UNITS
			Min.	Typ.	Max.	
Gate-No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +16V, I_D = 200 μA V_{G2S} = +4V	-	-2	-4	V
Gate-No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +16V, I_D = 200 μA V_{G1S} = 0	-	-2	-4	V
Gate-No.1-Leakage Current	I_{G1SS}	V_{G1S} = -20V, V_{G2S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G1S} = +1V, V_{G2S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G1S} = -20V, V_{G2S} = 0 V_{DS} = 0, T_A = 125°C	-	-	0.2	μA
Gate-No.2-Leakage Current	I_{G2SS}	V_{G2S} = -20V, V_{G1S} = 0 V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G2S} = +1, V_{DS} = 0 V_{G1S} = 0, T_A = 25°C	-	-	1	nA
		V_{G2S} = -20V, V_{G1S} = 0 V_{DS} = 0, T_A = 125°C	-	-	0.2	μA
Zero-Bias Drain Current	I_{DSS}*	V_{DD} = +14V, V_{G1S} = 0 V_{G2S} = +4V	5	18	30	mA
Forward Transconductance (Gate-No.1-to-Drain)	g_{fs}	V_{DD} = +14V, I_D = 10 mA V_{G2S} = +4V, f = 1 kHz	7000	10,000	18,000	μmho
Cutoff Forward Transconductance (Gate-No.1-to-Drain)	$g_{fs(off)}$	V_{DD} = +14V, V_{G1S} = -0.5V V_{G2S} = -2V, f = 1 kHz	-	-	100	μmho
Small-Signal, Short-Circuit Input Capacitance▲	C_{iss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	3	5.5	7	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No.1)♦	C_{rss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	0.01	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 MHz	-	2.2	-	pF
Maximum Usable Power Gain (See Fig.1 for Measurement Circuit)	MUG	V_{DD} = +15V, R_S = 270Ω R_G = 50Ω, f = 200 MHz	16	18	22	dB
Measured Noise Figure (See Fig.1 for Measurement Circuit)	NF	V_{DD} = +15V, R_S = 270Ω f = 200 MHz, R_G = 50Ω	-	2.5	3.5	dB

* Pulse Test: Pulse duration ≤ 20 ms, duty factor ≤ 0.15.
▲ Capacitance between Gate No.1 and all other terminals.
♦ Three-Terminal Measurement with Gate No.2 and Source Returned to Guard Terminal.



* Tubular ceramic
▼ Disc ceramic
\# Ferrite bead (1/2 used); Indiana General No. H 1742C-(A-147) or F1157-1-H or equivalent.
‡ VHF plug in socket Jettron CD72-148 and CD72149 (part No.7977-1) or equivalent.

C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - 200-MHz power gain and noise-figure test circuit for type 3N159.

TYPICAL CHARACTERISTICS

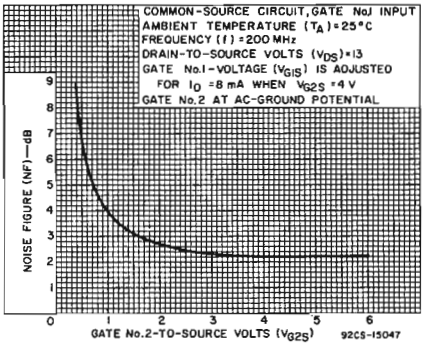


Fig.2 - Noise figure vs gate No.2-to-source voltage.

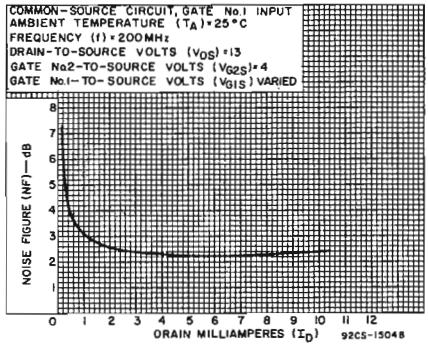


Fig.3 - Noise figure vs drain current.

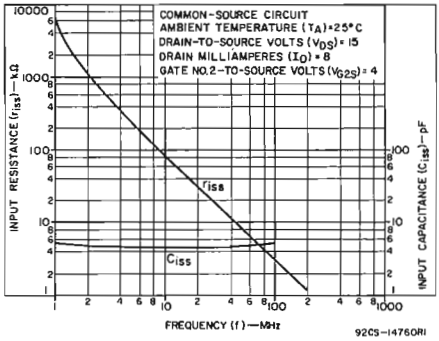


Fig.4 - Input resistance and capacitance vs frequency.

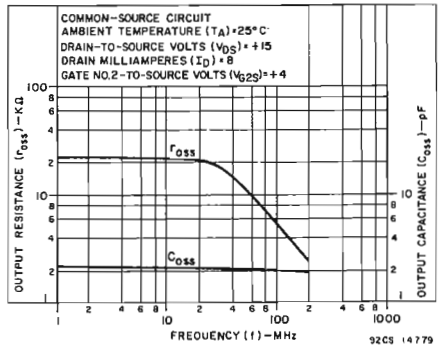


Fig.5 - Output resistance and capacitance vs frequency.

TYPICAL SMALL-SIGNAL y PARAMETERS at 200 MHz

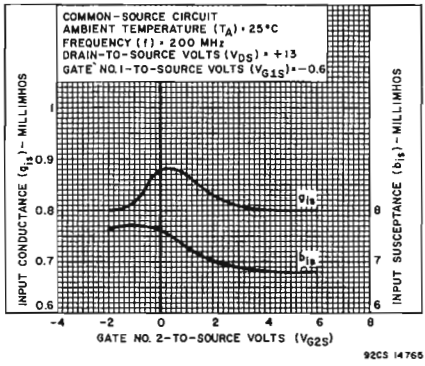


Fig.6 - Input conductance and susceptance vs gate No.2-to-source voltage.

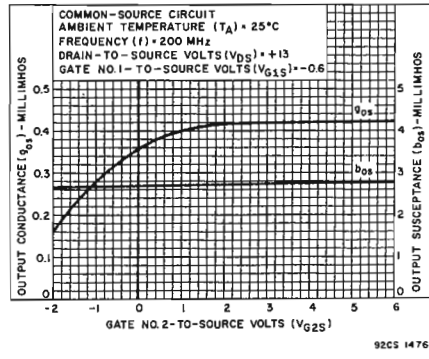


Fig.7 - Output conductance and susceptance vs gate No.2-to-source voltage.

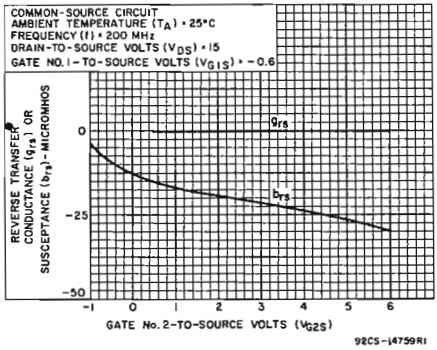


Fig.8 - Reverse transfer conductance or susceptance vs gate No.2-to-source voltage.

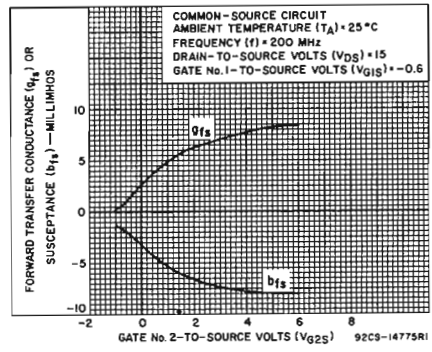


Fig.9 - Forward transfer conductance or susceptance vs gate No.2-to-source voltage.

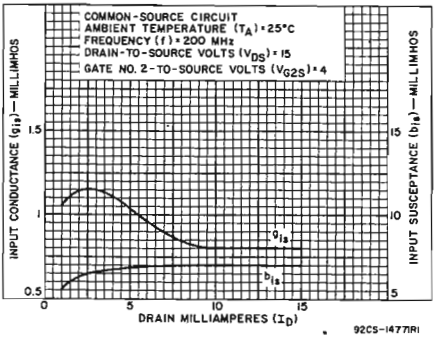


Fig.10 - Input conductance and susceptance vs drain milliamperes.

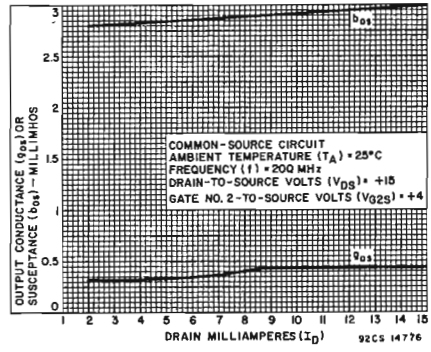


Fig.11 - Output conductance and susceptance vs drain milliamperes.

TYPICAL SMALL-SIGNAL y PARAMETERS at 200 MHz

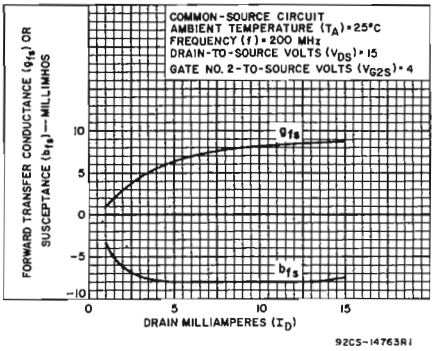


Fig.12 - Forword transfer conductance and susceptance vs drain current.

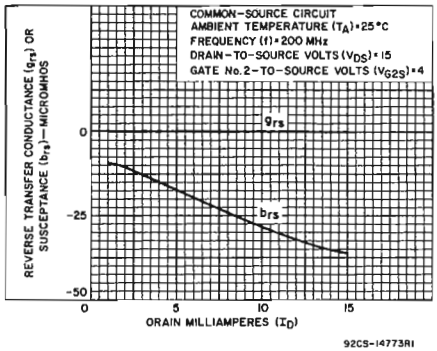


Fig.13 - Reverse tronsfer conductance ond susceptonce vs drain current.

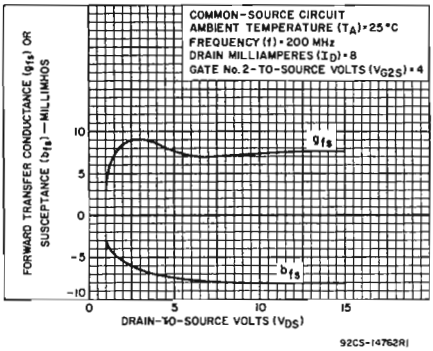


Fig.14 - Forward transfer conductonce and susceptance vs drain-to-source voltage.

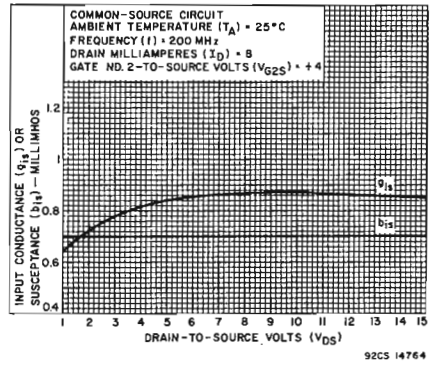


Fig.15 - Input conductance and susceptance vs drain-to-saurce voltage.

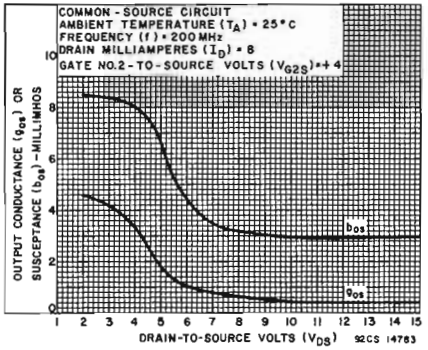


Fig.16 - Output conductance and susceptance vs drain-ta-source voltage.

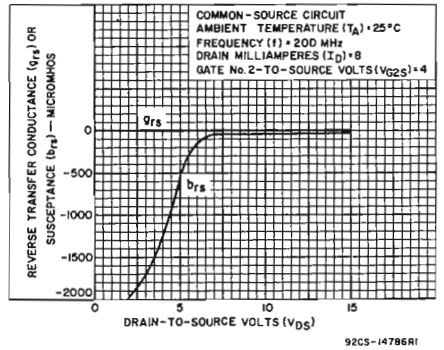


Fig.17 - Reverse transfer conductance ond susceptance vs drain-to-source voltage.

TYPICAL CHARACTERISTICS

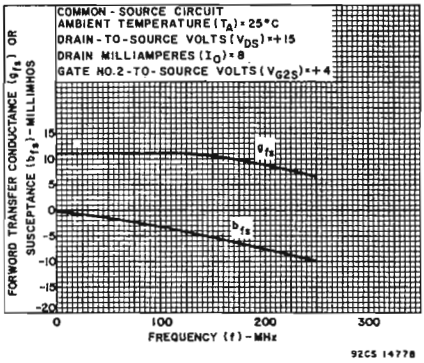


Fig.18 - Forword transfer conductance and susceptance vs frequency.

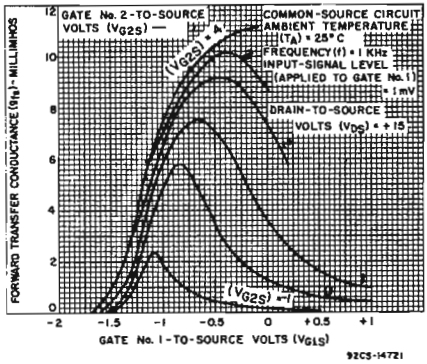


Fig.19 - Forward transfer conductance vs gate No.1-to-source voltage.

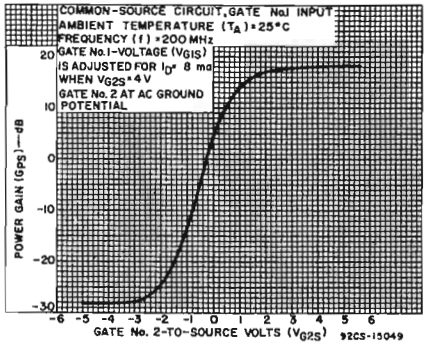
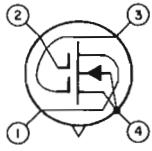


Fig.20 - Power gain vs gate No.2-to-source voltage.

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - GATE No.2
LEAD 3 - GATE No.1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

RCA Solid State Division

MOS Field-Effect Transistors

N-Channel Depletion Types

3N187

JEDEC TO-72

Silicon Dual Insulated-Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits

For Military and Industrial Applications up to 300 MHz

Device Features

- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance — g_{fs} = 12,000 μmho (typ.)
- High unneutralized RF power gain — G_{ps} = 18 dB(typ.) at 200 MHz
- Low VHF noise figure — 3.5 dB(typ.) at 200 MHz

RCA-3N187 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS▲ pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 3N187 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-3N187 make it useful for a wide variety of rf-amplifier applications at frequencies up to 300 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 3N187 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 3N187 is hermetically sealed in the metal JEDEC TO-72 package.

▲ Metal-Oxide-Semiconductor

Applications

- RF amplifier, mixer, and IF amplifier in military, and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

Performance Features

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's
- Wide dynamic range permits large-signal handling before overload
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

Maximum Ratings,

Absolute-Maximum Values, at T_A = 25°C

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No. 1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No. 2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
* DRAIN CURRENT, I_D	50	mA
* TRANSISTOR DISSIPATION P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE: Storage and Operating	-65 to +175	°C
* LEAD TEMPERATURE (During Soldering): At distances ≥ 1/32 inch from seating surface for 10 seconds max.	265	°C

* In accordance with JEDEC Registration Data Format JS-9 RDF-19A

ELECTRICAL CHARACTERISTICS, at T_A = 25° C unless otherwise specified

	CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
*	Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V		−0.5	−2	−4	V
*	Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0		−0.5	−2	−4	V
*	Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V $V_{G2S} = V_{DS}$ = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V $V_{G2S} = V_{DS}$=0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V $V_{G1S} = V_{DS}$=0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V $V_{G1S} = V_{DS}$=0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V V_{G2S} = +4 V V_{G1S} = 0		5	15	30	mA
	Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 kHz		7000	12,000	18,000	μmho
*	Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 MHz		4.0	6.0	8.5	pF
*	Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No. 1)♦	C_{rss}			0.005	0.02	0.03	pF
*	Small-Signal, Short-Circuit Output Capacitanc	C_{oss}			–	2.0	–	pF
	Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 200 MHz		16	18	22	dB
	Maximum Available Power Gain	MAG			–	20	–	dB
	Maximum Usable Power Gain (unneutralized)	MUG			–	20▲	–	dB
	Noise Figure (see Fig. 1)	NF			–	3.5	4.5	dB
*	Magnitude of Forward Transadmittance	$\lvert Y_{fs}\rvert$			–	12,000	–	μmho
*	Phase Angle of Forward Transadmittance	θ			–	−35	–	Degrees
	Magnitude of Reverse Transadmittance	$\lvert Y_{rs}\rvert$			–	25	–	μmho
	Angle of Reverse Transadmittance	θ_{rs}			–	−25	–	Degrees
*	Input Resistance	r_{iss}			–	1.0	–	kΩ
*	Output Resistance	r_{oss}			–	2.8	–	kΩ
*	Gate-to-Source Forward Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSF}$	$I_{G1SSF} = I_{G2SSF}$ = 100 μA		6.5	10	–	V
	Gate No. 2	$V_{(BR)G2SSF}$						
*	Gate-to-Source Reverse Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSR}$	$I_{G1SSR} = I_{G2SSR}$ = -100 μA		−6.5	−10	–	V
	Gate No. 2	$V_{(BR)G2SSR}$						

▲Limited only by practical design considerations.

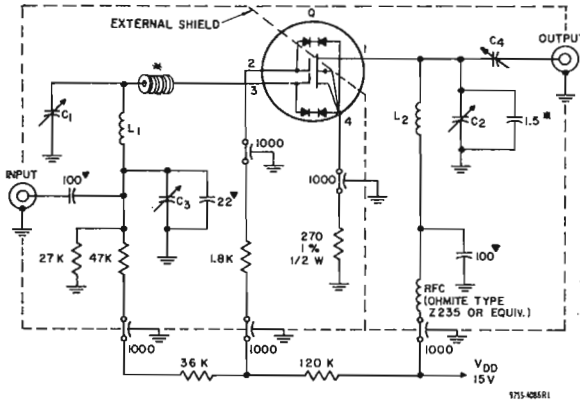
† Capacitance between Gate No. 1 and all other terminals

♦ Three-terminal measurement with Gate No. 2 and Source returned to ground terminal.

* In accordance with JEDEC Registration Data Format JS-9 RDF-19A

OPERATING CONSIDERATIONS

The flexible leads of the 3N187 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.



Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness.

Q = 3N187

▼ Disc ceramic.

* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1: 1.8–8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.

C_2: 1.5–5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.

C_3: 1–10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8–4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.08 in.

L_2: 4½ turns silver-plated 0.02-in thick, 0.085-0.095-in. wide, 5/16-in. ID. Coil ≈ .90 in. long.

Fig. 1 - 200-MHz Power gain and noise-figure test circuit

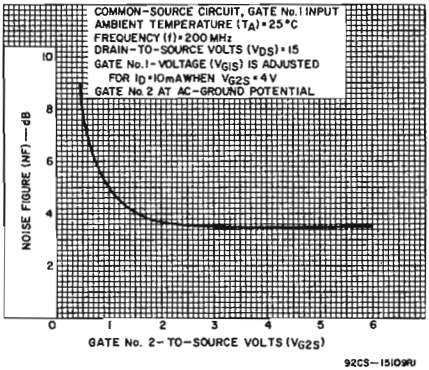


Fig. 2 - NF vs. V_{G2S}

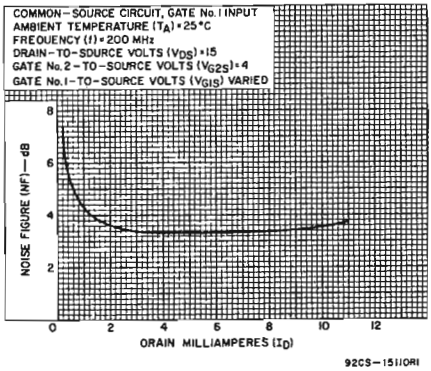


Fig. 3 - NF vs. I_D

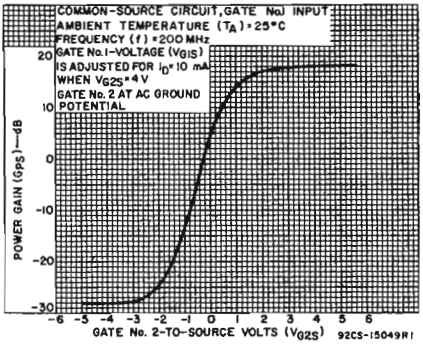


Fig. 4 - G_{PS} vs. V_{G2S}

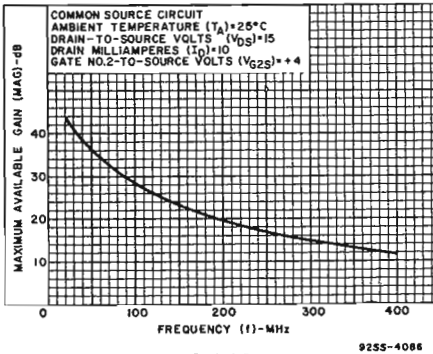


Fig. 5 - MAG. vs. f

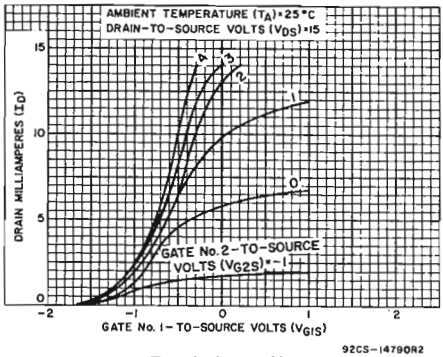


Fig. 6- I_D vs. V_{G1S}

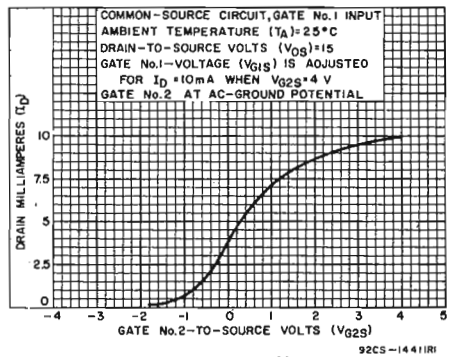


Fig. 7- I_D vs. V_{G2S}

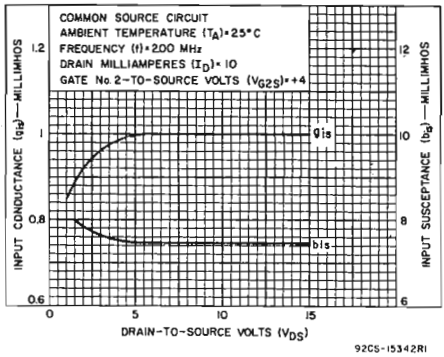


Fig. 8- y_{is} vs. V_{DS}

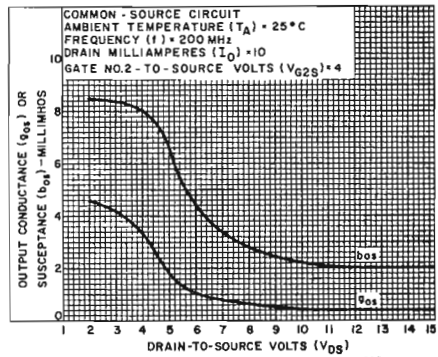


Fig. 9- y_{os} vs. V_{DS}

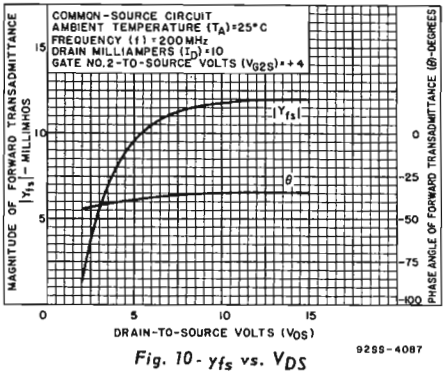


Fig. 10- y_{fs} vs. V_{DS}

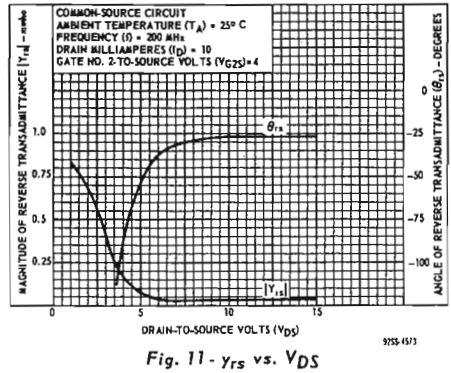


Fig. 11- y_{rs} vs. V_{DS}

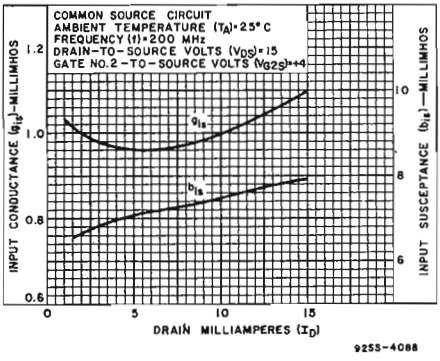


Fig. 12 - y_{is} vs. I_D

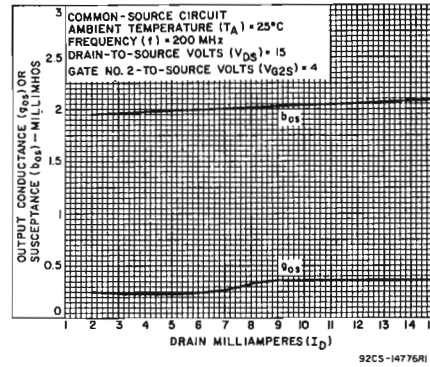


Fig. 13 - y_{os} vs. I_D

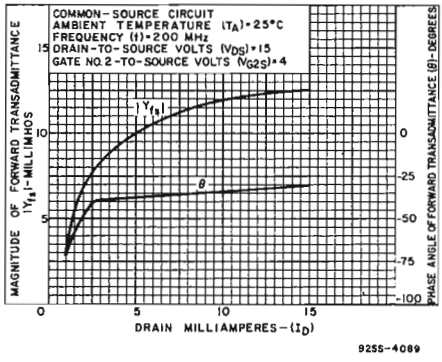


Fig. 14 - y_{fs} vs. I_D

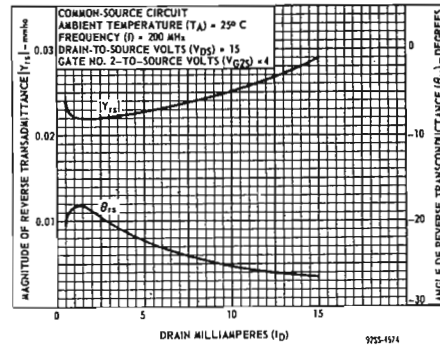


Fig. 15 - y_{rs} vs. I_D

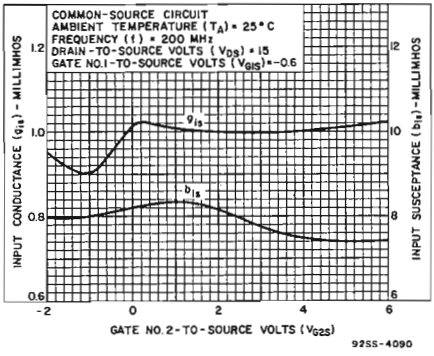


Fig. 16 - y_{is} vs. V_{G2S}

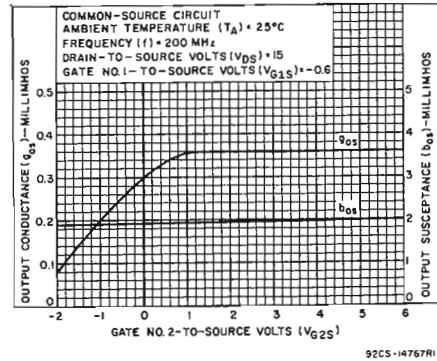


Fig. 17 - y_{os} vs. V_{G2S}

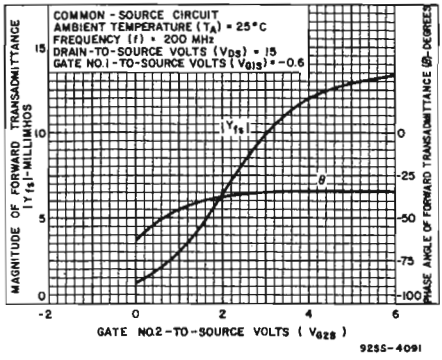


Fig. 18 - y_{fs} vs. V_{G2S}

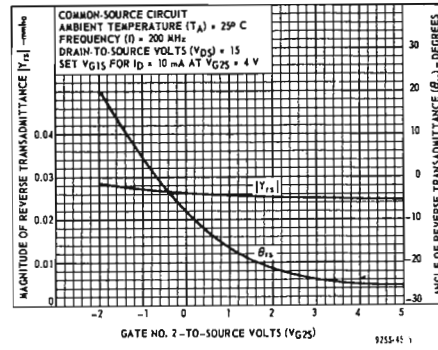


Fig. 19 - y_{rs} vs. V_{G2S}

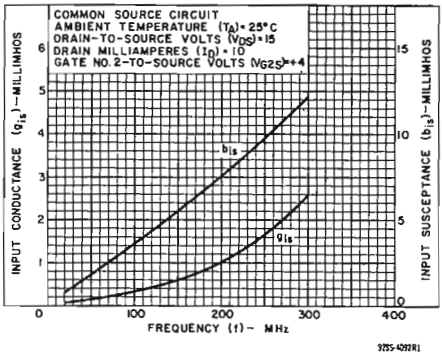


Fig. 20 - y_{is} vs. frequency

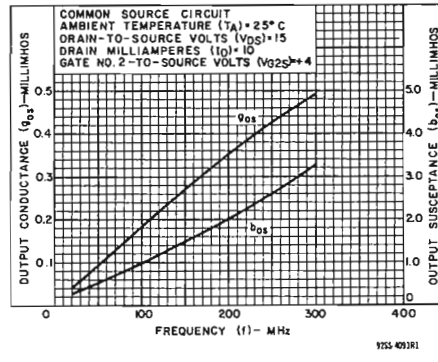


Fig. 21 - y_{os} vs. frequency

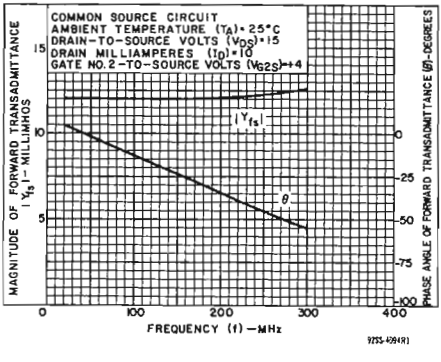


Fig. 22 - y_{fs} vs. frequency

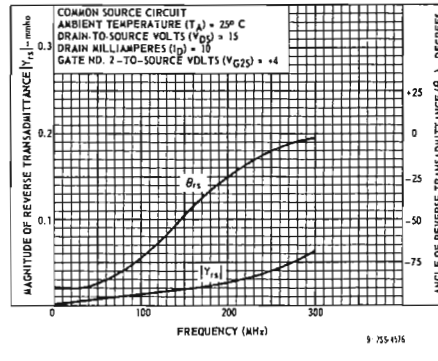


Fig. 23. - y_{rs} vs. frequency

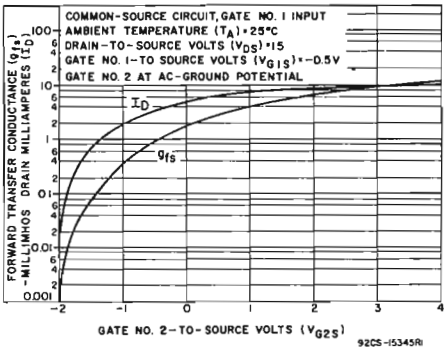


Fig. 24 - g_{fs} and I_D vs. V_{G2S}

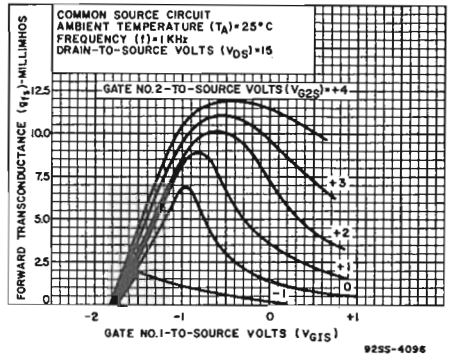


Fig. 25. - g_{fs} vs. V_{G1S}

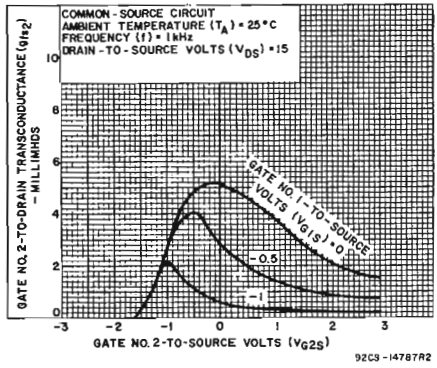
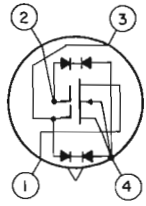


Fig. 26 - g_{fs_2} vs. V_{G2S}

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

RCA
Solid State
Division

MOS Field-Effect Transistors

N-Channel Depletion Types

3N200

JEDEC TO-72

Silicon Dual Insulated-Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits

For Military and Industrial Applications up to 500 MHz

Applications

- RF amplifier, mixer, and IF amplifier in military and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

RCA-3N200 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 3N200 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-3N200 make it useful for a wide variety of rf-amplifier applications at frequencies up to 500 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 3N200 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 3N200 is hermetically sealed in the metal JEDEC TO-72 package.

Maximum Ratings, *Absolute-Maximum Values, at* $T_A = 25^oC$

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
* DRAIN CURRENT, I_D	50	mA
* TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
* LEAD TEMPERATURE (During soldering):		
At distances ≥1/32 inch from seating surface for 10 seconds max.	265	°C

*In accordance with JEDEC registration data format (JS-9 RDF-19A)

Performance Features

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- Wide dynamic range permits large-signal handling before overload
- Dual-gate permits simplified agc circuitry
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

Device Features

- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance — g_{fs} = 15,000 μmho (typ.)
- High unneutralized RF power gain — G_{ps} = 12.5 dB (typ.) at 400 MHz = 19 dB (typ.) at 200 MHz
- Low VHF noise figure — 3.9 dB (typ.) at 400 MHz 3.0 dB (typ.) at 200 MHz

	ELECTRICAL CHARACTERISTICS *at T_A = 25°C unless otherwise specified*		SYMBOLS	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
*	Gate No. 1-to-Source Cutoff Voltage		$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V		-0.1	-1	-3	V
*	Gate No. 2-to-Source Cutoff Voltage		$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0		-0.1	-1	-3	V
*	Gate No. 1-Terminal Forward Current		I_{G1SSF}	V_{G1S} = +1 V V_{G2S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 1-Terminal Reverse Current		I_{G1SSR}	V_{G1S} = -6 V V_{G2S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Forward Current		I_{G2SSF}	V_{G2S} = +6 V V_{G1S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Reverse Current		I_{G2SSR}	V_{G2S} = -6 V V_{G1S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Zero-Bias Drain Current		I_{DS}	V_{DS} = +15 V, V_{G1S} = 0 V_{G2S} = +4 V		0.5	5.0	12	mA
*	Forward Transconductance (Gate No. 1-to-Drain)		g_{fs}	V_{DS} = +15 V I_D = 10 mA V_{G2S} = +4 V	f = 1 kHz	10,000	15,000	20,000	μmho
	Small-Signal, Short-Circuit Input Capacitance†		C_{iss}		f = 1 MHz	4.0	6.0	8.5	pF
*	Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦		C_{rss}			0.005	0.02	0.03	pF
	Small-Signal, Short-Circuit Output Capacitance		C_{oss}			–	2.0	–	pF
*	Power Gain (see Fig. 1)		G_{PS}		f = 400 MHz	10	12.5	–	dB
	Noise Figure (see Fig. 1)		NF			–	3.9	6.0	dB
*	Bandwidth		BW			28	–	38	MHz
*	Gate-to-Source Forward Breakdown Voltage	Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	V_{G2S} = V_{DS} = 0	6.5	–	13	V
		Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} = V_{DS} = 0				
*	Gate-to-Source Reverse Breakdown Voltage	Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	V_{G2S} = V_{DS} = 0	-6.5	–	-13	V
		Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} = V_{DS} = 0				

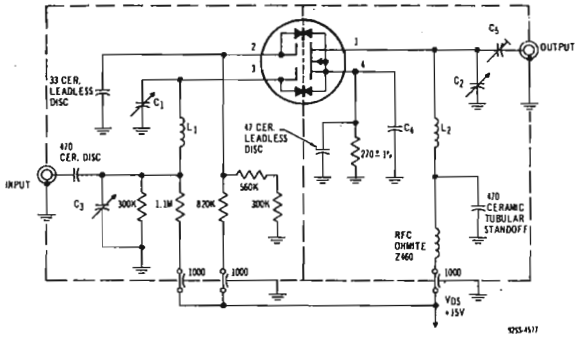
*In accordance with JEDEC registration data format (JS-9 RDF-19A)

†Capacitance between Gate No. 1 and all other terminals.

♦Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.

OPERATING CONSIDERATIONS

The flexible leads of the 3N200 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.



All resistances in ohms
All capacitances in pF

C_1, C_2: 1.3-5.4 pF variable air capacitor: Hammerland Mac 5 type or equivalent

C_3: 1.9-13.8 pF variable air capacitor: Hammerland Mac 15 type or equivalent

C_4: Approx. 300 pF - capacitance formed between socket cover & chassis

C_5: 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent

L_1, L_2: Inductance to tune circuit

Fig. 1 - 400 MHz power gain and noise figure test circuit

Typical Characteristics

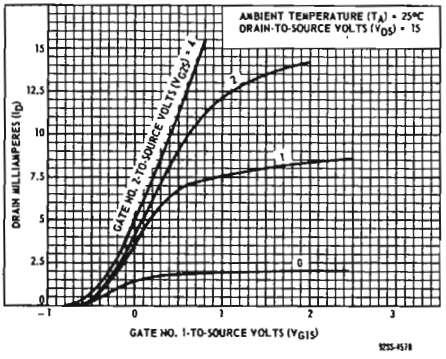


Fig. 2 - I_D vs. V_{G1S}

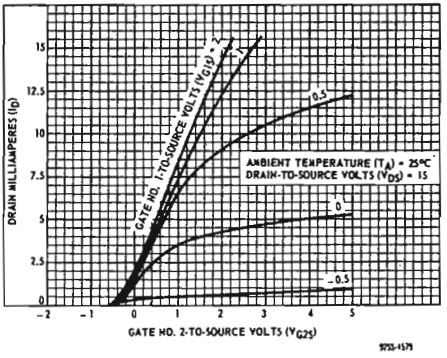


Fig. 3 - I_D vs. V_{G2S}

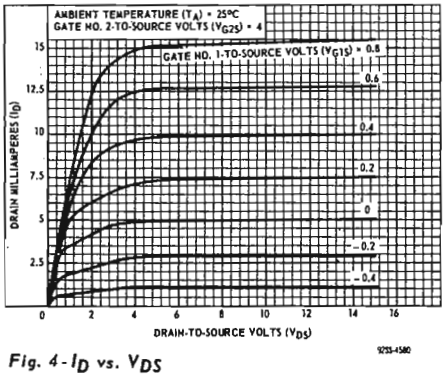


Fig. 4 - I_D vs. V_{DS}

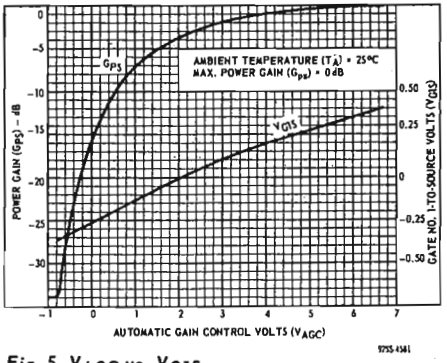


Fig. 5 - V_{AGC} vs. V_{G1S}

y and s Parameters vs. Frequency

TEST CONDITIONS: Drain-to-Source Volts (V_{DS}) = 15, Drain Milliamperes (I_D) = 10, Gate No. 2-to-Source Volts (V_{G2S}) = 4

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz)					UNITS
		100	200	300	400	500	
Maximum Available Power Gain	MAG	32	24	17.5	13	10	dB
Maximum Usable Power Gain (Unneutralized)*	MUG	32	24	17.5	13	10	dB
Y Parameters							
Input Conductance	g_{is}	0.25	0.8	2.0	3.6	6.2	mmho
Input Susceptance	b_{is}	3.4	5.8	8.5	11.2	15.5	mmho
Magnitude of Forward Transadmittance	$\lvert y_{fs} \rvert$	15.3	15.3	15.4	15.5	16.3	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	−15	−25	−35	−47	−60	degrees
Output Conductance	g_{os}	0.15	0.3	0.5	0.8	1.1	mmho
Output Susceptance	b_{os}	1.5	2.7	3.6	4.25	5.0	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs} \rvert$	0.012	0.025	0.06	0.14	0.26	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	−60	−25	0	14	20	degrees
S Parameters							
Magnitude of Input Reflection Coeff.	$\lvert s_{is} \rvert$	0.97	0.90	0.84	0.78	0.70	
Angle of Input Reflection Coeff.	$\angle s_{is}$	−20	−32	−55	−68	−82	degrees
Magnitude of Forward Transmission Coeff.	$\lvert s_{fs} \rvert$	1.50	1.40	1.25	1.1	0.9	
Angle of Forward Transmission Coeff.	$\angle s_{fs}$	153	133	112	90	70	degrees
Mangitude of Output Reflection Coeff.	$\lvert s_{os} \rvert$	0.985	0.95	0.93	0.92	0.91	
Angle of Output Reflection Coeff.	$\angle s_{os}$	−7.5	−16	−22	−28	−34	degrees
Magnitude of Reverse Transmission Coeff.	$\lvert s_{rs} \rvert$	0.001	0.0025	0.005	0.010	0.0165	
Angle of Reverse Transmission Coeff.	$\angle s_{rs}$	100	125	141	150	142	degrees

*Limited only by practical design considerations

Typical y Parameters vs. V_{DS}

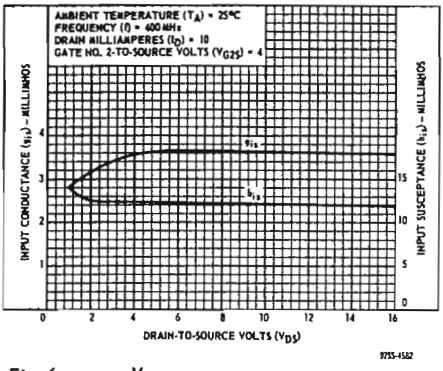


Fig. 6 - y_{is} vs. V_{DS}

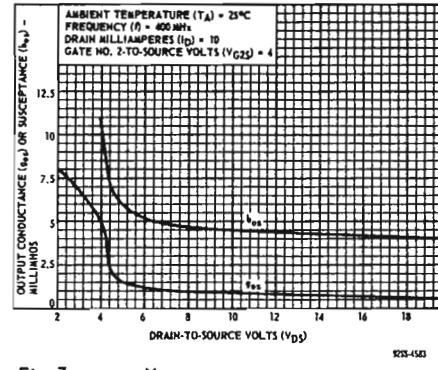


Fig. 7 - y_{os} vs. V_{DS}

Typical y Parameters vs. V_{DS} (cont'd)

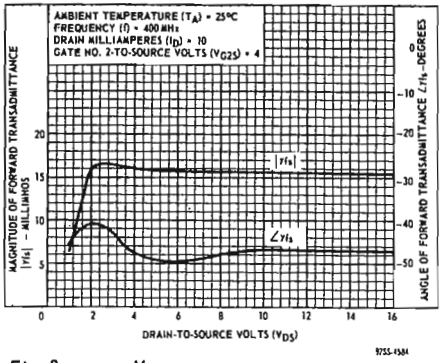


Fig. 8 - y_{fs} vs. V_{DS}

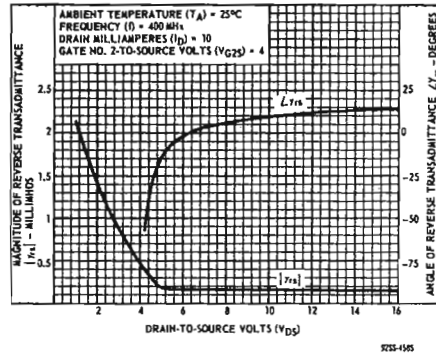


Fig. 9 - y_{rs} vs. V_{DS}

Typical y Parameters vs I_D

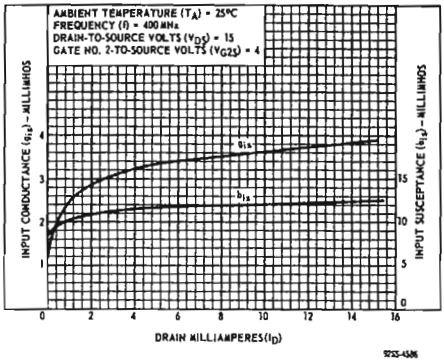


Fig. 10 - y_{is} vs. I_D

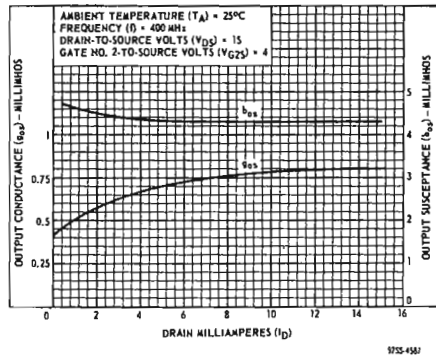


Fig. 11 - y_{os} vs. I_D

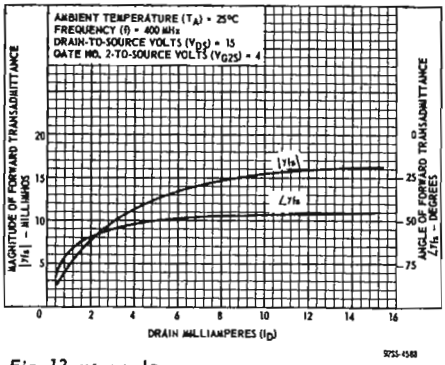


Fig. 12 - y_{fs} vs. I_D

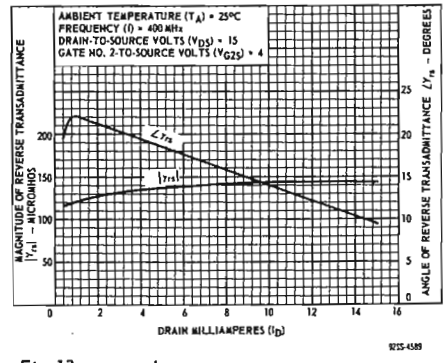


Fig. 13 - y_{rs} vs. I_D

Typical y Parameters vs. V_{G2S}

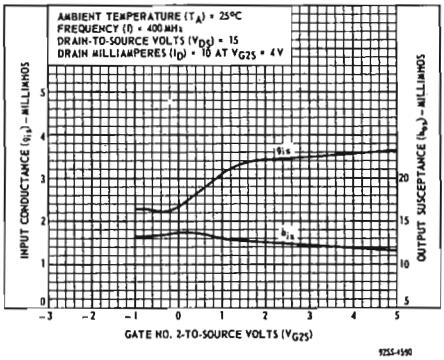


Fig. 14 - y_{is} vs. V_{G2S}

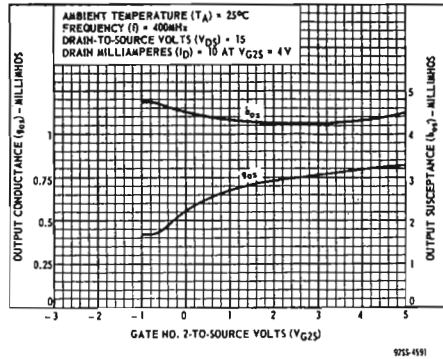


Fig. 15 - y_{os} vs. V_{G2S}

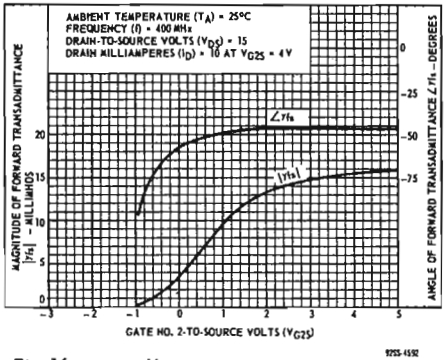


Fig. 16 - y_{fs} vs. V_{G2S}

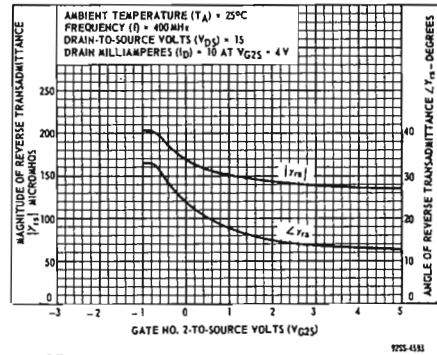


Fig. 17 - y_{rs} vs. V_{G2S}

Typical Characteristics

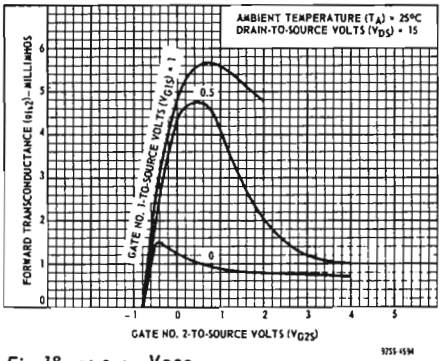


Fig. 18 - g_{fs2} vs. V_{G2S}

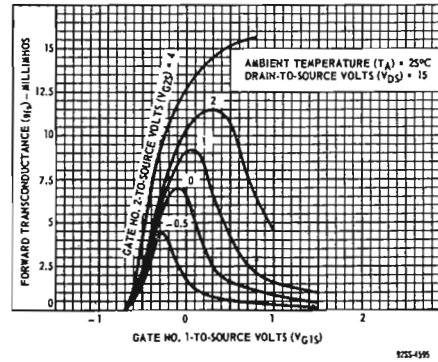


Fig. 19 - g_{fs} vs. V_{G1S}

Typical Characteristics (Cont'd)

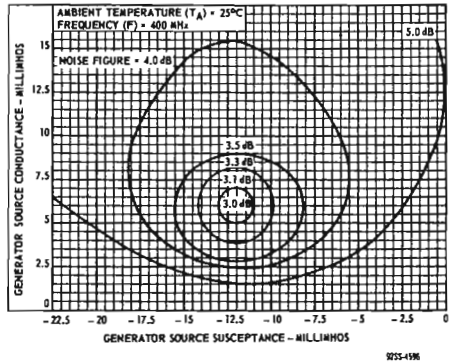
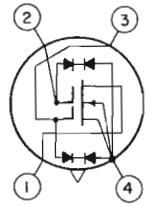


Fig. 20 - Noise figure vs. generator source admittance

TERMINAL DIAGRAM



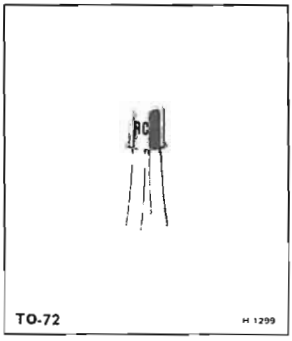
LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

RCA
Solid State
Division

MOS Field-Effect Transistors

N-Channel Depletion Type

40467A



Silicon MOS Transistor

For VHF Tuners and Other VHF Amplifier Applications in Industrial & Commercial Electronic Equipment Operating up to 220 MHz

Device Features:

- Low feedback capacitance - C_{rss} = 0.25 pF typ.
- High forward transconductance - g_{fs} = 7500 μmho typ.
- High vhf power gain - G_{PS} = 16 dB typ at 200 MHz
- Low vhf noise figure - NF = 3.5 dB typ at 200 MHz
- Exceptionally good cross-modulation characteristics

Performance Features:

- Large dynamic range
- Greatly reduced spurious responses
- Permits use of vacuum-tube biasing techniques
- Excellent thermal stability
- Superior cross-modulation performance and greater dynamic range than bipolar transistors

RCA-40467A is an n-channel depletion-type silicon insulated-gate field-effect transistor utilizing the MOS■ construction. It is intended primarily for vhf-amplifier applications in industrial and commercial electronic equipment.

The 40467A is useful in vhf applications requiring devices capable of providing high useful power gains at frequencies up to approximately 220 MHz.

The 40467A features high forward transconductance, high dc gate-to-source resistance, and low feedback capacitance. Because of the improved transfer characteristic and increased dynamic range, the 40467A provides substantially better cross-modulation performance in linear-amplifier applications than conventional (bipolar) transistors and is free from diode-current loading, a problem that exists in junction type FET s. This device is hermetically sealed in the TO-72 metal case and utilizes full-gate construction.

■ Metal-Oxide Semiconductor

Maximum Ratings, *Absolute-Maximum Values at* T_A = 25°C:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	V
DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
GATE-TO-SOURCE VOLTAGE, V_{GS}:		
CONTINUOUS (dc)	+1, -8	V
PEAK ac	±15	V
DRAIN CURRENT, I_D	50	mA
TRANSISTOR DISSIPATION:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate at 2.2	mW/°C
AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265	°C

ELECTRICAL CHARACTERISTICS AT T_C = 25°C WITH BULK (SUBSTRATE) CONNECTED TO SOURCE

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS			UNITS
		FREQUENCY f	DC DRAIN-TO-SOURCE VOLTAGE V_{DS}	DC DRAIN CURRENT I_D	RCA 40467A			
		MHz	V	mA	Min	Typ.	Max.	
Gate-to-Source Cutoff Voltage	$V_{GS(off)}$		12	0.1	-	-	-8	V
Gate Leakage Current	I_{GSS}		0	V_{GS} = +1V	-	-	1	nA
			0	V_{GS} = -8V	-	-	1	nA
Zero-Bias Drain Current	I_{DSS}		15	V_{GS} = 0	5	15	30	mA
Small-Signal, Short-Circuit Forward Transconductance	g_{fs}	1 KHz	15	5	4000	7500	-	μmho
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15	5	0.12	0.25	0.35	pF
Small Signal Short-Circuit Input Capacitance	C_{iss}	1	15	5	-	5.5	-	pF
Input Admittance	Y_{is}	Common Source Configuration f = 200 mHz V_{DS} = 15V I_D = 5 mA			-	0.4 + j7.3	-	
Forward Transfer Admittance	Y_{fs}				-	7 - j2	-	
Output Admittance	Y_{os}				-	0.28 + j1.8	-	
Maximum Available Power Gain	MAG	200	15	5	-	21	-	dB
Maximum Usable Power Gain (unneutralized)	MUG	200	15	5	-	12	-	dB
Maximum Usable Power Gain (neutralization)	MUG	200	15	5	12	16	-	dB
Noise Figure	NF	200	15	5	-	3.5	5	dB

TYPICAL CHARACTERISTICS

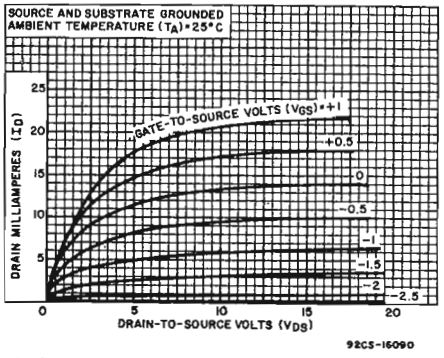


Fig. 1

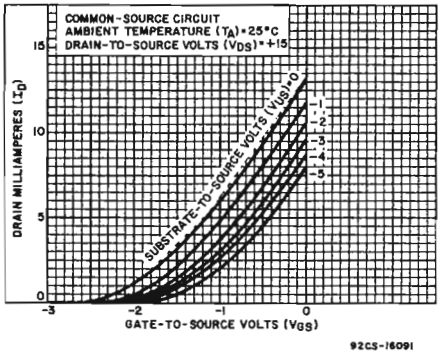


Fig. 2

TYPICAL ADMITTANCE CHARACTERISTICS

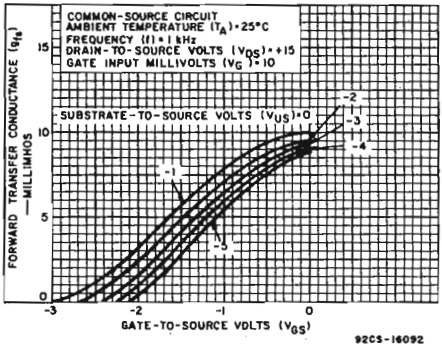


Fig. 3

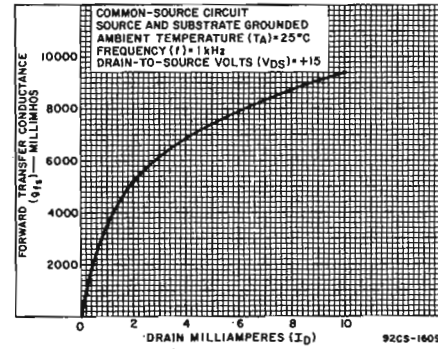


Fig. 4

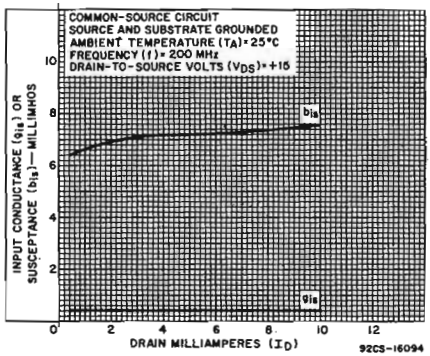


Fig. 5

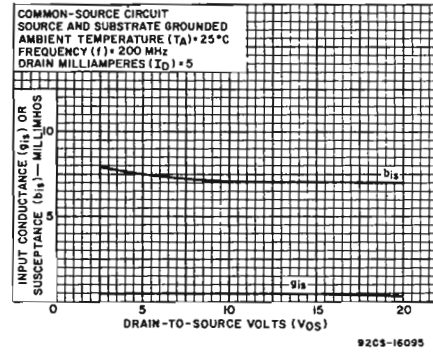


Fig. 6

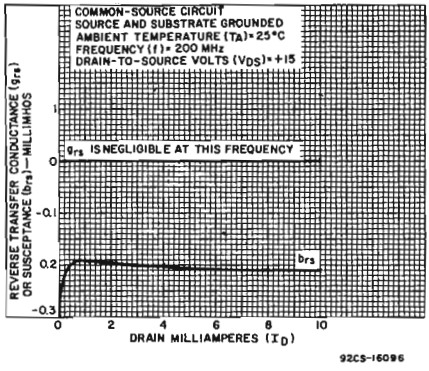


Fig. 7

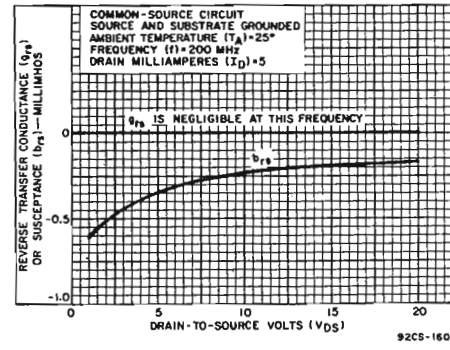


Fig. 8

TYPICAL ADMITTANCE CHARACTERISTICS (cont'd)

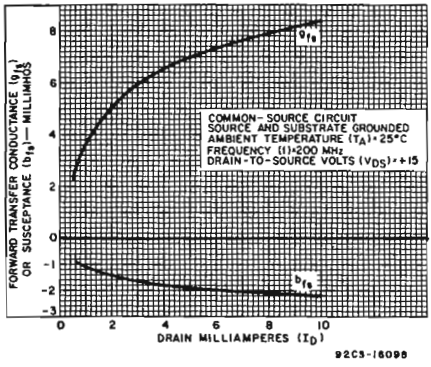


Fig. 9

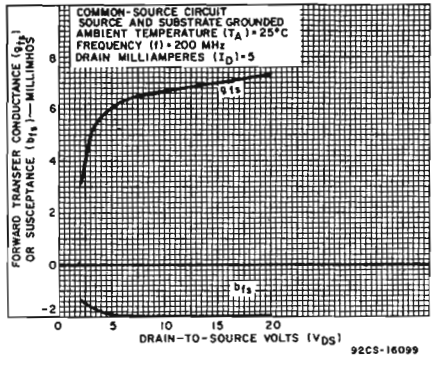


Fig. 10

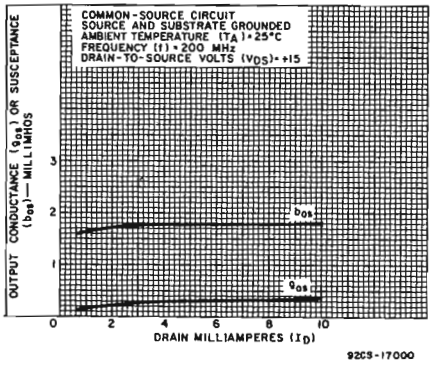


Fig. 11

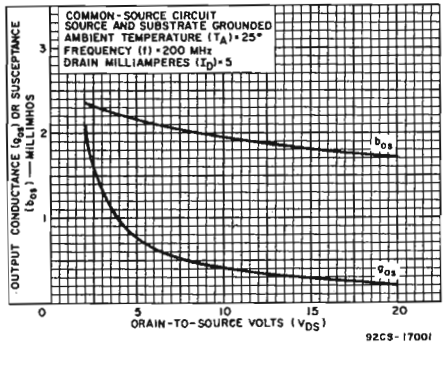
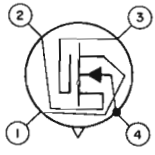


Fig. 12

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

OPERATING CONSIDERATIONS

The flexible leads of the 40467A are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the devices against high electric fields.

This device should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

RCA
Solid State
Division

MOS Field-Effect Transistors

N-Channel Depletion Types

40468A
40559A

TO-72

MOS Silicon Transistors

For RF Amplifier and Mixer Applications in FM and AM/FM Receivers

Device Features:

- **high forward transconductance - -**
  gfs = 7500 μmho typ. for 40468A
- **low feedback capacitance - -**
  C_{rss} = 0.35 pF max. for 40468A
  0.38 pF max. for 40559A
- **high useful power gains - -**
  neutralized - 17 dB typ.
  unneutralized - 14 dB typ.
- **hermetically sealed in TO-72 metal package**

RCA-40468A and 40559A are silicon insulated-gate field-effect transistors of the n-channel depletion type utilizing the MOS* construction. They are intended primarily for use as the rf amplifier and mixer, respectively, in FM receivers covering the 88 to 108 MHz band, but can be used for general amplifier applications at frequencies up to 125 MHz. For circuit design and typical performance data refer to RCA Application Note AN3535 "An FM Tuner Using Single-Gate MOS Field-Effect Transisters as RF Amplifier and Mixer".

The wide dynamic range of these transistors reduces cross-modulation effects in AM receivers and minimizes the generation of spurious responses in FM receivers.

Operating as a neutralized amplifier at 100 MHz, the 40468A can provide a power gain of 17 dB (typ.). A power gain of 14 dB (typ.) can be realized without neutralization.

* Metal-Oxide-Semiconductor.

Performance Features:

- **reduced spurious responses in FM tuners**
- **reverse bias on substrate improves linearity**
- **reduced cross-modulation effects in AM receivers**

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	V
DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
GATE-TO-SOURCE VOLTAGE, V_{GS}:		
CONTINUOUS (dc)	+1, -8	V
PEAK ac	±15	V
DRAIN CURRENT, I_D	25	mA
TRANSISTOR DISSIPATION:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate at 2.2	mW/°C
AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265	°C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

With Bulk (Substrate) Connected to Source Unless Otherwise Specified

Characteristics	Symbols	TEST CONDITIONS			LIMITS						Units
		Frequency f	DC Drain-to-Source V_{DS}	DC Drain Current I_D	RCA-40468A RF Amplifier			RCA-40559A Mixer			
		MHz	V	mA	Min.	Typ.	Max.	Min.	Typ.	Max.	
Drain-to-Source Cutoff Current	$I_{D(off)}$	-	12	V_{GS} = -8V	-	-	100	-	-	500	μA
Gate Leakage Current	I_{GSS}	- -	0 0	V_{GS} = -8V V_{GS} = +1V	- -	- -	1 1	- -	- -	1 1	nA nA
Zero-Bias Drain Current	I_{DSS}	-	15	V_{GS} = 0	5	15	30	5	15	30	mA
Small-Signal, Short-Circuit Forward Transconductance	g_{fs}	1 kHz	15	5	-	7500	-	-	-	-	μmho
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15	5	-	0.25	0.35	-	0.25	0.38	pF
Input Capacitance	C_{iss}	1	15	5	-	5.5	-	-	5.5	-	pF
Admittance	-	RF | Mixer		RF | Mixer		-			-		-
Input Admittance	Y_{is}	100 MHz	15	5 | 3	0.155 + j 3.45			0.14 + j 3.38			mmho
Forward Transfer Admittance	Y_{fs}	100 MHz	15	5 | 3	7.4 + j 0.9			-			mmho
Output Admittance	Y_{os}	100 MHz | 10.7 MHz	15	5 | 3	0.21 + j 0.9			0.076 + j 0.153			mmho
Forward Conversion Transconductance	$g_{fs(c)}$	1 kHz	15	3	-	-	-	-	2800*	-	μmho
Maximum Available Power Gain	MAG	100	15	5	-	26	-	-	-	-	dB
Maximum Usable Power Gain (Unneutralized)	MUG	100	15	5	-	14	-	-	-	-	dB
Maximum Usable Power Gain (Neutralized)	MUG	100	15	5	14	17	-	-	-	-	dB
Maximum Available Conversion Gain	MAG_C	f_{in} = 100 f_{out} = 10.7	15	3	-	-	-	-	22	-	dB
Noise Figure	NF	100	15	5	-	3.5	5	-	-	-	dB

* Bulk (Substrate)-to-Source Volts (V_{BS}) = -3.

OPERATING CONSIDERATIONS

The flexible leads of the 40468A and 40559A are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the devices against high electric fields.

These devices should not be connected into, or disconnected from, circuits with the power on because high transient voltages may cause permanent damage to the devices.

TYPICAL y-PARAMETER CHARACTERISTICS

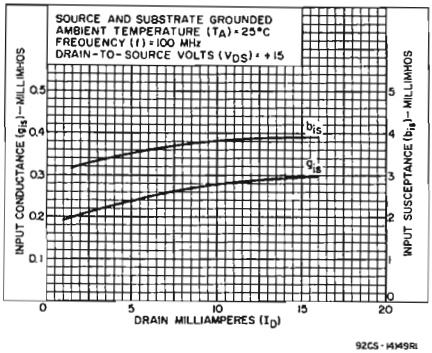


Fig.1 - Input admittance (y_{is}) vs drain current (I_D).

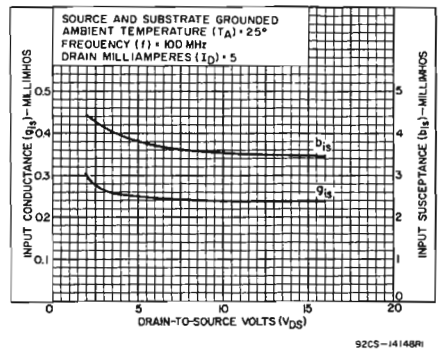


Fig.2 - Input admittance (y_{is}) vs drain-to-source voltage (V_{DS}).

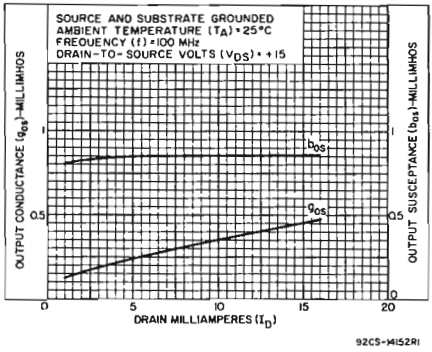


Fig.3 - Output admittance (y_{os}) vs drain current (I_D).

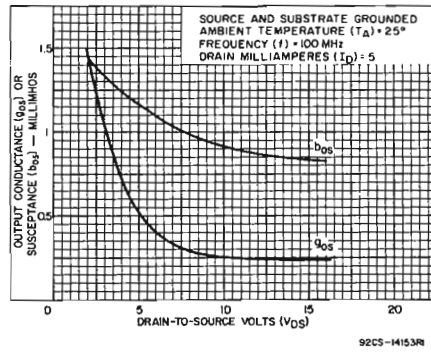


Fig.4 - Output admittance (y_{os}) vs drain-to-source voltage (V_{DS}).

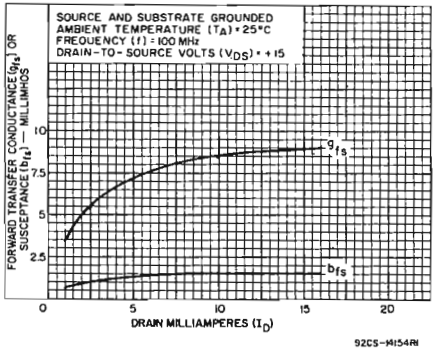


Fig.5 - Forward transadmittance (y_{fs}) vs drain current (I_D).

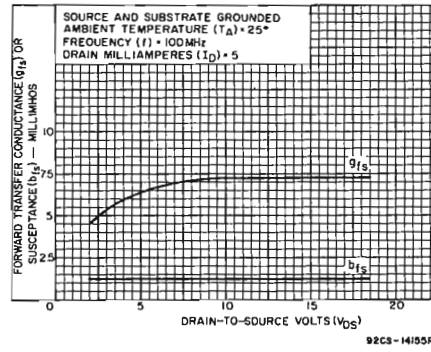


Fig.6 - Forward transadmittance (y_{fs}) vs drain-to-source voltage (V_{DS}).

TYPICAL y-PARAMETER CHARACTERISTICS

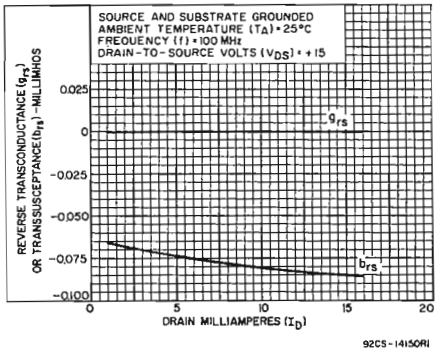


Fig.7 - Reverse transadmittance (y_{rs}) vs drain current (I_D).

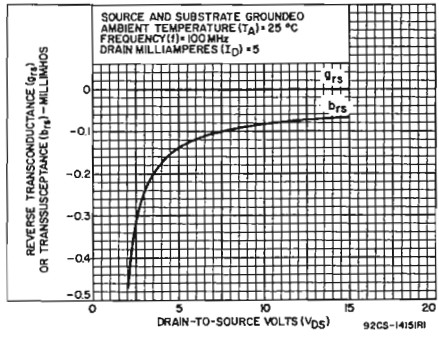


Fig.8 - Reverse transadmittance (y_{rs}) vs drain-to-source voltage (V_{DS}).

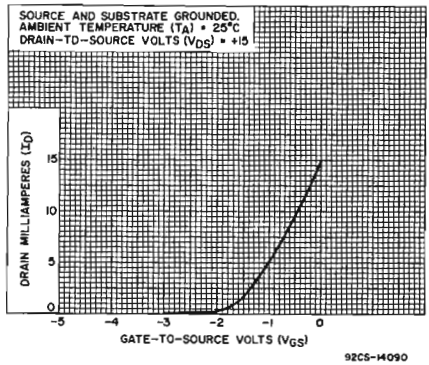
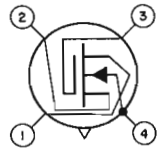


Fig.9 - Typical characteristic of drain current (I_D) vs gate-to-source voltage (V_{GS}).

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - SOURCE
LEAD 3 - INSULATED GATE
LEAD 4 - BULK (SUBSTRATE) AND CASE

RCA Solid State Division

MOS Field-Effect Transistors

40600
40601
40602

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTORS

TO-72

N-Channel Depletion Types For VHF TV Receiver Applications

RCA 40600, 40601, and 40602 are n-channel depletion type, dual-insulated-gate, field-effect transistors utilizing the MOS construction. These devices have characteristics which make them highly desirable for rf-amplifier applications (40600), mixer applications (40601), and first-if-amplifier applications (40602) in vhf TV receivers and other types of commercial equipment operating at frequencies up to approximately 250 MHz.

These transistors feature a series arrangement of two separate channels, each channel having an independent control gate. In amplifier applications the 40600 and 40602 with their wide dynamic range provide substantially better cross-modulation performance than is obtainable with bipolar or single-gate field-effect transistors. In mixer applications the 40601 provides excellent isolation between the oscillator and rf signals because each of the two signal frequencies being mixed has its own control element. The wide dynamic range of the 40601 minimizes cross-modulation which is generally encountered in mixer stages.

Provision of two insulated gates also results in extremely low feedback capacitances (0.02 pF typ.), a feature which enables the 40600 and 40602 to provide high maximum useable power gains in unneutralized circuits — for example, 20 dB at 200 MHz typ. for the 40600, and 35 dB typ. at 44 MHz for the 40602. The gain of the rf and if stages can be controlled by applying agc voltage to gate No.2 and agc delay is easily obtained. Virtually no agc power is required for full gain reduction.

Types 40600, 40601, and 40602 are hermetically sealed in metal JEDEC TO-72 packages.

APPLICATIONS

- VHF TV Receiver
  - 40600 for rf amplifier applications
  - 40601 for mixer applications
  - 40602 for first-if-amplifier applications

PERFORMANCE FEATURES

- superior cross-modulation performance and greater dynamic range than bipolar and single-gate field-effect transistors
- permits use of vacuum-tube biasing techniques
- excellent thermal stability

DEVICE FEATURES

- extremely low feedback capacitance
  C_{rss} = 0.02 pF typ.
- high power gain
  MUG_u = 20 dB typ. for 40600
  MAG = 35 dB typ. for 40602
  MAG_c = 14 dB typ. for 40601

Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25°C$:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	0 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	+1 to -8	V
Peak ac	+20 to -8	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-8 to 40% of V_{DS}	V
Peak ac	-8 to +20	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} or V_{DG2}	+20	V
DRAIN CURRENT, I_D (Pulsed):		
Pulse duration $\leq$ 20 ms, duty factor $\leq$ 0.15	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	400	mW
At ambient temperatures above 25°C	derate linearly at 2.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances $\geq$ 1/32" from seating surface for 10 seconds max.	265	°C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS 40600, 40601, 40602			UNITS
			Min.	Typ.	Max.	
Gate No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15V, I_D = 200 μA V_{G2S} = +4V	-	-2	-	V
Gate No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15V, I_D = 200 μA V_{G1S} = 0	-	-2	-	V
Gate No.1 Leakage Current	I_{G1SS}	V_{G1S} = -20V, V_{G2S} = 0, V_{DS} = 0	-	-	1	nA
Gate No.2 Leakage Current	I_{G2SS}	V_{G2S} = -20V, V_{G1S} = 0, V_{DS} = 0	-	-	1	nA
Drain Current	I_{DSS}	V_{DS} = +13V, V_{G1S} = 0, V_{G2S} = +4V	-	18	-	mA
Forward Transconductance	g_{fs}	V_{DS} = +13V, I_D = 10 mA V_{G2S} = +4V, f = 1 kHz	-	10000	-	μmho

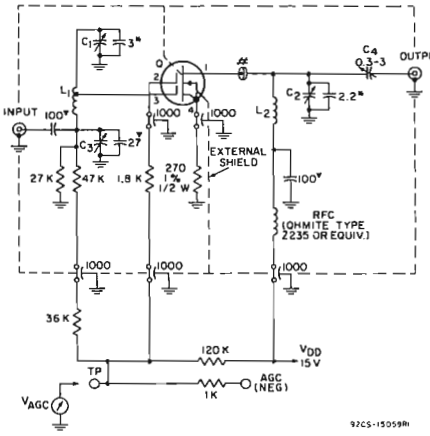
TYPICAL PERFORMANCE CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS	SYMBOLS	40600 RF AMPLIFIER f = 200 MHz	40602 IF AMPLIFIER f = 44 MHz	40601 MIXER f = 200 MHz	UNITS
		V_{G1S} is adjusted for I_D = 10 mA Gate No.2 at AC ground potential V_{DS} = 13V, V_{G2S} = +4V		Local-oscillator injection Voltage on Gate No.2 = 750 mV V_{DS} = 15V V_{G2S} = +0.6V V_{G1S} = 0.75V	
Small-Signal, Short Circuit Reverse-Transfer Capacitance (Drain-to-Gate No.1) at f = 1 MHz	C_{rss}	0.02 typ. 0.03 max.	0.02 typ. 0.03 max.	0.02 typ. 0.03 max.	pF
Output Capacitance	C_{oss}	2.2	2.2	2.2 at f = 44 MHz	pF
Input Capacitance	C_{iss}	5.5	5.5	5.5	pF
Input Resistance	r_{iss}	1.2	10	1.2	KΩ
Output Resistance	r_{oss}	2.8	12	12 at f = 44 MHz	KΩ
Magnitude of Forward Transadmittance	$\|Y_{fs}\|$	11000	11000	2700*	μmho
Phase Angle of Forward Transadmittance	$\angle\theta$	-46	-11	-	degrees
Maximum Available Power Gain	MAG	20	35	14**	dB
Maximum Usable Power Gain (Unneutralized)	MUG_u	20▲	1 Stage 28 2 Stages 26 3 Stages 24	- - -	dB dB dB
Power Gain See Fig.1 for measurement circuit	G_{PS}	17.5	-	-	dB
Noise Figure	NF	5 max.	-	-	dB

* Magnitude of forward conversion transadmittance

** Maximum available conversion gain

▲ Limited by practical design considerations



* Tubular ceramic.

▼ Disk ceramic.

\# Ferrite bead (½ used); Indiana General No. H1742C-(A-147) or F1157-1-H, or equivalent.

C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102, or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13, or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07"- 0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - 200 MHz Power Gain and Noise Figure Test Circuit for 40600 and 40602

TYPICAL SMALL-SIGNAL Y-PARAMETER CHARACTERISTICS at 200 MHz

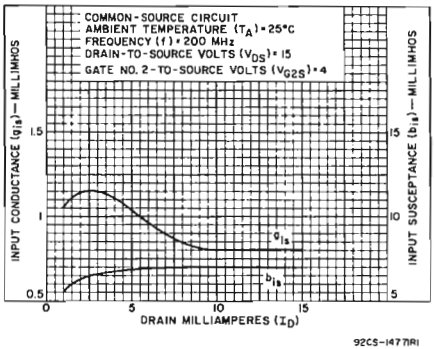


Fig.2 - Y_{is} vs. I_D

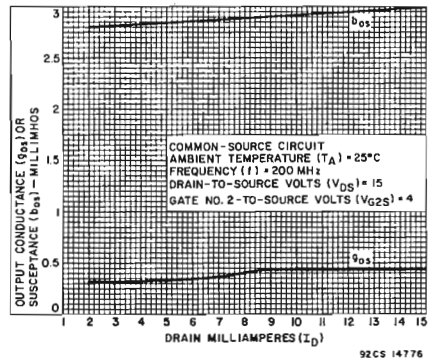


Fig.3 - Y_{os} vs. I_D

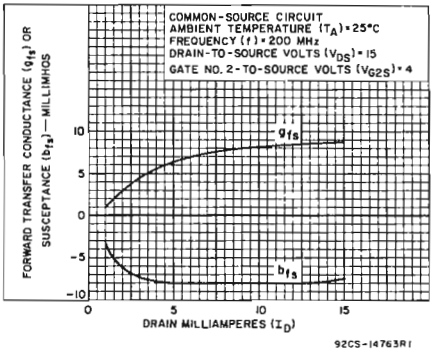


Fig.4 - Y_{fs} vs. I_D

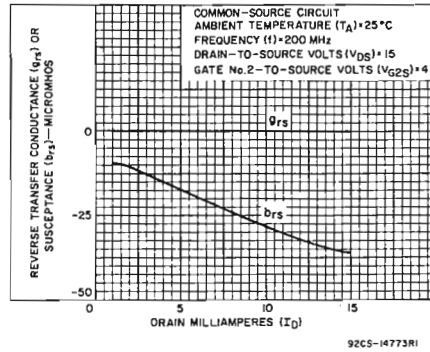


Fig.5 - Y_{rs} vs. I_D

TYPICAL SMALL-SIGNAL Y-PARAMETER CHARACTERISTICS at 200 MHz

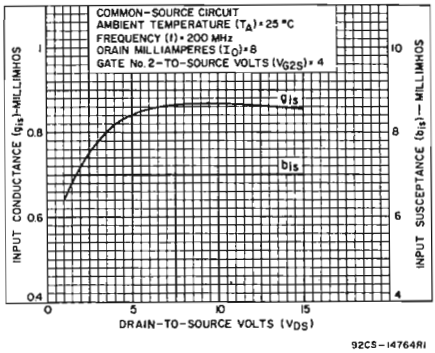


Fig.6 - Y_{is} vs. V_{DS}

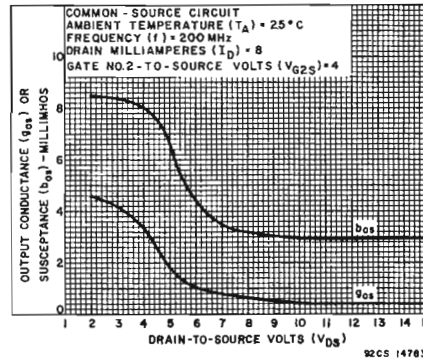


Fig.7 - Y_{os} vs. V_{DS}

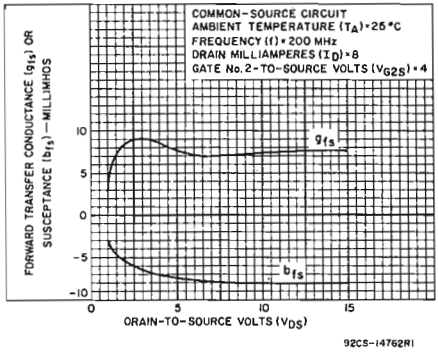


Fig.8 - Y_{fs} vs. V_{DS}

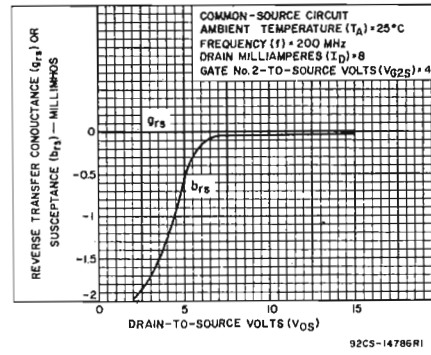


Fig.9 - Y_{rs} vs. V_{DS}

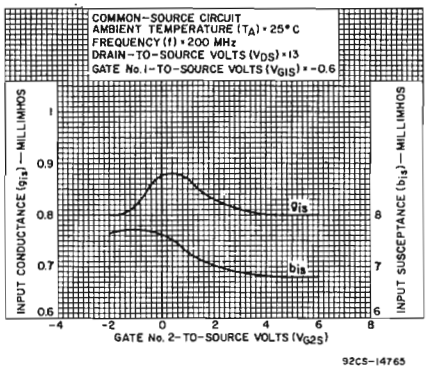


Fig.10 - Y_{is} vs. V_{G2S}

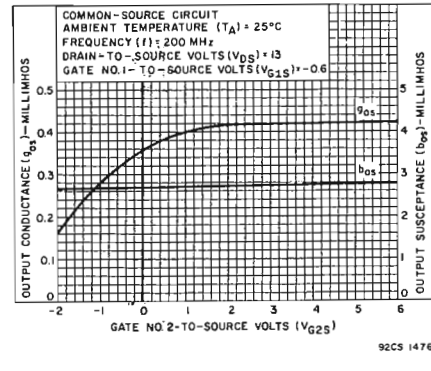


Fig.11 - Y_{os} vs. V_{G2S}

TYPICAL Y-PARAMETER CHARACTERISTICS at 200 MHz

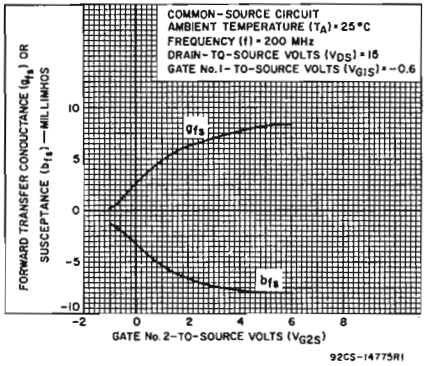


Fig.12 - Y_{fs} vs. V_{G2S}

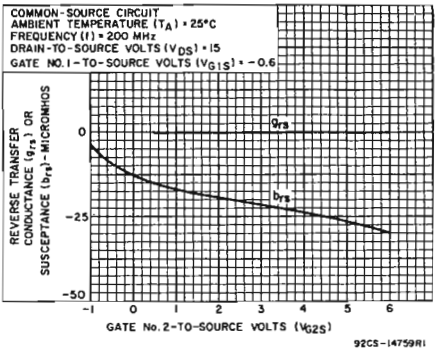


Fig.13 - Y_{rs} vs. V_{G2S}

TYPICAL SMALL-SIGNAL Y-PARAMETER CHARACTERISTICS at 44 MHz

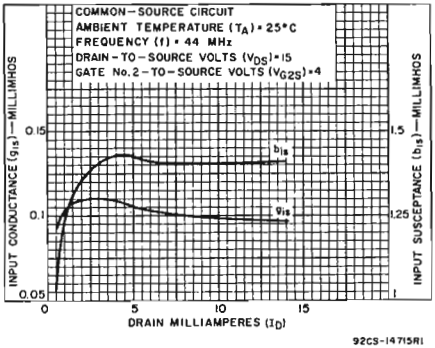


Fig.14 - Y_{is} vs. I_D

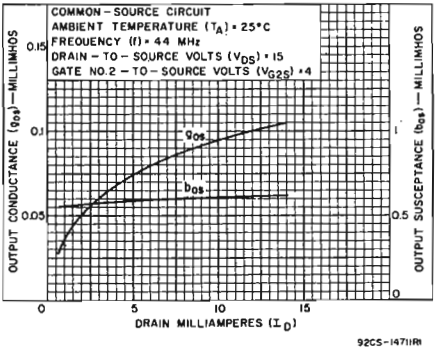


Fig.15 - Y_{os} vs. I_D

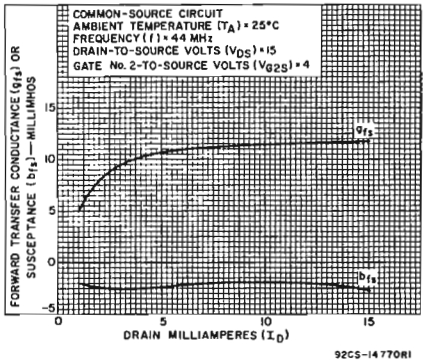


Fig.16 - Y_{fs} vs. I_D

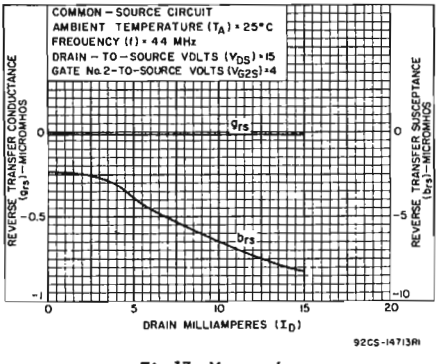


Fig.17 - Y_{rs} vs. I_D

TYPICAL SMALL-SIGNAL Y-PARAMETER CHARACTERISTICS at 44 MHz

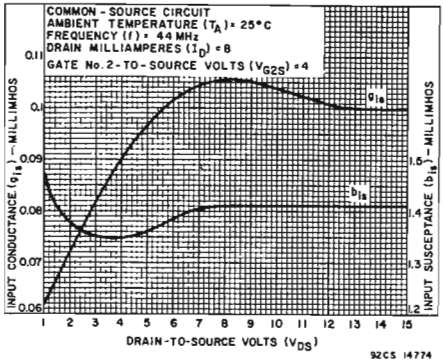


Fig.18 - Y_{is} vs. V_{DS}

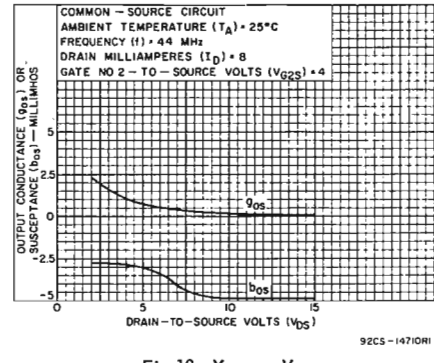


Fig.19 - Y_{os} vs. V_{DS}

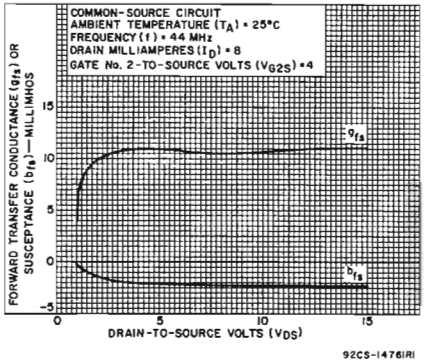


Fig.20 - Y_{fs} vs. V_{DS}

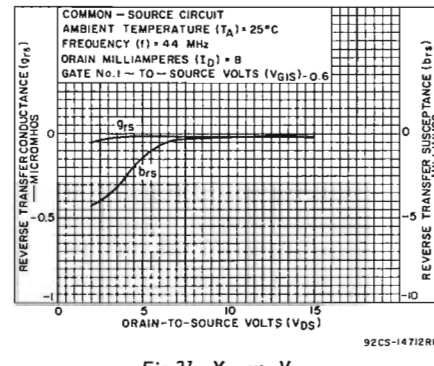


Fig.21 - Y_{rs} vs. V_{DS}

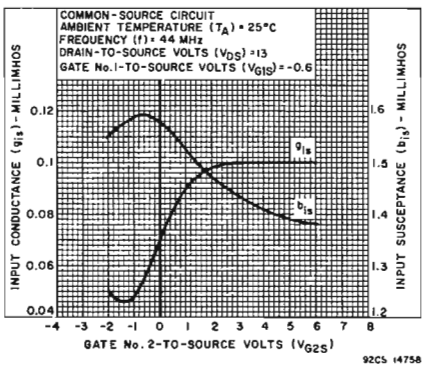


Fig.22 - Y_{is} vs. V_{G2S}

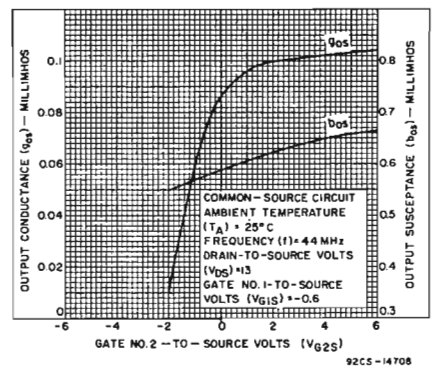


Fig.23 - Y_{os} vs. V_{G2S}

TYPICAL SMALL-SIGNAL Y-PARAMETER CHARACTERISTICS at 44 MHz

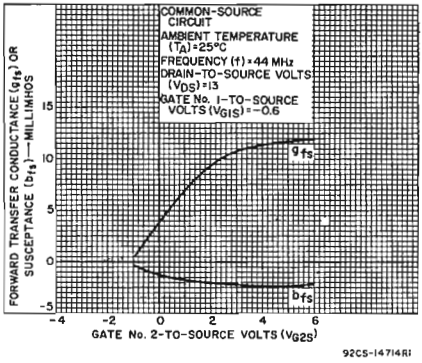


Fig.24 - Y_{fs} vs. V_{G2S}

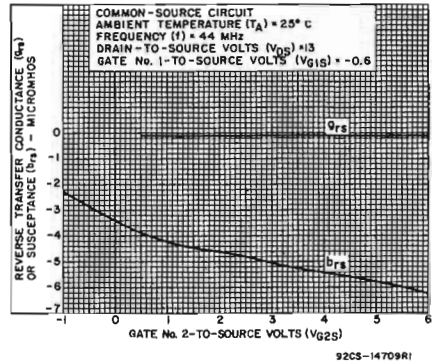


Fig.25 - Y_{rs} vs. V_{G2S}

TYPICAL SMALL-SIGNAL CHARACTERISTICS vs. FREQUENCY

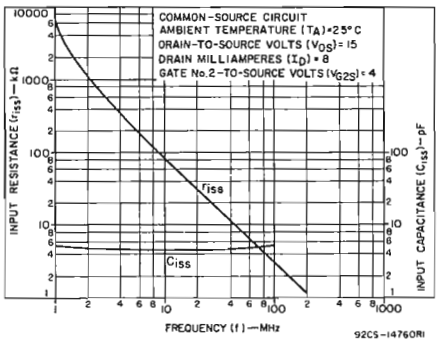


Fig.26 - C_{iss} and R_{iss} vs. f

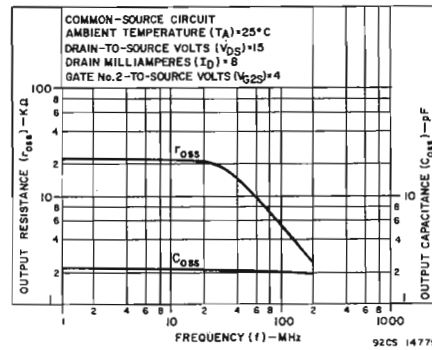


Fig.27 - C_{oss} and R_{oss} vs. f

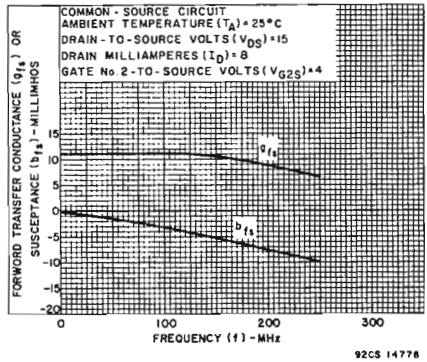


Fig.28 - Y_{fs} vs. f

TYPICAL TRANSFER CHARACTERISTICS

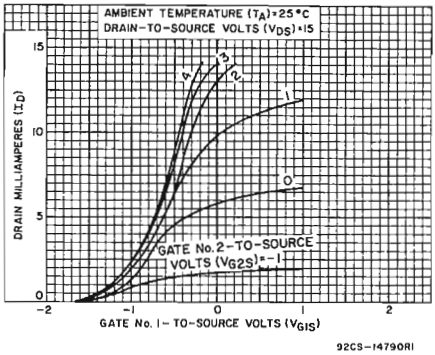


Fig.29 - I_D vs. V_{G1S}

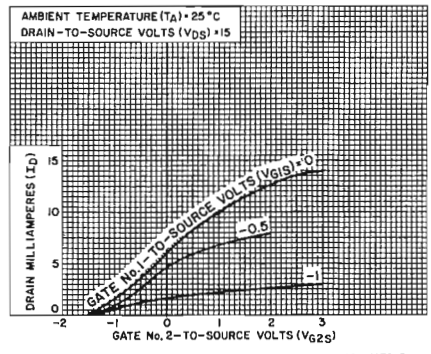


Fig.30 - I_D vs. V_{G2S}

TYPICAL OPERATING CHARACTERISTICS

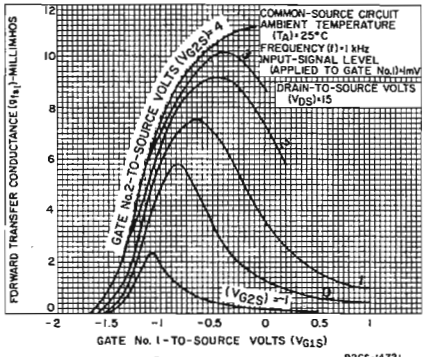


Fig.31 - g_{fs1} vs. V_{G1S}

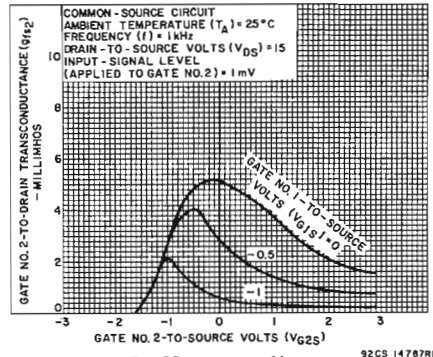
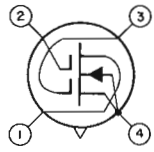


Fig.32 - g_{fs2} vs. V_{G2S}

TERMINAL DIAGRAM



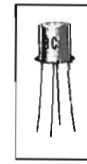
Lead 1 — Drain
Lead 2 — Gate No. 2
Lead 3 — Gate No. 1
Lead 4 — Source, Substrate and Case

RCA Solid State Division

MOS Field-Effect Transistors

40603
40604

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTORS



TO-72

N-Channel Depletion Types For FM Tuner Applications

RCA 40603 and 40604 are n-channel silicon, depletion type, dual insulated-gate, field-effect transistors utilizing the MOS construction.

These devices have exceptional characteristics for rf-amplifier (40603) and mixer applications (40604) in FM tuners and other commercial equipment operating at frequencies up to approximately 150 MHz. These transistors feature a series arrangement of two separate channels, each channel having an independent control gate. For amplifier applications the 40603 with its wide dynamic range provides substantially better cross-modulation performance and relative freedom from spurious responses than is obtainable with bipolar or single-gate field-effect transistors. The mixing function performed by the 40604 is unique in that the signal applied to gate No.2 is used to modulate the input-gate (gate No.1) transfer characteristic. This technique is superior to conventional "square law" mixing, which can only be accomplished in the non-linear region of the device transfer characteristic.

Because of the low feedback capacitance (0.02 typ. pF) the 40603 can provide a power gain of 25 dB (typ.) at 100 MHz in an unneutralized amplifier circuit.

The gain of the rf stage can be controlled by applying agc voltage to gate No.2. Virtually no agc power is required for full gain reduction.

The 40603 and 40604 are hermetically sealed in JEDEC TO-72 packages.

PERFORMANCE FEATURES

- large dynamic range permits large-signal handling before overload
- dual gates allow product mixing with extremely low hormonic generation
- greatly reduces spurious responses in FM receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability
- superior cross-modulation performance and greater dynamic range than bipolar and single-gate field-effect transistors

DEVICE FEATURES

- extremely low feedback capacitance
  C_{rss} = 0.02 pF typ.
- high unneutrolized RF power gain
  MUG = 25 dB (typ.) for 40603
- low noise figure
  NF = 2.5 dB typ. for 40603

Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25^{\circ}C$:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	0 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-8 to +1	V
Peak ac	-8 to +20	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-8 to 40% of V_{DS}	V
Peak ac	-8 to +20	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} or V_{DG2}	+20	V
DRAIN CURRENT, I_D (Pulsed):		
Pulse duration $\leq$ 20 ms, duty factor $\leq$ 0.15	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures: up to 25°C	400	mW
At ambient temperatures: above 25°C	derate linearly at 2.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances $\geq$ 1/32" from seating surface for 10 seconds max.	265	°C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			40603 RF AMPLIFIER		40604 MIXER		
			Typ.	Max.	Typ.	Max.	
Gate No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 200 μA V_{G2S} = +4 V	-2	--	-2	--	V
Gate No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 200 μA V_{G1S} = 0	-2	--	-2	--	V
Gate No.1 Leakage Current	I_{G1SS}	V_{G1S} = -20 V, V_{G2S} = 0, V_{DS} = 0	--	1	--	1	nA
Gate No.2 Leakage Current	I_{G2SS}	V_{G2S} = -20 V, V_{G1S} = 0, V_{DS} = 0	--	1	--	1	nA
Zero-Bias-Voltage Drain Current	I_{DSS}	V_{G2S} = +4 V, V_{G1S} = 0, V_{DS} = +13 V	18	--	18	--	mA
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate-No.1)	C_{rss}	V_{DS} = +13 V, I_D = 10 mA, f = 1 MHz V_{G2S} = +4 V	0.02	0.03	0.02	0.03	pF
Input Capacitance	C_{iss}	V_{DS} = +13 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 MHz	5.5	--	5.5	--	pF
Output Capacitance	C_{oss}	V_{DS} = +13 V, I_D = 10 mA V_{G2S} = +4 V, f = 100 MHz	2.1	--	2.3	--	pF
Input Resistance	r_{is}	V_{DS} = +13 V, I_D = 10 mA V_{G2S} = +4 V, f = 100 MHz	3.5	--	3.5	--	kΩ
Output Resistance	r_{os}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V; f = 100 MHz	4	--	--	--	kΩ
		V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V; f = 10.7 MHz	--	--	20	--	kΩ
Forward Transconductance	g_{fs}	V_{DS} = +13 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 kHz	10,000	--	2800*	--	μmho
Maximum Available Power Gain	MAG	V_{DS} = +13 V, I_D = 10 mA V_{G2S} = +4 V f = 100 MHz, f_{out} for 40604 (mixer) = 10.7 MHz	26	--	21	--	dB
Maximum Uaable Power Gain (Unneutralized)	MUG		25▲	-	--	--	dB
Noise Figure	NF		2.5	--	--	--	dB

* conversion transconductance

▲ or limited by practical design considerations

TYPICAL Y-PARAMETER CHARACTERISTICS at 100 MHz

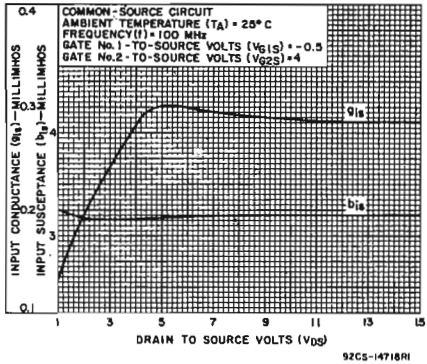


Fig.1 - Y_{is} vs. V_{DS}

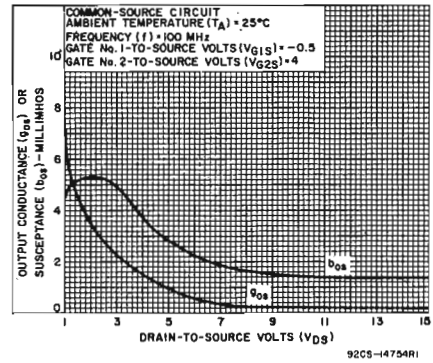


Fig.2 - Y_{os} vs. V_{DS}

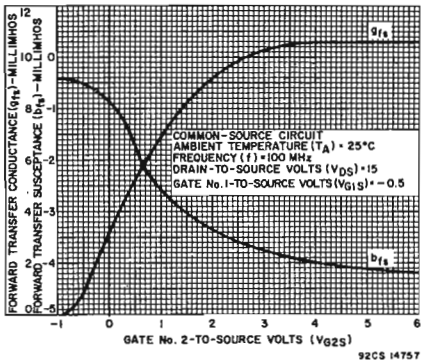


Fig.3 - Y_{fs} vs. V_{G2S}

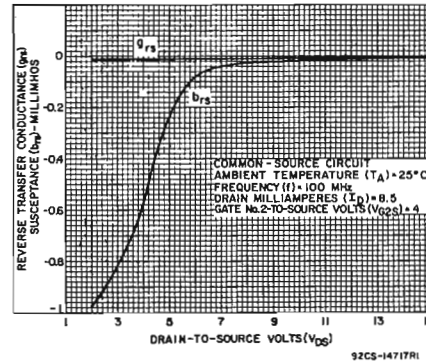


Fig.4 - Y_{rs} vs. V_{DS}

TYPICAL TRANSCONDUCTANCE CHARACTERISTIC

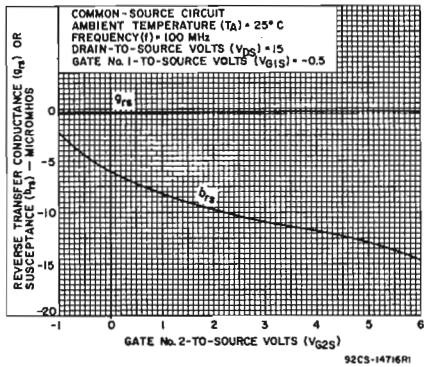


Fig.5 - Y_{rs} vs. V_{G2S}

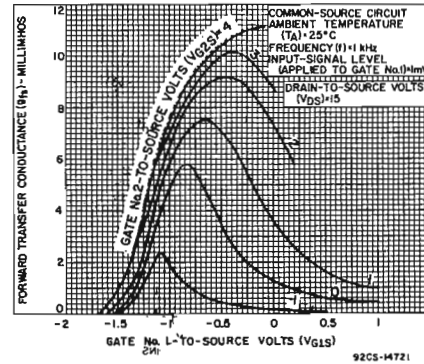


Fig.6 - Y_{fs} vs. V_{G1S}

TYPICAL Y-PARAMETER CHARACTERISTICS at 100 MHz

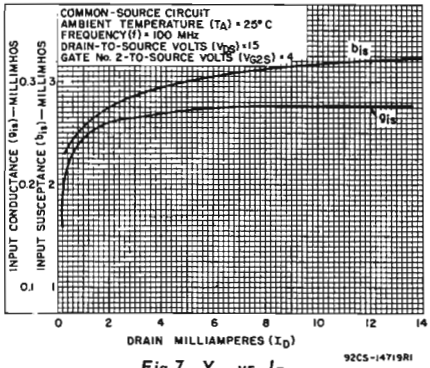


Fig.7 - Y_{is} vs. I_D

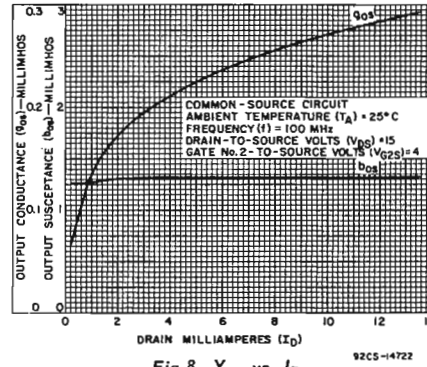


Fig.8 - Y_{os} vs. I_D

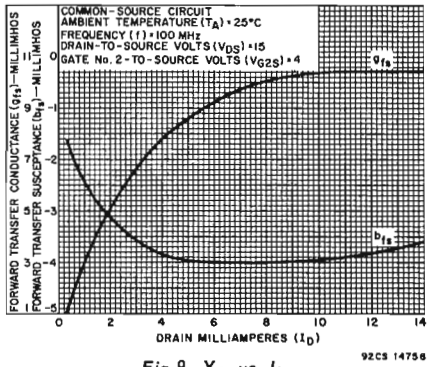


Fig.9 - Y_{fs} vs. I_D

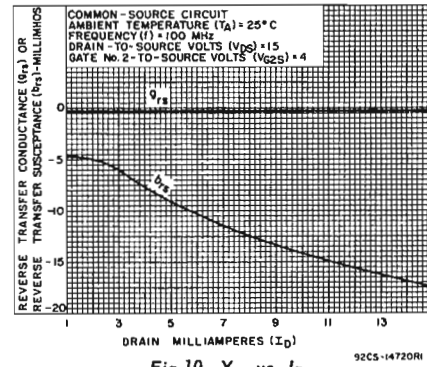
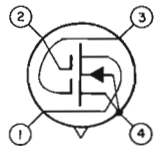


Fig.10 - Y_{rs} vs. I_D

TERMINAL DIAGRAM



Lead 1 — Drain
Lead 2 — Gate No. 2
Lead 3 — Gate No. 1
Lead 4 — Source, Substrate and Case

RCA Solid State Division

MOS Field-Effect Transistors

40673

RCA-40673 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS* pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 40673 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-40673 make it useful for a wide variety of rf-amplifier applications at frequencies up to 400 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two gate arrangement of the 40673 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 40673 is hermetically sealed in the metal JEDEC TO-72 package.

*Metal-Oxide-Semiconductor.

Maximum Ratings, *Absolute-Maximum Values, at T_A = 25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +1	V
Peak ac	-6 to +6	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
DRAIN CURRENT, I_D	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
above 25°C	derate linearly at 2.2 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances ≥ 1/32 inch from seating surface for 10 seconds max.	265	°C

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTOR

N-Channel Depletion Type With Integrated Gate-Protection Circuits For RF Amplifier Applications up to 400 MHz

JEDEC TO-72

APPLICATIONS

- RF amplifier, mixer, and IF amplifier in military, industrial, and consumer communications equipment
- aircraft and marine vehicular receivers
- CATV and MATV equipment
- telemetry and multiplex equipment

PERFORMANCE FEATURES

- superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- wide dynamic range permits large-signal handling before overload
- dual-gate permits simplified agc circuitry
- virtually no agc power required
- greatly reduces spurious responses in fm receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability

DEVICE FEATURES

- back-to-back diodes protect each gate against handling and in-circuit transients
- low gate leakage currents —— I_{G1SS} & I_{G2SS} = 20 nA(max.) at T_A = 25°C
- high forward transconductance —— g_{fs} = 12,000 μmho (typ.)
- high unneutralized RF power gain —— G_{ps} = 18 dB(typ.) at 200 MHz
- low VHF noise figure —— 3.5 dB(typ.) at 200 MHz

ELECTRICAL CHARACTERISTICS, at T_A = 25°C unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Gate-No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15V, I_D = 200μA V_{G2S} = +4V	–	–2	–4	V
Gate-No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15V, I_D = 200μA V_{G1S} = 0	–	–2	–4	V
Gate-No.1-Leakage Current	I_{G1SS}	V_{G1S} = +1 or–6 V V_{DS} = 0, V_{G2S} = 0	–	–	50	nA
Gate-No.2-Leakage Current	I_{G2SS}	V_{G2S} = ±6V V_{DS} = 0, V_{G1S} = 0	–	–	50	nA
Zero-Bias Drain Current	I_{DSS}	V_{DS} = +15V V_{G2S} = +4V V_{G1S} = 0	5	15	35	mA
Forward Transconductance (Gate-No.1-to-Drain)	g_{fs}	V_{DS} = +15V, I_D = 10mA V_{G2S} = +4V, f = 1kHz	–	12,000	–	μmho
Small-Signal, Short-Circuit Input Capacitance †	C_{iss}	V_{DS} = +15V, I_D = 10mA V_{G2S} = +4V, f=1MHz	–	6	–	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No.1) ♦	C_{rss}		0.005	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}		–	2.0	–	pF
Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15V, I_D = 10mA V_{G2S} = +4V, f = 200 MHz	14	18	–	dB
Maximum Available Power Gain	MAG		–	20	–	dB
Maximum Usable Power Gain (unneutralized)	MUG		–	20*	–	dB
Noise Figure (see Fig. 1)	NF		–	3.5	6.0	dB
Magnitude of Forward Transadmittance	$\lvert Y_{fs} \rvert$		–	12,000	–	μmho
Phase Angle of Forward Transadmittance	θ		–	–35	–	degrees
Input Resistance	r_{iss}		–	1.0	–	kΩ
Output Resistance	r_{oss}		–	2.8	–	kΩ
Protective Diode Knee Voltage	V_{knee}	$I_{DIODE(REVERSE)}$=±100μA	–	±10	–	V

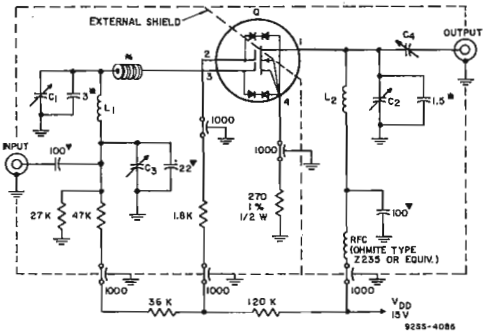
*Limited only by practical design considerations.

†Capacitance between Gate No. 1 and all other terminals

♦Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.

OPERATING CONSIDERATIONS

The flexible leads of the 40673 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.



#Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness.

All resistors in ohms

All capacitors in pF

Q = 40673
▼ Disc ceramic.
*Tubular ceramic.

C_1: 1.8 – 8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.

C_2: 1.5 – 5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.

C_3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.80 in.

L_2: 4½ turns silver-plated 0.02-in. thick, 0.085-0.095-in. wide, 5/16-in. ID. Coil ≈ .90 in. long.

Fig. 1. 200-MHz Power gain and noise-figure test circuit

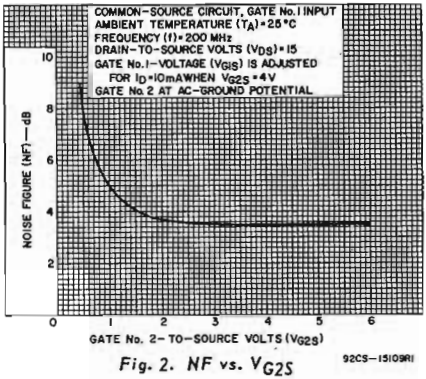


Fig. 2. NF vs. V_{G2S}

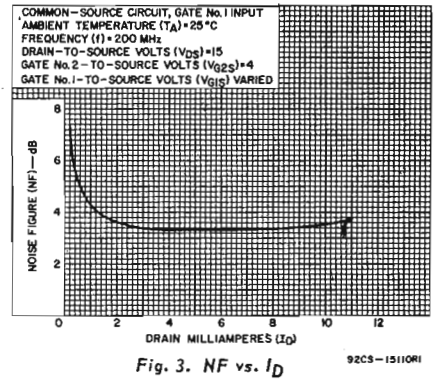


Fig. 3. NF vs. I_D

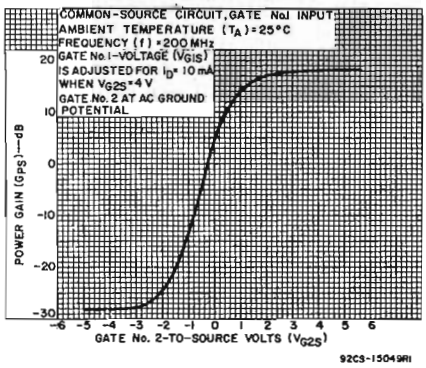


Fig. 4. G_{PS} vs. V_{G2S}

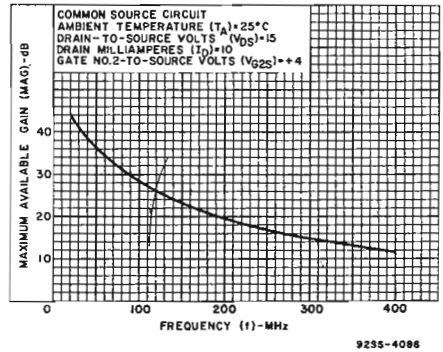


Fig. 5. MAG. vs. f

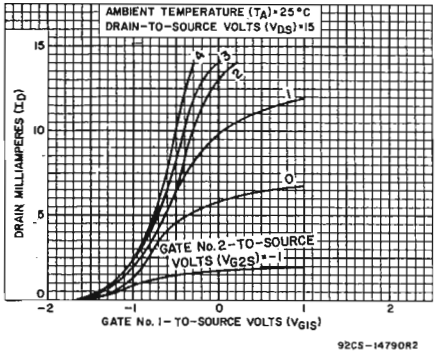


Fig. 6. I_D vs. V_{G1S}

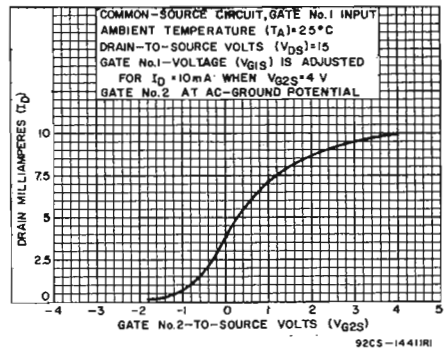


Fig. 7. I_D vs. V_{G2S}

Typical y Parameters vs. V_{DS}

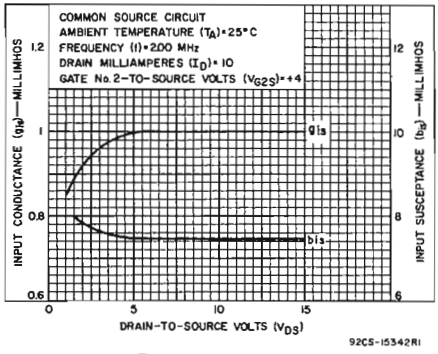


Fig. 8. y_{is} vs. V_{DS}

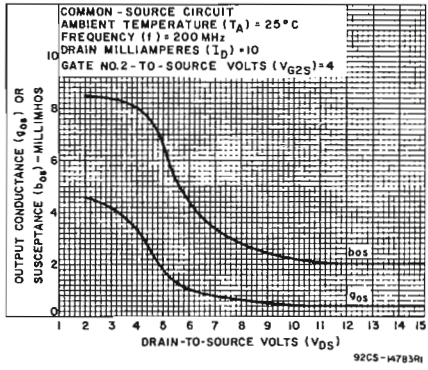


Fig. 9. y_{os} vs. V_{DS}

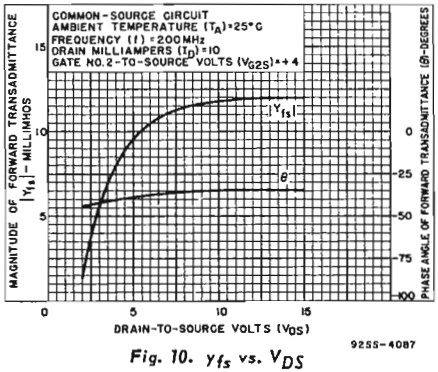


Fig. 10. y_{fs} vs. V_{DS}

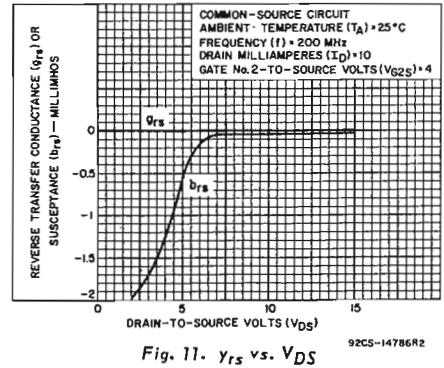


Fig. 11. y_{rs} vs. V_{DS}

Typical y Parameters vs. I_D

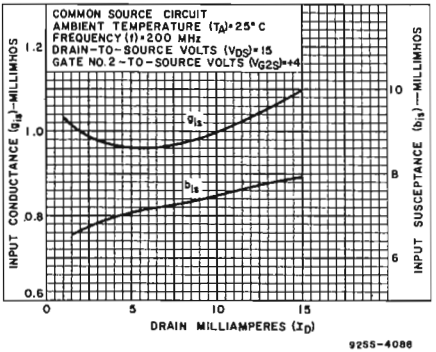


Fig. 12. y_{is} vs. I_D

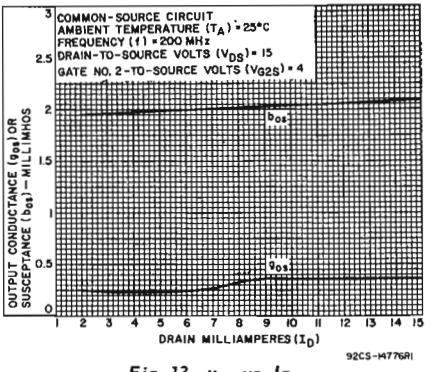


Fig. 13. y_{os} vs. I_D

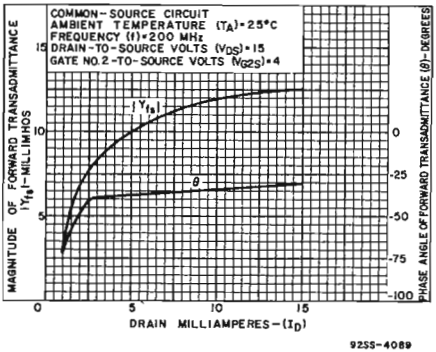


Fig. 14. y_{fs} vs. I_D

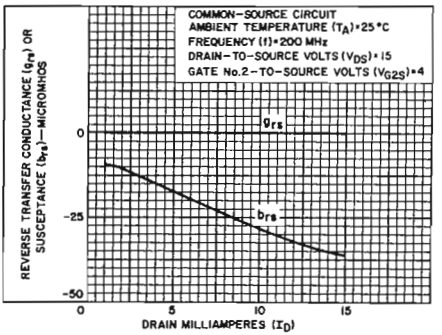


Fig. 15. y_{rs} vs. I_D

Typical y Parameters vs. V_{G2S}

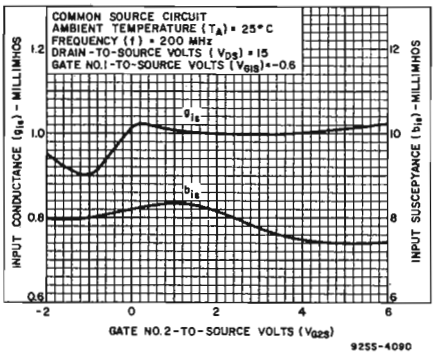


Fig. 16. y_{is} vs. V_{G2S}

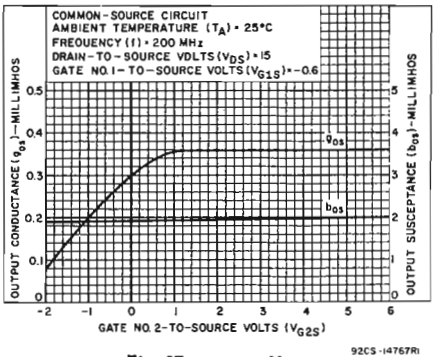


Fig. 17. y_{os} vs. V_{G2S}

Typical y Parameters vs. V_{G2S} (Cont'd)

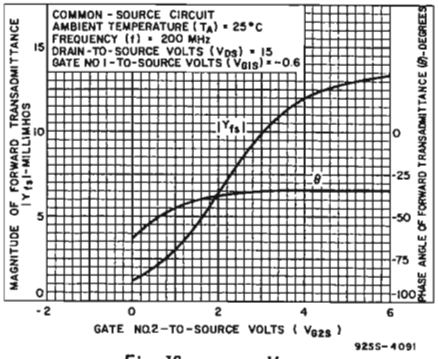


Fig. 18. y_{fs} vs. V_{G2S}

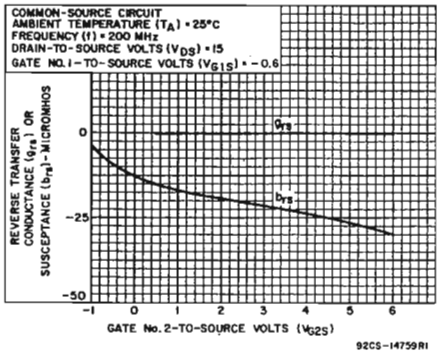


Fig. 19. y_{rs} vs. V_{G2S}

Typical y Parameters vs. Frequency

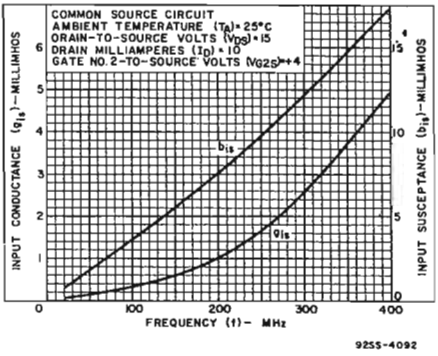


Fig. 20. y_{is} vs. frequency

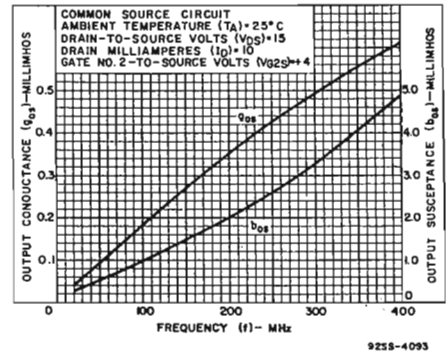


Fig. 21. y_{os} vs. frequency

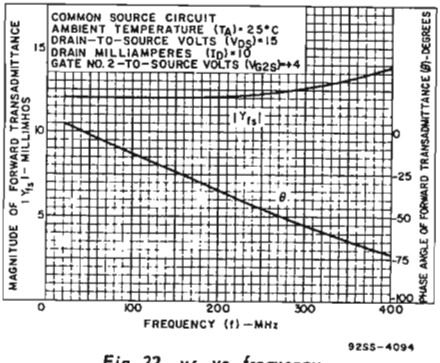


Fig. 22. y_{fs} vs. frequency

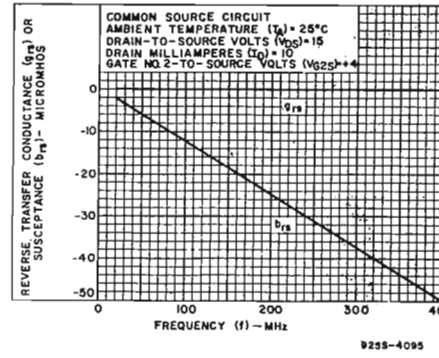


Fig. 23. y_{rs} vs. frequency

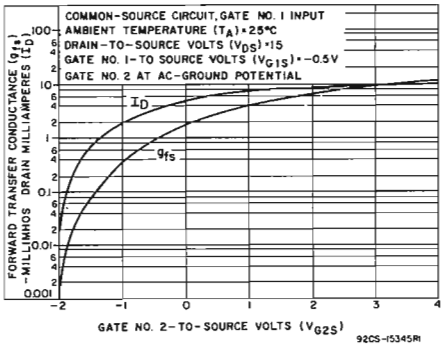


Fig. 24. g_{fs} and I_D vs. V_{G2S}

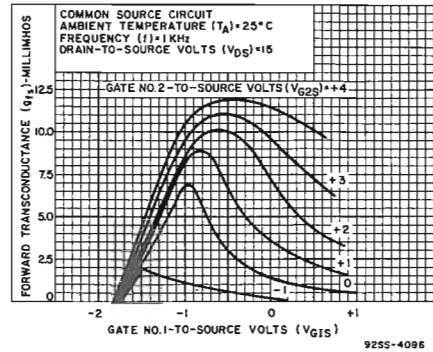


Fig. 25. g_{fs} vs. V_{G1S}

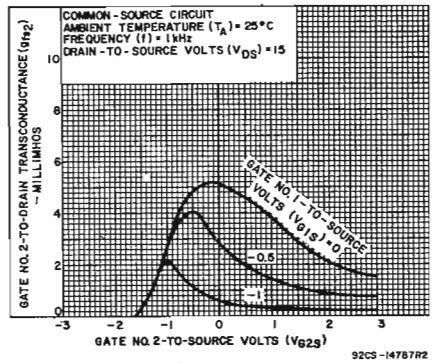
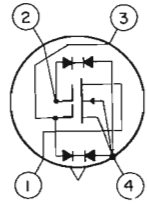


Fig. 26. g_{fs_2} vs. V_{G2S}

TERMINAL DIAGRAM



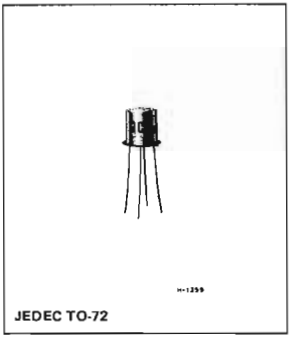
LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

RCA Solid State Division

MOS Field-Effect Transistors

N-Channel Depletion Type

40819



JEDEC TO-72

Silicon Dual-Insulated-Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits

For RF Amplifier Applications up to 250 MHz

Device Features

- back-to-back diodes protect each gate against handling and in-circuit transients
- high forward transconductance: g_{fs} = 12,000 μmho (typ.)
- high unneutralized RF power gain: G_{ps} = 18 dB (typ.) at 200 MHz
- low VHF noise figure: 3.5 dB (typ.) at 200 MHz
- low gate leakage currents: I_{G1SS} & I_{G2SS} = 50 nA at T_A = 25° C
- increased drain-to-source voltage rating: V_{DS} = −0.2 to +25 V

RCA-40819 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor (FET).

The excellent overall performance characteristics of the RCA-40819 make it useful for a wide variety of rf-amplifier applications at frequencies up to 250 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 40819 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac grounding Gate No.2. The reduced capacitance allows operation at maximum gain *without neutralization* and reduces local oscillator feedthrough to the antenna — features of special importance in rf and if amplifiers.

Special back-to-back diodes are diffused directly into the MOS* pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts and protect the gates against damage in all normal handling and usage.

The back-to-back diode configuration permits the 40819 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

Applications

- RF amplifier, mixer, and IF amplifier in military, industrial, and consumer communications equipment
- aircraft and marine vehicular receivers
- CATV and MATV equipment
- telemetry and multiplex equipment

Performance Features

- superior cross-modulation performance and greater dynamic range than bipoler or single-gate FET s
- wide dynamic range permits large-signal handling before overload
- virtually no agc power required
- greatly reduces spurious responses in FM receivers
- dual gate permits simplified AGC circuitry

The 25-volt drain-to-source rating permits the use of higher voltage power supplies.

The 40819 is hermtically sealed in the metal JEDEC TO-72 package.

*Metal-Oxide-Semiconductor

Maximum Ratings

Continuous Working Voltage#, at T_A = 25°C:

Gate No.1-to-Source Voltage, V_{G1S}	−6 to +3	V
Gate No.2-to-Source Voltage, V_{G2S}	−6 to +6 or 40% of V_{DS} (whichever value is less)	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+25	V

#Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the absolute Maximum Ratings are not exceeded.

Absolute Maximum Values, at T_A = 25°C:

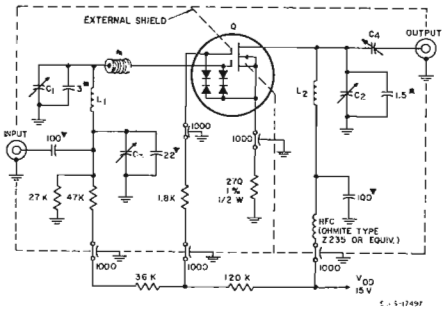
Drain-to-Source Voltage, V_{DS}	−0.2 to +25	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	μA
Drain-to-Gate Voltege, V_{DG1} or V_{DG2}	+31	V
Drain Current, I_D	50	mA
Transistor Dissipation, P_T:		
At T_A up to 25°C	330	mW
At T_A above 25°C	derate linearly 2.2	mW/°C
Ambient Temperature Range:		
Operating and Storage	−65 to +175	°C
Lead Temperature (During Soldering):		
At distances 1/32 in from seating surface for 10 s max.	265	°C

ELECTRICAL CHARACTERISTICS, at T_A = 25° C unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Gate-No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 200 μA, V_{G2S} = +4 V	–	−2	−4	V
Gate-No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 200 μA, V_{G1S} = 0	–	−2	−4	V
Gate-No.1-Leakage Current	I_{G1SS}	V_{G1S} = ± 6 V, V_{DS} = 0, V_{G2S} = 0	–	–	50	nA
Gate-No.2-Leakage Current	I_{G2SS}	V_{G2S} = ± 6 V, V_{DS} = 0, V_{G1S} = 0	–	–	50	nA
Zero-Bias Drain Current	I_{DSS}	V_{DS} = + 15 V, V_{G2S} = +4 V, V_{G1S} = 0	5	15	35	mA
Forward Transconductance (Gate-No.1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 kHz	–	12,000	–	μmho
Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 MHz	–	6	–	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No.1)♦	C_{rss}		0.005	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}		–	2	–	pF
Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V, f = 200 MHz	14	18	–	dB
Maximum Available Power Gain	MAG		–	20	–	dB
Maximum Usable Power Gain (unneutralized)	MUG		–	20*	–	dB
Noise Figure (see Fig. 1)	NF		–	3.5	6.0	dB
Magnitude of Forward Transedmittance	$\|Y_{fs}\|$		–	12,000	–	μmho
Phase Angle of Forward Transadmittance	θ		–	−35	–	degrees
Input Resistance	r_{iss}		–	1	–	kΩ
Output Resistance	r_{oss}		–	2.8	–	kΩ
Protective Diode Knee Voltage	V_{knee}	I_{diode} (reverse) = ±100 μA	–	±10	–	V

* Limited only by practical design considerations. † Capacitance between Gate No.1 and all other terminals.

♦ Three-terminal measurement with Gate No.2 and Source returned to guard terminal.



#Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in OD; 0.03 in ID; 0.063 in thickness.

Q = 40673

▼ Disc ceramic.

* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1: 1.8 – 8.7 pF variable air capacitor: E. F. Johnson Type 160-104, or equivalent.

C_2: 1.5 – 5 pF variable air capacitor: E. F. Johnson Type 160-102, or equivalent.

C_3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in thick, 0.075-0.085 in wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.80 in.

L_2: 4-1/2 turns silver-plated 0.02 in thick, 0.085-0.095-in wide, 5/16-in; ID Coil = .90 in long.

Fig. 1. 200 MHz power gain and noise figure test circuit

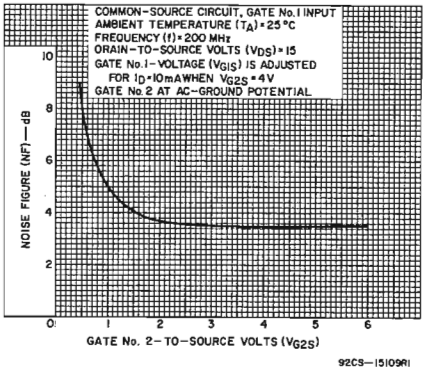


Fig. 2. NF vs. V_{G2S}

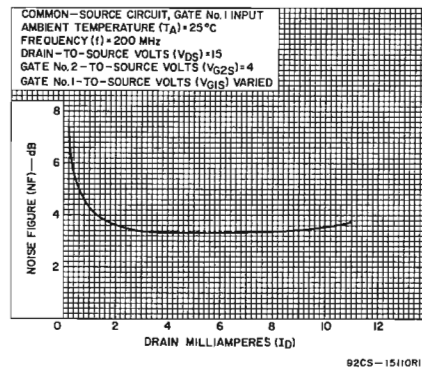


Fig. 3. NF vs. I_D

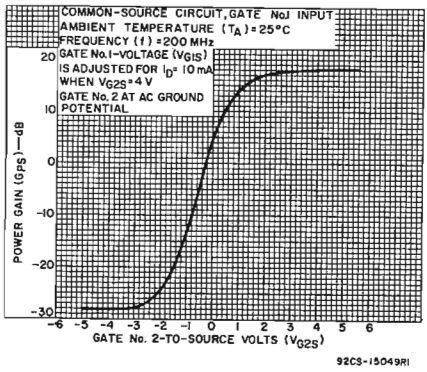


Fig. 4. G_{PS} vs. V_{G2S}

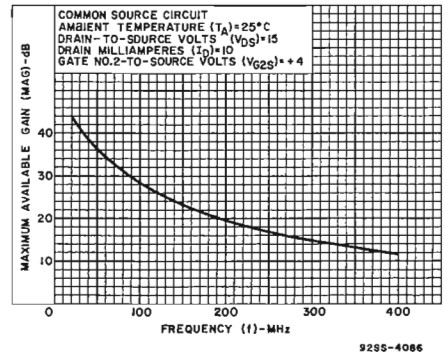


Fig. 5. MAG vs. f

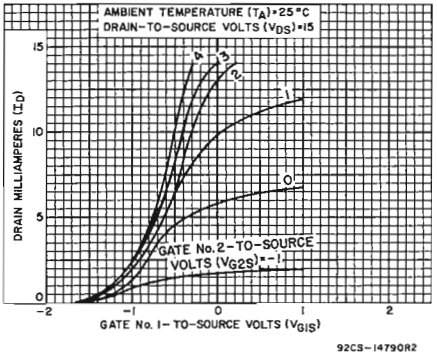


Fig. 6. I_D vs. V_{G1S}

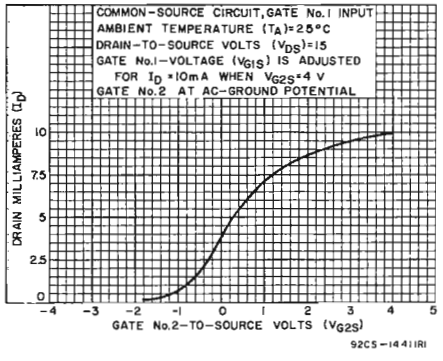


Fig. 7. I_D vs. V_{G2S}

Typical y Parameters vs. V_{DS}

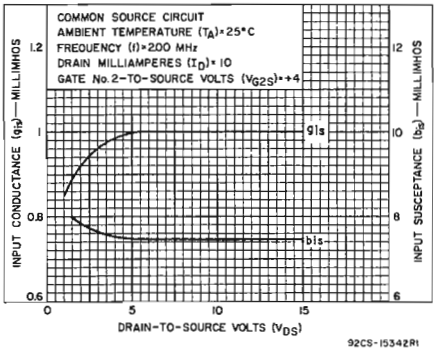


Fig. 8. y_{is} vs. V_{DS}

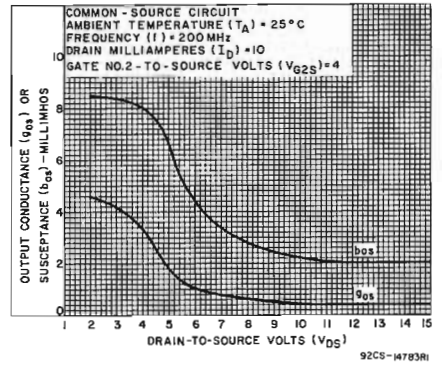


Fig. 9. y_{os} vs. V_{DS}

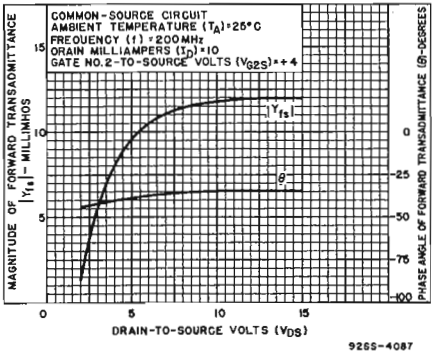


Fig. 10. y_{fs} vs. V_{DS}

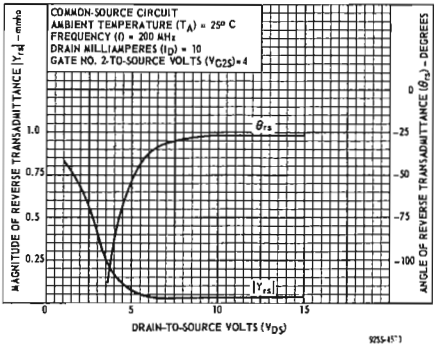


Fig. 11. y_{rs} vs. V_{DS}

Typical y Parameters vs. I_D

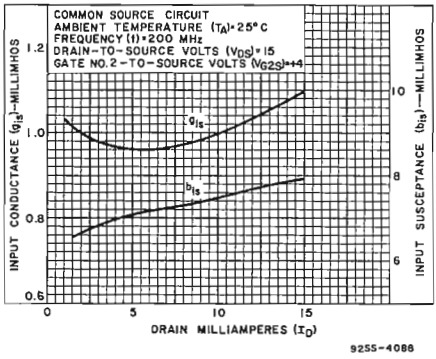


Fig. 12. y_{is} vs. I_D

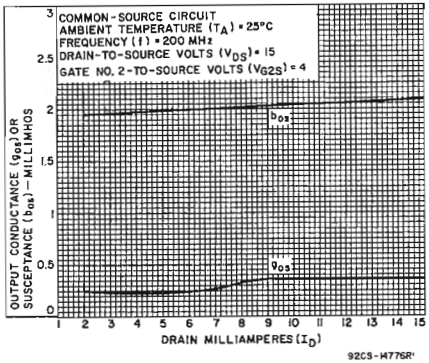


Fig. 13. y_{os} vs. I_D

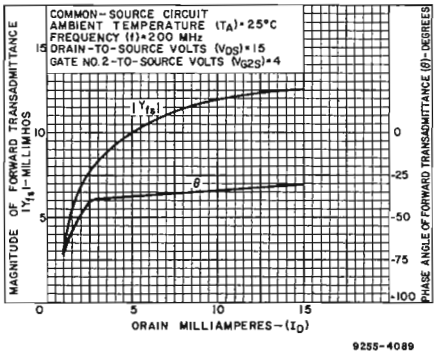


Fig. 14. y_{fs} vs. I_D

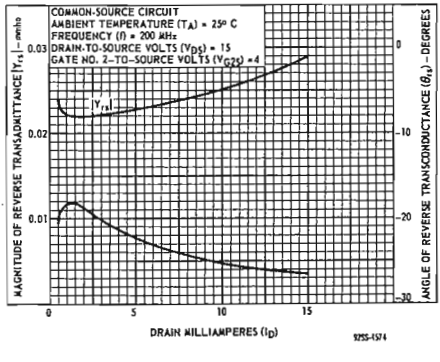


Fig. 15. y_{rs} vs. I_D

Typical y Parameters vs. V_{G2S}

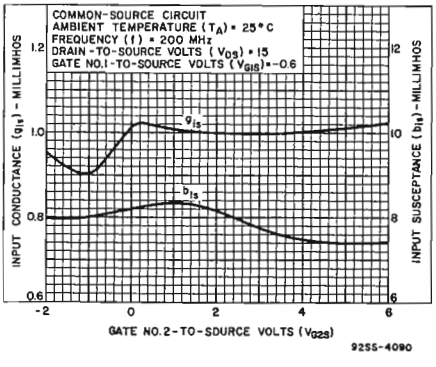


Fig. 16. y_{is} vs. V_{G2S}

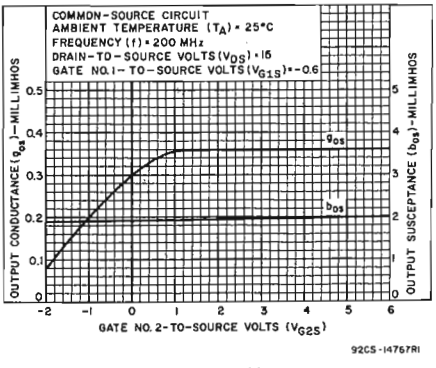


Fig. 17. y_{os} vs. V_{G2S}

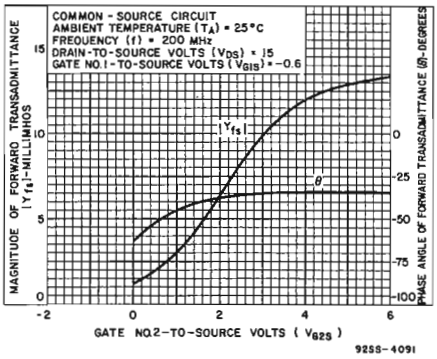


Fig. 18. y_{fs} vs. V_{G2S}

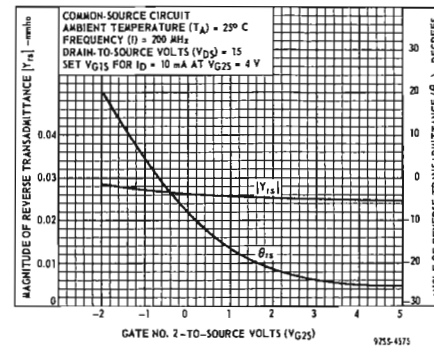


Fig. 19. y_{rs} vs. V_{G2S}

Typical y Parameters vs. Frequency

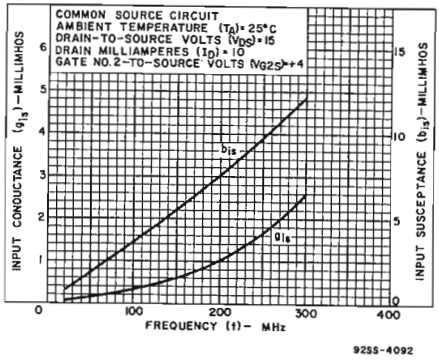


Fig. 20. y_{is} vs. frequency

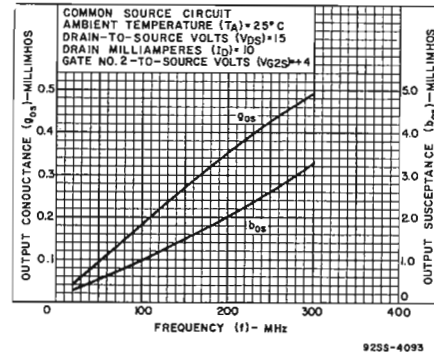


Fig. 21. y_{os} vs. frequency

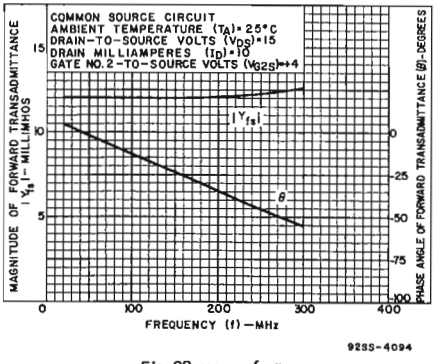


Fig. 22. y_{fs} vs. frequency

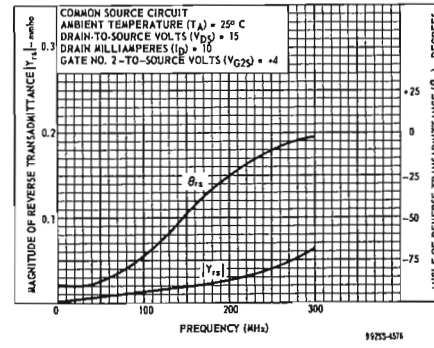


Fig. 23. y_{rs} vs. frequency

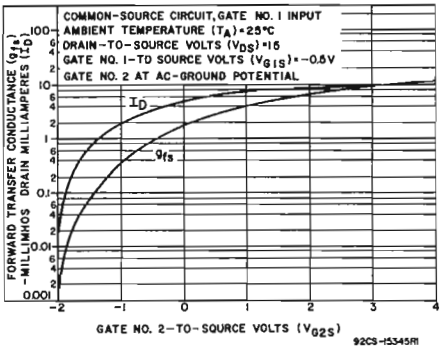


Fig. 24 g_{fs} and I_D vs. V_{G2S}

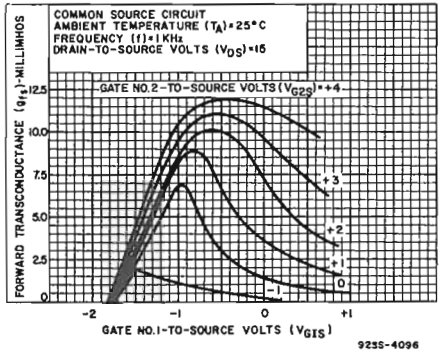


Fig. 25. g_{fs} vs. V_{G1S}

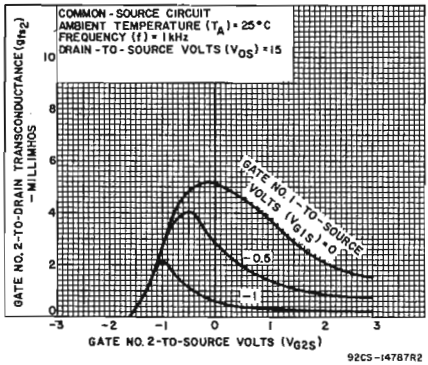
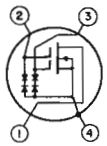


Fig. 26. g_{fs2} vs. V_{G2S}

OPERATING CONSIDERATIONS

The flexible leads of the 40819 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.

TERMINAL DIAGRAM



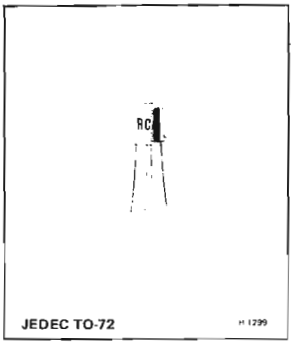
LEAD 1 - DRAIN
LEAD 2 - GATE No.2
LEAD 3 - GATE No.1
LEAD 4 - SOURCE, SUBSTRATE, AND CASE

RCA
Solid State
Division

MOS Field-Effect Transistors

N-Channel Depletion Types

40820—40821



Silicon Dual-Insulated-Gate Field-Effect Transistors

With Integrated Gate-Protection Circuits
For VHF-TV Tuner Applications

40820 – RF Amplifier 40821 – Mixer

Device Features

- back-to-back diodes protect each gate against handling and in-circuit transients
- high forward transconductance: g_{fs} = 12,000 μmho (typ.)
- high unneutralized RF power gain: G_{ps} = 17 dB (typ.) at 200 MHz (40820)
- low VHF noise figure: 3.5 dB (typ.) at 200 MHz (40820)
- low gate leakage currents: I_{G1SS} & I_{G2SS} = 50 nA

RCA-40820 and 40821 are n-channel silicon, depletion type, dual-insulated-gate, MOS▲ field-effect transistors for RF amplifier (40820) and mixer (40821) applications in VHF-TV receivers and other commercial equipment operating at frequencies up to 250 MHz.

These devices designed for VHF performance, provide excellent power gain, low-noise figures and have wide dynamic range. The dual-gate feature offers good cross-modulation performance over the AGC range and reduces feedback capacitance by shielding Gate No. 1 from the drain. The very low feedback capacitance also eliminates the need for circuit neutralization and reduces local oscillator feed-through to the antenna.

Virtually no AGC power is required because of the high gate input resistance of the MOS FET types. Automatic AGC delay can be achieved with a very slight change in the input impedance by the application of AGC voltage to Gate No. 2.

▲ Metal-Oxide-Semiconductor.

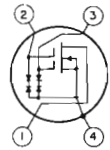
Performance Features

- superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- wide dynamic range permits large-signal handling before overload
- virtually no agc power required
- dual gate permits simplified AGC circuitry

The dual-gate arrangement also makes it possible to isolate the local oscillator signal from the incoming signal by applying each signal to a separate gate.

Integral back-to-back diodes protect the gates against damage in normal handling and usage by limiting transient voltages that exceed ±10 volts. The 40820 and 40821 are hermetically sealed in metal JEDEC TO-72 packages.

TERMINAL DIAGRAM



LEAD 1 – DRAIN
LEAD 2 – GATE No.2
LEAD 3 – GATE No.1
LEAD 4 – SOURCE, SUBSTRATE, AND CASE

Maximum Ratings	40820	40821	
Continuous Working Voltage#, at T_A = 25°C:			
Gate No. 1-to-Source Voltage, V_{G1S}	−6 to +3	−4.5 to +3	V
Gate No. 2-to-Source Voltage, V_{G2S}	-6 to +6 or 40% of V_{DS} (whichever value is less)	-4.5 to +4.5 or -4.5 to 40% of V_{DS} (whichever value is less)	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+20	+20	V
Absolute Maximum Values, at T_A = 25°C:			
Drain-to-Source Voltage, V_{DS}	−0.2 to +20	−0.2 to +20	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+26	+24.5	V
Drain Current, I_D	50	50	mA
Transistor Dissipation:			
At T_A up to 25°C	330	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C		
Ambient Temperature Range:			
Operating and Storage	−65 to +175	−65 to +175	°C
Lead Temperature (During Soldering):			
At distances 1/32 in from seating surface for 10 s max.	265	265	°C

Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the Absolute Maximum Ratings are not exceeded.

TYPICAL CHARACTERISTICS

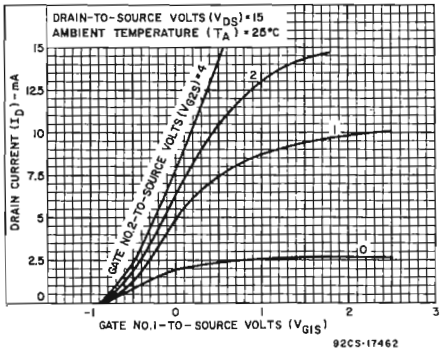


Fig.1 — I_D vs. V_{G1S} for types 40820 and 40821.

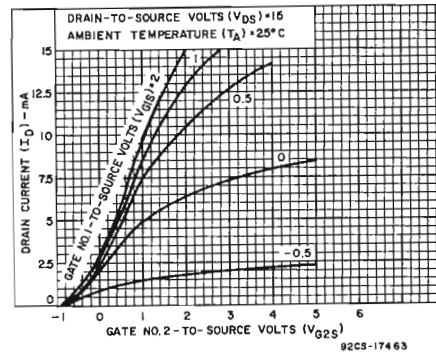


Fig.2 — I_D vs. V_{G2S} for types 40820 and 40821.

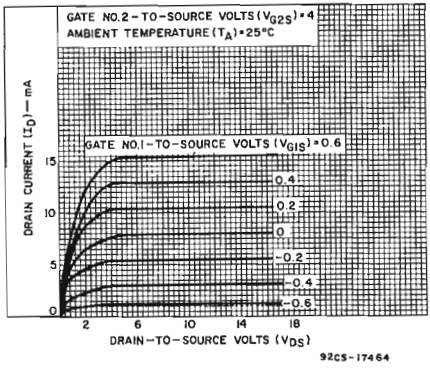


Fig.3 — I_D vs. V_{DS} for types 40820 and 40821.

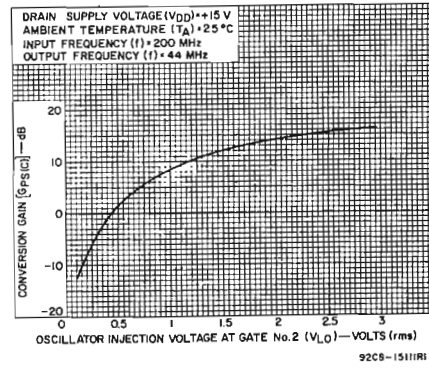


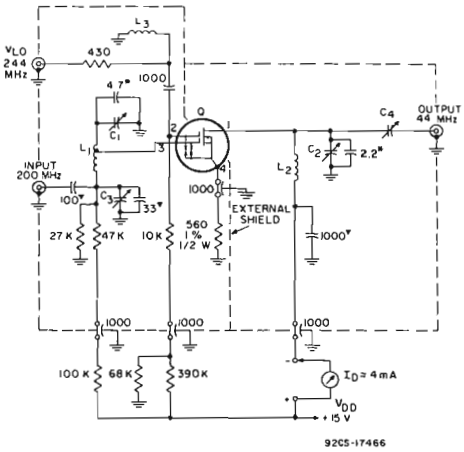
Fig.4 — $G_{PS(C)}$ vs. V_{LO} for type 40821.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS 40820 Min.	40820 Typ.	40820 Max.	40821 Min.	40821 Typ.	40821 Max.	UNITS
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS}= +15V, I_D=200μA, V_{G2S}= +4V		–	–1	–3	–	–1	–3	V
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS}= +15V, I_D=200μA, V_{G1S}=0		–	–1	–3	–	–1	–3	V
Gate-to-Source Forward Breakdown Voltage Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} I_{G2SSF} 100 μA	V_{G2S} V_{DS} 0	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} V_{DS} 0	–	9	–	–	11	–	V
Gate-to-Source Reverse Breakdown Voltage Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} I_{G2SSR} 100 μA	V_{G2S} V_{DS} 0	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} V_{DS} 0	–	9	–	–	11	–	V
Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{DS} V_{G2S} 0	V_{G1S} 6 V	–	–	50	–	–	–	nA
			V_{G1S} 4.5 V	–	–	–	–	–	50	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{DS} V_{G2S} 0	V_{G1S} 6 V	–	–	50	–	–	–	nA
			V_{G1S} -4.5 V	–	–	–	–	–	50	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{DS} V_{G1S} 0	V_{G2S} 6 V	–	–	50	–	–	–	nA
			V_{G2S} 4.5 V	–	–	–	–	–	50	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{DS} V_{G1S} 0	V_{G2S} -6 V	–	–	50	–	–	–	nA
			V_{G2S} 4.5 V	–	–	–	–	–	50	nA
Zero-Bias Drain Current	I_{DS}	V_{DS} +15 V, V_{G1S} 0, V_{G2S} +4 V		0.5	8	15	0.5	8	20	mA
Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} +15 V I_D 10 mA V_{G2S} +4 V	f 1 kHz	–	12000	–	–	12000	–	μmho
Small-Signal, Short-Circuit Input Capacitance♦	C_{iss}		f 1 MHz	–	6	8.5	–	6	9	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦	C_{rss}			0.005	0.02	0.03	0.005	0.02	0.04	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2	–	–	2	–	pF
Power Gain (see Fig. 6)	G_{PS}		f 200 MHz	14	17	–	–	–	–	dB
Noise Figure (see Fig. 6)	NF			–	4.5	6	–	–	–	dB
Conversion Gain	$G_{PS(C)}$		f 200/44 MHz	–	–	–	11	–	–	dB

♦ Capacitance between Gate No. 1 and all other terminals.

♠ Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.



Q = 40821
▼Disc. ceramic.
* Tubular ceramic.
All resistors in ohms
All capacitors in pF

C_1, C_2: 1.5–5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.9–7 pF compression-type capacitor: ARCO 400 or equivalent.

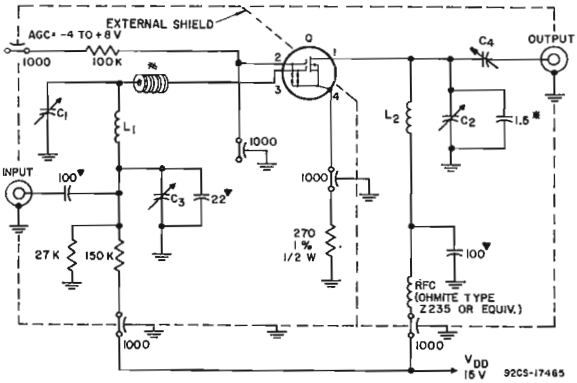
L_1: 5 turns silver-plated 0.02" thick, 0.07"–0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Ohmite Z-235 RF choke or equivalent

L_3: J. W. Miller Co. #4580 0.1 μH RF choke or equivalent.

Note: If 50Ω meter is used in place of sweep detector, a low pass filter must be provided to eliminate local oscillator voltage from load.

Fig. 5 – Conversion power gain test circuit for type 40821.



#Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in OD; 0.03 in ID; 0.063 in thickness.

Q = 40820
▼ Disc ceramic.
* Tubular ceramic.

All resistors in ohms
All capacitors in pF

C_1: 1.8 – 8.7 pF variable air capacitor: E. F. Johnson Type 160-104, or equivalent.

C_2: 1.5 – 5 pF variable air capacitor: E. F. Johnson Type 160-102, or equivalent.

C_3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in thick, 0.075-0.085 in wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.80 in.

L_2: 4-1/2 turns silver-plated 0.02 in thick, 0.085-0.095 in wide, 5/16-in; ID Coil ≈0.90 in. long.

Fig. 6 – 200 MHz power gain and noise figure test circuit for type 40820.

Table 1 – y parameters vs. frequency

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz) 50	100	200	250	UNITS
Y Parameters						
Input Conductance	g_{is}	0.08	0.33	1.0	1.6	mmho
Input Susceptance	b_{is}	1.8	3.6	7.5	9.8	mmho
Magnitude Forward Transadmittance	$\lvert y_{fs}\rvert$	12	12	12	12.3	mmho
Angle of Forward Transadmittance	$<y_{fs}$	–2	–13	–35	–45	degrees
Output Conductance	g_{os}	0.10	0.18	0.36	0.42	mmho
Output Susceptance	b_{os}	0.5	1.0	2.0	2.6	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs}\rvert$	8	12	25	40	μmho
Angle of Reverse Transadmittance	$<y_{rs}$	–88	–73	–25	–10	degrees

TEST CONDITIONS: Drain-to-Source Volts (V_{DS}) = 15, Drain Milliamperes (I_D) = 10, Gate No.2-to-Source Volts (V_{G2S}) = 4

TYPICAL CHARACTERISTICS

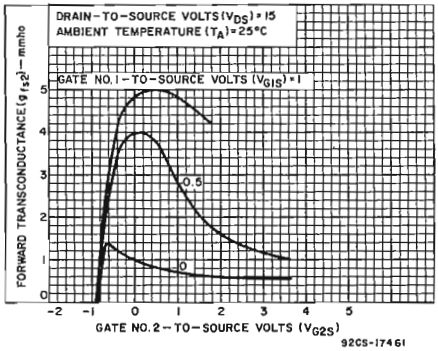


Fig. 7 — g_{fs} vs. V_{G2S} for types 40820 and 40821.

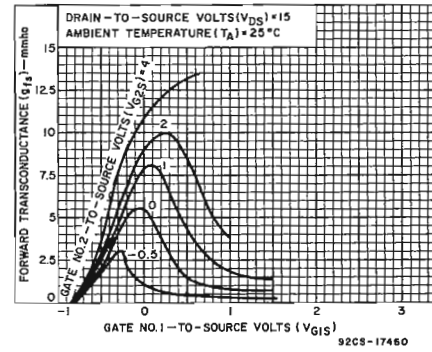


Fig. 8 — g_{fs} vs. V_{G1S} for types 40820 and 40821.

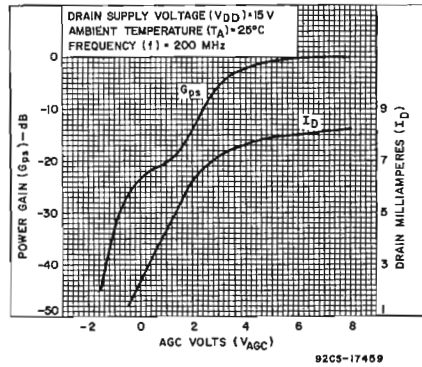


Fig. 9 — G_{PS} vs. V_{AGC} for type 40820.

OPERATING CONSIDERATIONS

The flexible leads of the 40820 and 40821 are usually soldered to the circuit elements. As is the case with any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.

TYPICAL y PARAMETERS

y parameters vs. V_{DS}

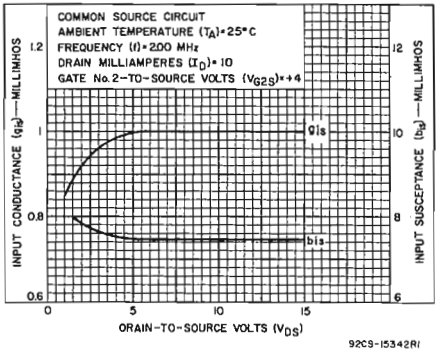


Fig. 10 – y_{is} vs. V_{DS}

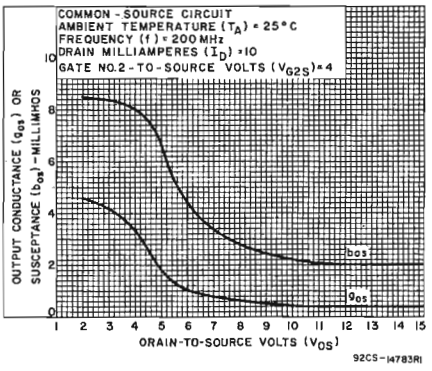


Fig. 11 – y_{os} vs. V_{DS}

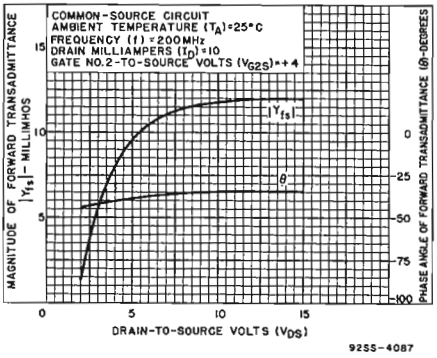


Fig. 12 – y_{fs} vs. V_{DS}

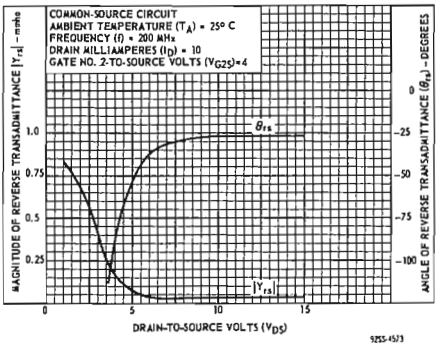


Fig. 13 – y_{rs} vs. V_{DS}

y parameters vs. I_D

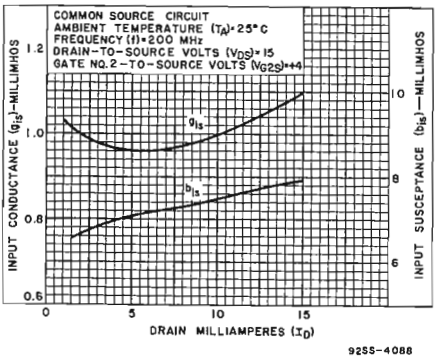


Fig. 14 – y_{is} vs. I_D

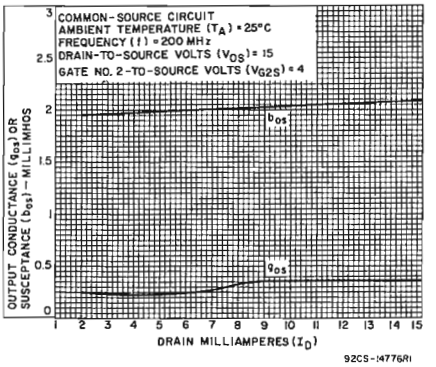


Fig. 15 – y_{os} vs. I_D

TYPICAL y PARAMETERS

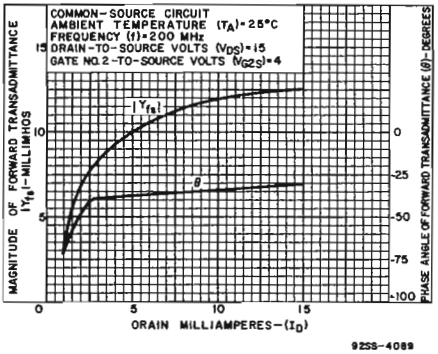


Fig. 16 – y_{fs} vs. I_D

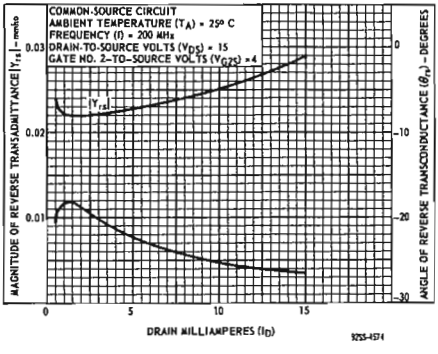


Fig. 17 – y_{rs} vs. I_D

y parameters vs. V_{G2S}

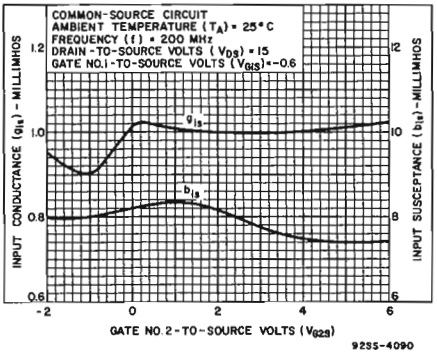


Fig. 18 – y_{is} vs. V_{G2S}

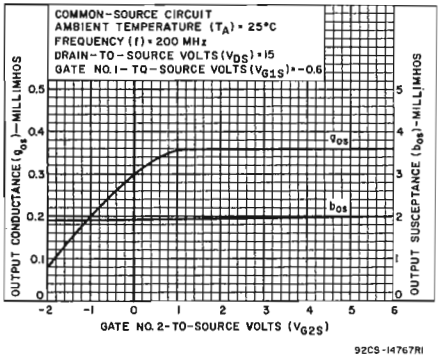


Fig. 19 – y_{os} vs. V_{G2S}

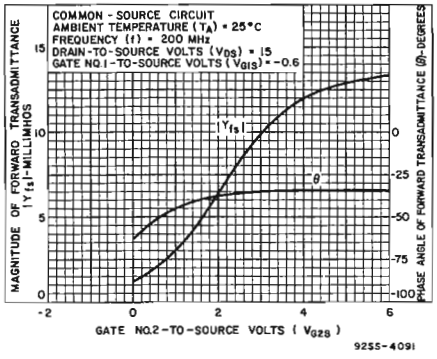


Fig. 20 – y_{fs} vs. V_{G2S}

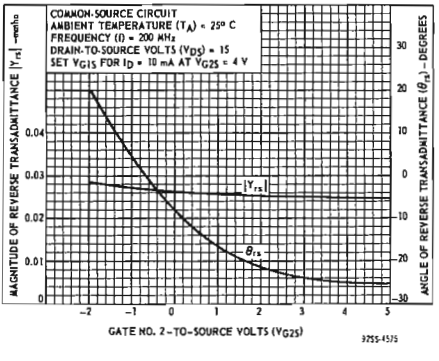


Fig. 21 – y_{rs} vs. V_{G2S}

RCA
Solid State
Division

MOS Field-Effect Transistors

N-Channel Depletion Types

40822-40823

JEDEC TO-72 H 1299

Silicon Dual-Insulated-Gate Field-Effect Transistors

With Integrated Gate-Protection Circuits

For FM Tuner Applications

40822 – RF Amplifier 40823 – Mixer

Device Features

- back-to-back diodes protect each gate against handling and in-circuit transients
- high forward transconductance: g_{fs} = 12,000 μmho (typ.)
- high unneutralized RF power gain: G_{ps} = 24 dB (typ.) at 100 MHz (40822)
- low VHF noise figure: 2 dB (typ.) at 100 MHz (40822)
- low gate leakage currents: I_{G1SS} & I_{G2SS} = 50 nA at T_A = 25°C

RCA-40822 and 40823 are n-channel silicon, depletion type, dual-insulated-gate, field-effect transistors for RF amplifier (40822) and mixer (40823) applications in FM receivers and other commercial equipment operating at frequencies up to 150 MHz.

These devices designed for VHF performance, provide excellent power gain, low-noise figures and have wide dynamic range. The dual-gate feature offers good cross-modulation performance over the AGC range and reduces feedback capacitance by shielding Gate No. 1 from the drain. The very low feedback capacitance also eliminates the need for circuit neutralization and reduces local oscillator feed-through to the antenna.

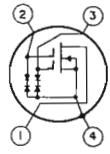
Virtually no power is required in AGC utilizing the 40822 and 40823. In addition, these devices minimize input impedance variations and automatically achieve AGC delay when AGC is applied to Gate No. 2. The dual-gate arrangement also makes it possible to isolate the local oscillator signal from the incoming signal by applying each signal to a specific gate.

Performance Features

- superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's
- wide dynamic range permits large-signal handling before overload
- virtually no agc power required
- greatly reduces spurious responses in FM receivers
- dual gate permits simplified AGC circuitry

Back-to-back diodes, diffused directly into the MOS pellet, protect the gates against damage in normal handling and usage by limiting transient voltages that exceed +10 volts. The 40822 and 40823 are hermetically sealed in metal JEDEC TO-72 packages.

TERMINAL DIAGRAM



LEAD 1 – DRAIN
LEAD 2 – GATE No.2
LEAD 3 – GATE No.1
LEAD 4 – SOURCE, SUBSTRATE AND CASE

Maximum Ratings

Continuous Working Voltage#, at T_A = 25°C:	40822	40823	
Gate No. 1-to-Source Voltage, V_{G1S}	−6 to +3	−4.5 to +3	V
Gate No. 2-to-Source Voltage, V_{G2S}	-6 to +6 or 40% of V_{DS} (whichever value is less)	-4.5 to +4.5 or 40% of V_{DS} (whichever value is less)	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+20	+20	V
Absolute Maximum Values, at T_A = 25°C:			
Drain-to-Source Voltage, V_{DS}	−0.2 to +18	−0.2 to +18	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+24	+22.5	V
Drain Current, I_D	50	50	mA
Transistor Dissipation:			
At T_A up to 25°C	330	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C		
Ambient Temperature Range:			
Operating and Storage	−65 to +175	−65 to +175	°C
Lead Temperature (During Soldering):			
At distances 1/32 in from seating surface for 10 s max.	265	265	°C

Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the Absolute Maximum Ratings are not exceeded.

TYPICAL CHARACTERISTICS FOR TYPES 40822 AND 40823

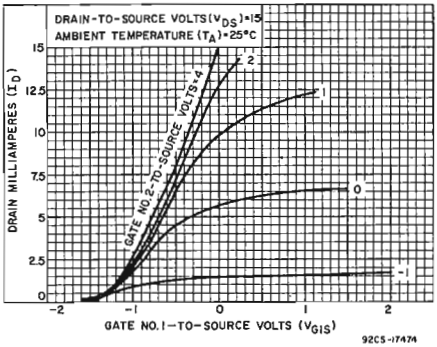


Fig. 1 - I_D vs. V_{G1S}

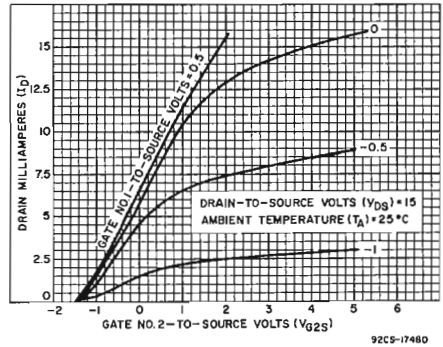


Fig. 2 - I_D vs. V_{G2S}

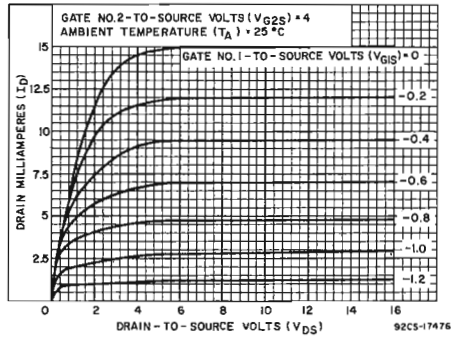


Fig. 3 - I_D vs. V_{DS}

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

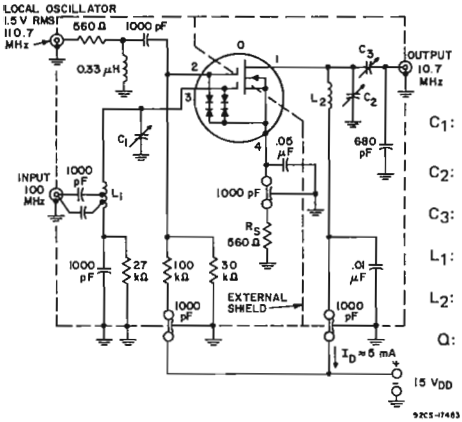
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS 40822 Min.	40822 Typ.	40822 Max.	40823 Min.	40823 Typ.	40823 Max.	UNITS
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS}= +15V, I_D=200μA, V_{G2S}= +4V		–	–2	–4	–	–2	–4	V
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS}= +15V, I_D=200μA, V_{G1S}=0		–	–2	–4	–	–2	–4	V
Gate-to-Source Forward Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	$V_{G2S} = V_{DS} = 0$	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSF}$		$V_{G1S} = V_{DS} = 0$	–	9	–	–	11	–	V
Gate-to-Source Reverse Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	$V_{G2S} = V_{DS} = 0$	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSR}$		$V_{G1S} = V_{DS} = 0$	–	9	–	–	11	–	V
Gate No. 1-Terminal Forward Current	I_{G1SSF}	$V_{DS} = V_{G2S} = 0$	V_{G1S} = 6 V	–	–	50	–	–	–	nA
			V_{G1S} = 4.5 V	–	–	–	–	–	50	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	$V_{DS} = V_{G2S} = 0$	V_{G1S} = –6 V	–	–	50	–	–	–	nA
			V_{G1S} = –4.5 V	–	–	–	–	–	50	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	$V_{DS} = V_{G1S} = 0$	V_{G2S} = 6 V	–	–	50	–	–	–	nA
			V_{G2S} = 4.5 V	–	–	–	–	–	50	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	$V_{DS} = V_{G1S} = 0$	V_{G2S} = –6 V	–	–	50	–	–	–	nA
			V_{G2S} = –4.5 V	–	–	–	–	–	50	nA
Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V, V_{G1S} = 0, V_{G2S} = +4 V		5	15	30	5	15	35	mA
Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V	f = 1 kHz	–	12000	–	–	12000	–	μmho
Small-Signal, Short-Circuit Input Capacitance †	C_{iss}		f = 1 MHz	–	6.5	9.5	–	6.5	10	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦	C_{rss}			0.005	0.020	0.030	0.005	0.025	0.045	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2	–	–	2	–	pF
Power Gain (see Fig. 5)	G_{PS}		f = 100 MHz	19	24	–	–	–	–	dB
Noise Figure (see Fig. 5)	NF			–	2	3.5	–	–	–	dB
Conversion Gain	$G_{PS(C)}$		f = 100 to 10.7 MHz	–	–	–	14	18	–	dB

† Capacitance between Gate No. 1 and all other terminals.

♦ Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.

OPERATING CONSIDERATIONS

The flexible leads of the 40820 and 40821 are usually soldered to the circuit elements. As is the case with any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.



C1: 1.3-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

C2: 2.7-19.6 pF variable air capacitor: E.F. Johnson Type 160-110 or equivalent.

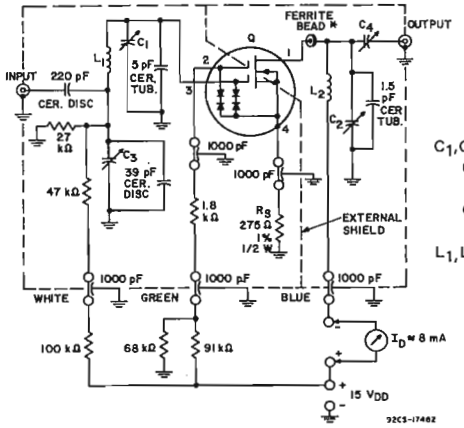
C3: 80 pF max. compression-type capacitor: Arco 405 or equivalent

L1: 8 turns No. 22 wire on 1/4" diameter air core. One turn spacing between windings. Tapped at one turn from low end.

L2: 37 turns No. 34 wire on 3/16" diameter air core. Unloaded Q = 63

Q: 40823.

Fig. 4 - 100/10.7-MHz conversion power gain test circuit for type 40823.



C_1, C_2: 1.3-5.4 pF variable air capacitor

C_3: 1-10 pF variable air capacitor, piston type: Johanson Co., No. 4335

C_4: 1-15 pF variable air capacitor, precision piston type: Roanwell Corp. SG11129/AG

L_1, L_2: 0.22 μH RF choke (7T): Miller, No. 4584

*Ferramic toroid (1/2 used): Indiana General, No. CF101-(0-6)

Fig. 5 - 100-MHz power gain and noise figure test circuit for type 40822.

TYPICAL CHARACTERISTICS FOR TYPES 40822 AND 40823

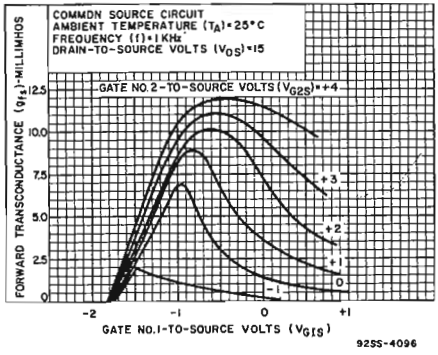


Fig. 6 - g_{fs} vs. V_{G1S}

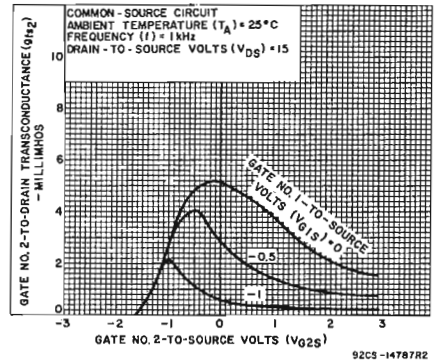


Fig. 7 - g_{fs2} vs. V_{G2S}

TYPICAL y PARAMETERS FOR TYPES 40822 and 40823

y Parameters vs. V_{DS}

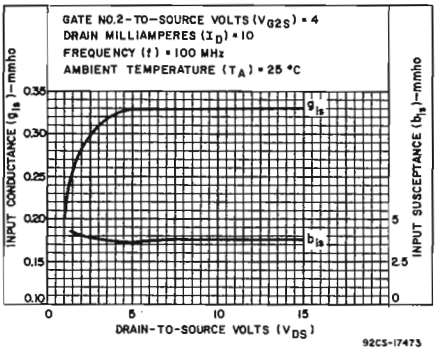


Fig. 8 - y_{is} vs. V_{DS}

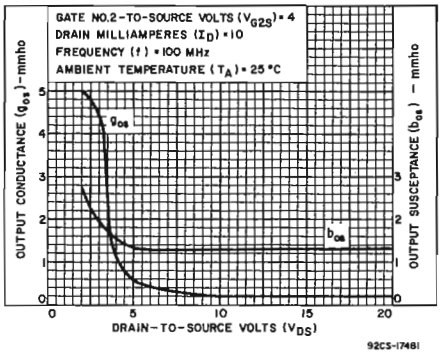


Fig. 9 - y_{os} vs. V_{DS}

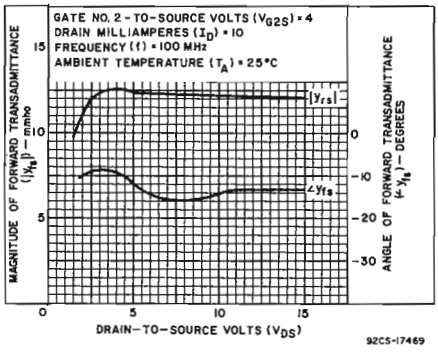


Fig. 10 - y_{fs} vs. V_{DS}

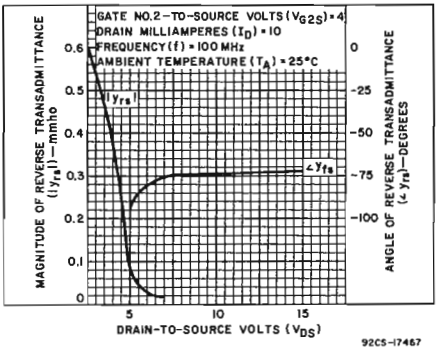


Fig. 11 - y_{rs} vs. V_{DS}

y Parameters vs. I_D

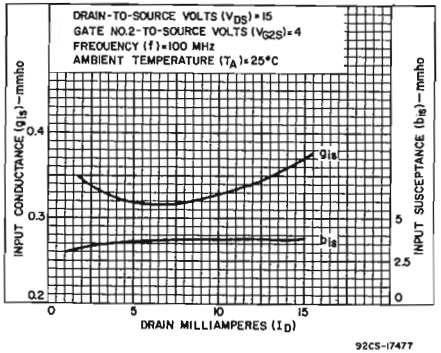


Fig. 12 - y_{is} vs. I_D

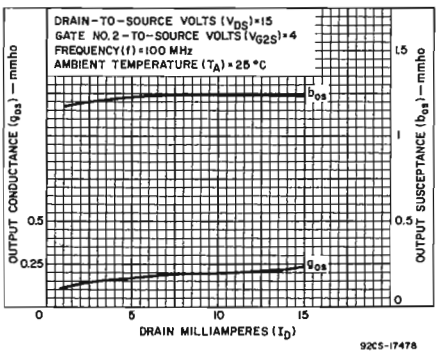


Fig. 13 - y_{os} vs. I_D

TYPICAL y PARAMETERS FOR TYPES 40822 and 40823

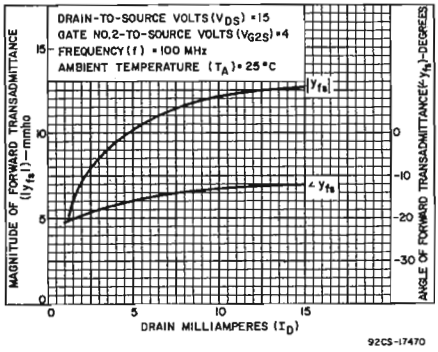


Fig. 14 - y_{fs} vs. I_D

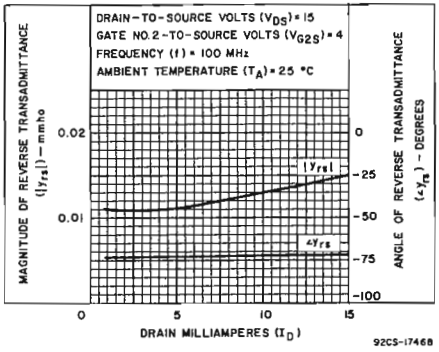


Fig. 15 - y_{rs} vs. I_D

y Parameters vs. V_{G2S}

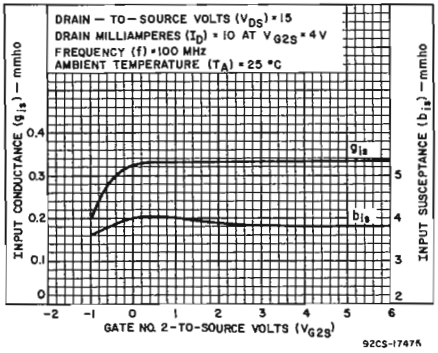


Fig. 16 - y_{is} vs. V_{G2S}

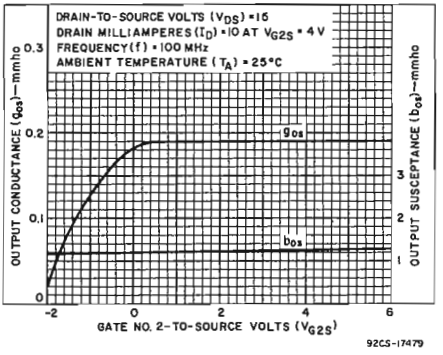


Fig. 17 - y_{os} vs. V_{G2S}

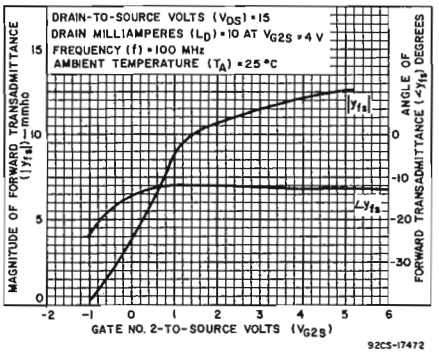


Fig. 18 - y_{fs} vs. V_{G2S}

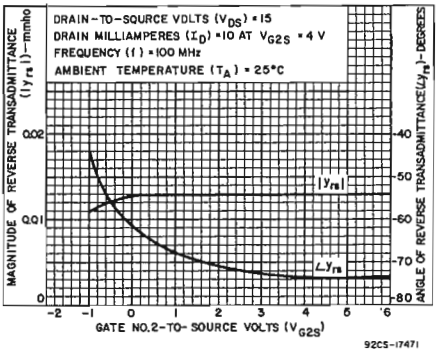


Fig. 19 - y_{rs} vs. V_{G2S}

RCA Solid State Division

MOS Field-Effect Transistors

N-Channel Depletion Types

40841

JEDEC TO-72

Silicon Dual-Insulated Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits

General-Purpose Economy Type for Applications from DC to 500 MHz

Applications:

- DC amplifiers
- RF amplifiers
- mixers
- IF amplifiers
- video amplifiers
- differential amplifiers
- frequency multipliers
- choppers
- voltage-controlled attenuators
- constant-current source
- voltage regulators
- telemetry & multiplex
- servo amplifiers
- proximity switches
- phase splitters
- thyristor trigger circuits
- industrial timers — long time delays

RCA-40841* is an n-channel silicon, depletion type, dual-insulated gate, field-effect transistor intended for general-purpose applications from DC to frequencies up to 500 MHz.

This MOS/FET provides excellent power gain, linear-circuit operation and has a wide dynamic operating range. Its square-law characteristics result in low cross-modulation performance over the AGC range. Its dual-gate construction reduces feedback capacitance by shielding Gate No. 1 from the drain, and makes it possible to isolate the local oscillator signal from the incoming signal by applying the two signals to separate gates. The very low feedback capacitance of this device eliminates the need for neutralization in circuits using the dual-gate configuration. Use of the device in the RF input stage of a receiver reduces local oscillator feed-through to the entenna. The 40841 requires negligible AGC power, provides automatic delay when AGC is applied to Gate No. 2, and exhibits slight input impedance variations during AGC functioning. The device has exceptionally high input impedance, an attribute for timing-circuit design.

Back-to-back diodes are fabricated on the same monolithic silicon pellet as the MOS/FET to protect the gates against damage due to electrostatic charges frequently encountered during normal handling. These back-to-back diodes also function as "transient trappers" by limiting in-circuit transient voltages that exceed ±10 volts.

Maximum ratings and electrical characteristics are included in the data for operation of the 40841 as the equivalent of a single-gate device. For single-gate operation, connect Gate No. 1 (Term. 2) to Gate No. 2 (Term. 3), as shown in the Terminal Diagrams on Page 2. The 40841 MOS/FET is hermetically sealed in the metal JEDEC TO-72 package.

The following dual-gate MOS/FET types are specified for applications requiring premimum-grade performance: 3N200, 3N187, 40673, 40819, 40820, 40821, 40822, and 40823.

Device Features:

- back-to-back diodes protect gate insulation against damage due to static changes frequently encountered during handling
- high forward transconductance: g_{fs} = 12,000 μmho (typ.)
- high power gain: G_{ps} = 32 dB (typ.) at 44 MHz
- gate leakage currents: I_{G1SS} and I_{G2SS} = 60 nA (max.) at $T_A = 25^oC$
- high input impedance
- excellent thermal stability

Performance Features:

- superior cross-modulation performance and greater dynamic range than bipolar and junction-gate FETs
- wide dynamic range permits large-signal handling before overloading
- virtually no agc power required
- greatly reduced spurious responses in AM and FM receivers
- dual-gate configuration permits simplified AGC circuitry
- operates at frequencies to 500 MHz without neutralization in circuits utilizing the dual-gate configuration
- operates up to UHF with low-noise performance

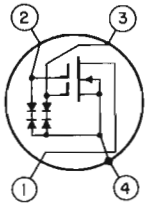
Detailed information, utilizing RCA dual-gate protected MOS/FETs in RF applications, is given in the following RCA Application Notes: AN-4431 "RF Applications of the Dual-Gate MOS/FET up to 500 MHz" and AN-4018 "Design of Gate-Protected MOS Field-Effact Transistors".

* Formerly Developmental Type TA8242.

Maximum Ratings	Dual-Gate Configuration	Single-Gate Configuration	
Absolute Maximum Values, at $T_A = 25^oC$:			
Drain-to-Source Voltage, V_{DS}	−0.2 to +18	−0.2 to +18	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	−	μA
Gate Terminal Current, I_{GS}	−	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+24	−	V
Drain-to-Gate Voltage, V_{DG}	−	+24	V
Drain Current, I_D	50	50	mA
Transistor Dissipation:			
At T_A up to 25°C	330	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C		
Ambient Temperature Range:			
Operating and Storage	−65 to +175	−65 to +175	°C
Lead Temperature (During Soldering):			
At distances 1/32 in from seating surface for 10 s max.	265	265	°C
Continuous Working Voltage#, at $T_A = 25^oC$:			
Gate No. 1-to-Source Voltage, V_{G1S}	−4.5 to +3	−	V
Gate No. 2-to-Source Voltage, V_{G2S}	-4.5 to +4.5 or 40% of V_{DS} (whichever value is less)	−	V
Gate-to-Source Voltage, V_{GS}	−	−4.5 to +3	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+20	−	V
Drain-to-Gate Voltage, V_{DG}	−	+20	V

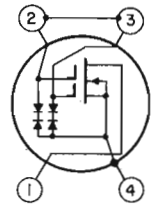
#Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the Absolute Maximum Ratings are not exceeded.

TERMINAL DIAGRAMS



DUAL-GATE CONFIGURATION

LEAD 1—DRAIN
LEAD 2—GATE No.2
LEAD 3—GATE No.1
LEAD 4—SOURCE
SUBSTRATE AND CASE



SINGLE-GATE CONFIGURATION

LEAD 1—DRAIN
LEADS—2 AND 3—GATE
LEAD 4—SOURCE,
SUBSTRATE AND CASE

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CONFIGURATION DUAL-GATE MIN.	DUAL-GATE TYP.	DUAL-GATE MAX.	SINGLE-GATE MIN.	SINGLE-GATE TYP.	SINGLE-GATE MAX.	UNITS
Gate-to-Source Cutoff Voltage:										
Dual-Gate (No. 1)	$V_{G1S(off)}$	V_{DS} = +15V, I_D=200μA, V_{G2S} = +4V		–	–2	–	–	–	–	V
Dual-Gate (No. 2)	$V_{G2S(off)}$	V_{DS} = +15V, I_D=200μA, V_{G1S}=0		–	–2	–	–	–	–	V
Single Gate	$V_{GS(off)}$	V_{DS} = +15V, I_D=200μA		–	–	–	–	–1.6	–	V
Gate-to-Source Forward Breakdown Voltage:		I_{G1SSF} =								
Dual-Gate (No. 1)	$V_{(BR)G1SSF}$	I_{G2SSF} =	$V_{G2S} = V_{DS} = 0$	–	9	–	–	–	–	V
Dual-Gate (No. 2)	$V_{(BR)G2SSF}$	100μA	$V_{G1S} = V_{DS} = 0$	–	9	–	–	–	–	V
Single-Gate	$V_{(BR)GSSF}$	I_{GSSF} = 100μA, V_{DS} = 0		–	–	–	–	9	–	V
Gate-to-Source Reverse Breakdown Voltage:		I_{G1SSR} =								
Dual-Gate (No. 1)	$V_{(BR)G1SSR}$	I_{G2SSR} =	$V_{G2S} = V_{DS} = 0$	–	9	–	–	–	–	V
Dual-Gate (No. 2)	$V_{(BR)G2SSR}$	100μA	$V_{G1S} = V_{DS} = 0$	–	9	–	–	–	–	V
Single-Gate	$V_{(BR)GSSR}$	I_{GSSR} = 100μA, V_{DS} = 0		–	–	–	–	9	–	V
Gate Terminal Forward Current:										
Dual-Gate (No. 1)	I_{G1SSF}	$V_{DS} = V_{G2S} = 0$, V_{G1S} = 6 V		–	–	60	–	–	–	nA
Dual Gate (No. 2)	I_{G2SSF}	$V_{DS} = V_{G1S} = 0$, V_{G2S} = 6 V		–	–	60	–	–	–	nA
Single-Gate	I_{GSSF}	V_{DS} = 0, V_{GS} = 6 V		–	–	–	–	–	120	nA
Gate Terminal Reverse Current:										
Dual-Gate (No. 1)	I_{G1SSR}	$V_{DS} = V_{G2S} = 0$, V_{G1S} = –6 V		–	–	60	–	–	–	nA
Dual-Gate (No. 2)	I_{G2SSR}	$V_{DS} = V_{G1S} = 0$, V_{G2S} = –6 V		–	–	60	–	–	–	nA
Single-Gate	I_{GSSR}	V_{DS} = 0, V_{GS} = –6 V		–	–	–	–	–	120	nA
Zero-Bias Drain Current:										
Dual-Gate	I_{DS}	V_{DS} = +15 V, V_{G1S} = 0, V_{G2S} = +4 V		–	10	–	–	–	–	mA
Single-Gate	I_{DSS}	V_{DS} = +15 V, V_{GS} = 0		–	–	–	–	3.7	–	mA
Forward Transconductance (Gate-to-Drain)†										
Dual-Gate	g_{fs}		1 kHz	–	12000	–	–	–	–	μmho
Single-Gate	g_{fs}			–	–	–	–	7000	–	μmho
Small-Signal, Short-Circuit Input Capacitance†	C_{iss}		f = 1 MHz	–	6.5	–	–	11	–	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦	C_{rss}	V_{DS} = +15 V, I_D = 10 mA		–	0.02	–	–	0.64	–	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}	[Dual-Gate only V_{G2S} = +4 V]		–	2	–	–	2	–	pF
Audio Spot Noise Figure*										
Dual-Gate	NF		f = 1 kHz	–	0.46	–	–	–	–	dB
Single-Gate	NF		f = 1 kHz	–	–	–	–	0.29	–	dB
Power Gain	G_{ps}		44 MHz	–	32	–	–	–	–	dB
Conversion Gain	$G_{ps(C)}$			–	24	–	–	–	–	dB

† Capacitance between Gate No. 1 and all other terminals (Dual-Gate), Gate and all other terminals (Single-Gate)

♦ Three-terminal measurement with Gate No. 2 and Source returned to guard terminal (Dual-Gate)

* Noise Figure = $10 \log_{10}\left[1 + \frac{e_n^2}{4\,KT\,BW\,R_g}\right]$ where K = 1.38×10^{-23}; T = Temperature in °Kelvin; BW = Bandwidth in Hz; R_g = Generator resistance

TYPICAL CHARACTERISTICS FOR 40841 IN DUAL-GATE CONFIGURATION

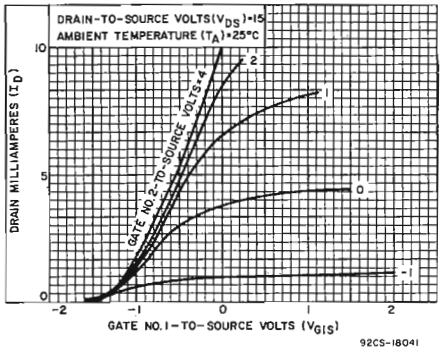


Fig.1–I_D vs. V_{G1S}.

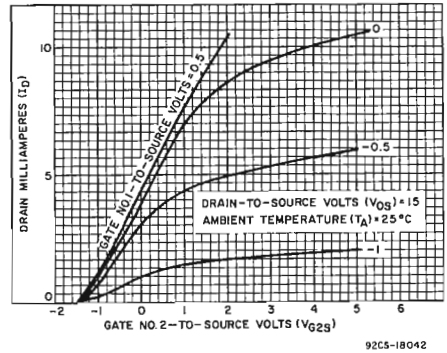


Fig.2–I_D vs. V_{G2S}.

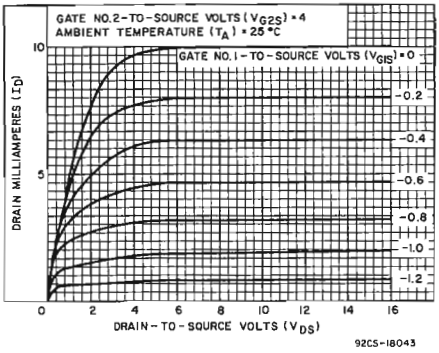


Fig.3–I_D vs. V_{DS}.

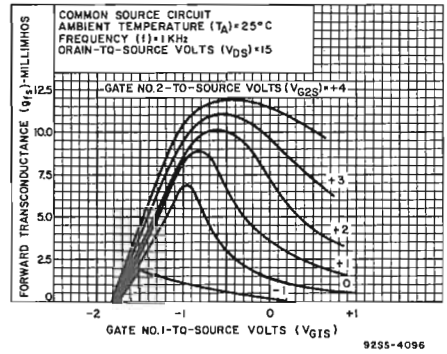


Fig.4–g_{fs} vs. V_{G1S}.

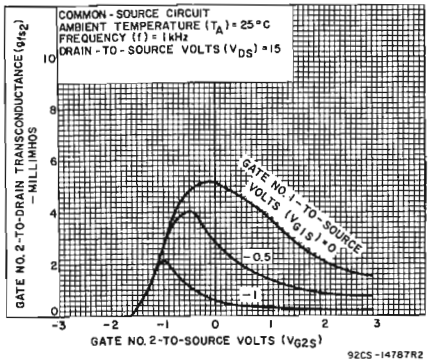


Fig.5–g_{fs2} vs. V_{G2S}.

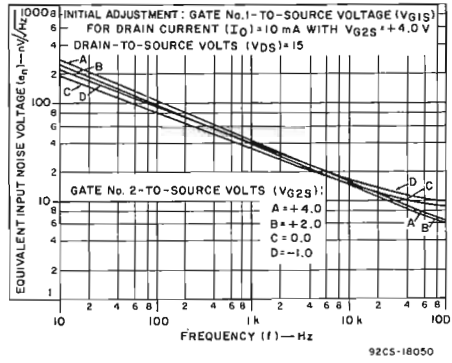


Fig.6–e_n vs. f.

TYPICAL CHARACTERISTICS FOR 40841 IN SINGLE-GATE CONFIGURATION
(Terminals 2 and 3 tied together to comprise effective single-gate)

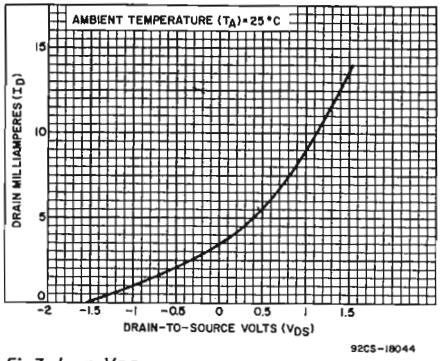


Fig.7—I_D vs. V_{DS}.

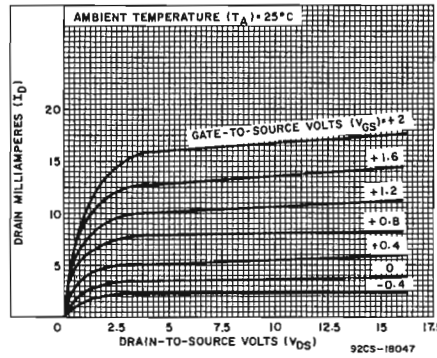


Fig.8—I_D vs. V_{DS}.

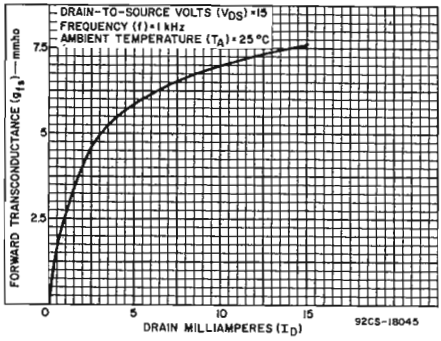


Fig.9—g_{fs} vs. I_D.

TYPICAL CHARACTERISTICS FOR 40841 IN SINGLE-GATE & DUAL-GATE CONFIGURATION

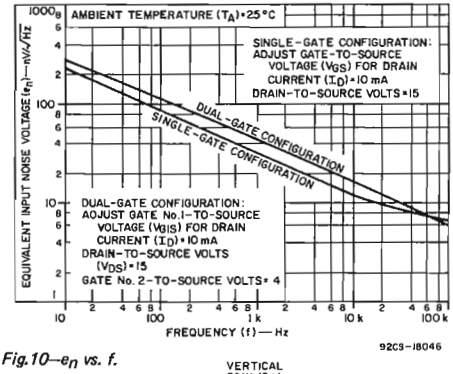


Fig.10—e_n vs. f.

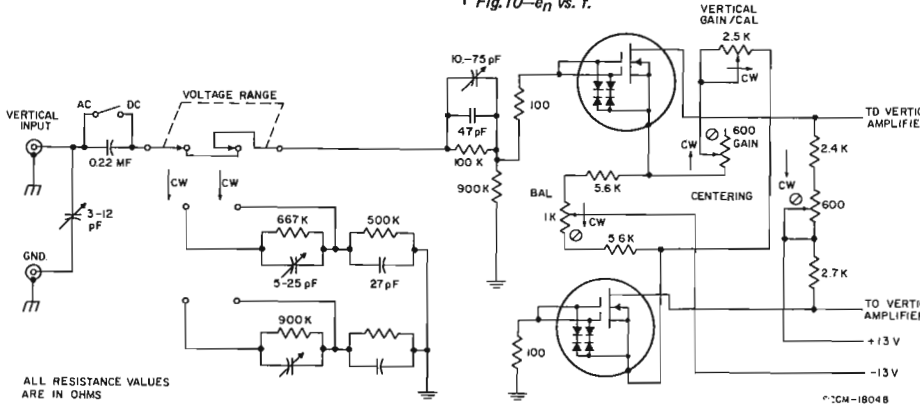
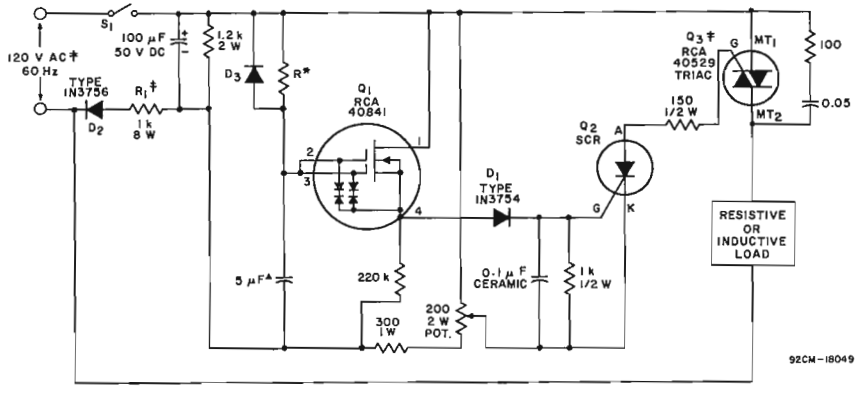


Fig.11—Typical differential amplifier utilizing the 40841 in the vertical input stage of a solid-state oscilloscope.

SOLID-STATE TIMER FOR INDUSTRIAL APPLICATIONS



▲ Cornell-Dubilier Electronics—Type MMW or equivalent.

* R controls duration of time delay. At R = 60 MΩ up to 5-minute delay (IRC resistor, Type CGH or equivalent)

‡ This circuit can also be used at supply voltages of 240 V AC and 24V AC (60Hz) by changing the values of R1 and Q3.

TIMING CIRCUIT CHARACTERISTICS

$T_A = -25^oC$ to $+60^oC$
Accuracy: ±10% (over temperature)
Repeatability: ±3% (at 25^oC)
Reset Time: Less than 160 ms

Q2: $V_{DRM} = 60V$
$I_{GT} = 200\mu A$
$I_T = 0.8A$

D3: $I_R = 1nA$
$V_R = 60V$

Fig.12—Typical timing circuit utilizing the 40841 in a single-gate configuration.

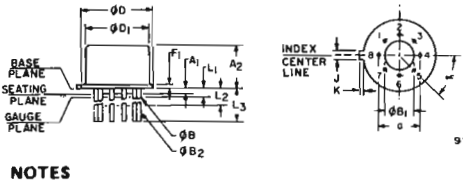
OPERATING CONSIDERATIONS

The flexible leads of the 40841 are usually soldered to the circuit elements. As in the case with any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.

Dimensional Outlines

DIMENSIONAL OUTLINES FOR LINEAR INTEGRATED CIRCUITS AND MOS/FET'S

JEDEC MO-002-AL 8-LEAD TO-5 STYLE

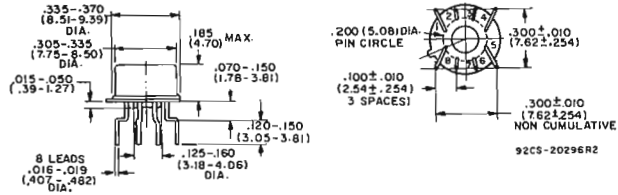


SYMBOL	INCHES MIN	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
a	0.200 TP		2	5.88 TP	
A_1	0.010	0.050		0.26	1.27
A_2	0.165	0.185		4.20	4.69
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0.125	0.160		3.18	4.06
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	45° TP			45° TP	
N	8		6	8	
N_1	3		5	3	

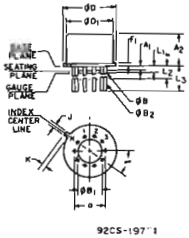
NOTES

1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178mm) radius of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

8-LEAD TO-5 STYLE WITH DUAL-IN-LINE FORMED LEADS (DIL-CAN)



10-LEAD TO-5 STYLE PACKAGE JEDEC MO-006-AF

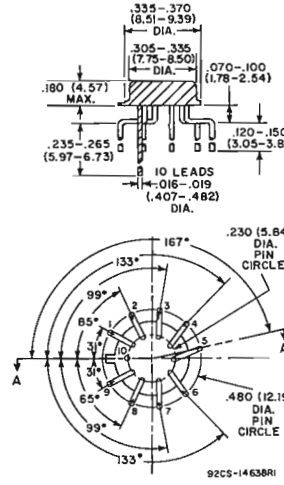


SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
a	0.230 TP		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0	0		0	0
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	36° TP			36° TP	
N	10		6	10	
N_1	1		5	1	

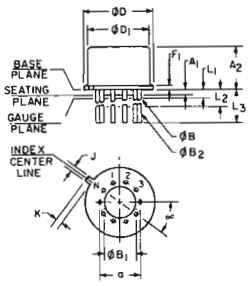
NOTES:

1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diamerer is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

10 FORMED LEADS RADIALLY ARRANGED TO-5 TYPE



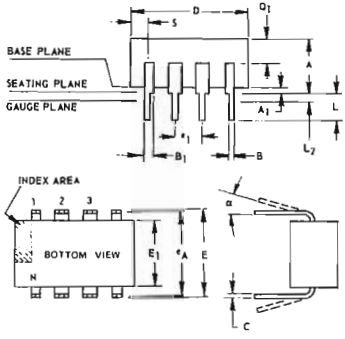
12-LEAD TO-5 STYLE PACKAGE JEDEC MO-006-AG



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0	0		0	0
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
.	30 TP			30 TP	
N	12		6	12	
N_1	1		5	1	

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

8-LEAD DUAL-IN-LINE PLASTIC PACKAGE (MINI-DIP)



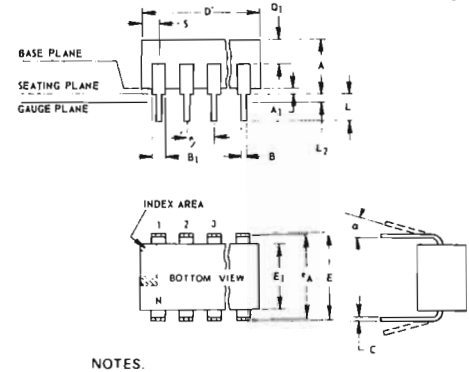
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.889	1.65
C	0.008	0.012*		0.203	0.304
D	0.370	0.400		9.40	10.16
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.762
α	0°	15°	4	0°	15°
N	8		5	8	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.381	1.52

NOTES:
1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

* When device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

92CS-24026

8-LEAD DUAL-IN-LINE FRIT-SEAL PACKAGE

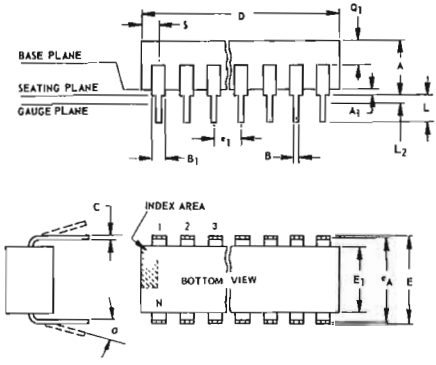


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012		0.203	0.304
D	0.376	0.396		9.55	10.05
E	0.315	0.345		8.00	8.76
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.100	0.150		2.54	3.81
L_2	0.000	0.030		0.000	0.762
α	0°	15°	4	0°	15°
N	8		5	8	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.020	0.060		0.508	1.52

92CM-20827

NOTES.
1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

14-LEAD DUAL-IN-LINE PLASTIC AND FRIT-SEAL PACKAGE
JEDEC MO-001-AB



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	●0.012		0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.68	2.28

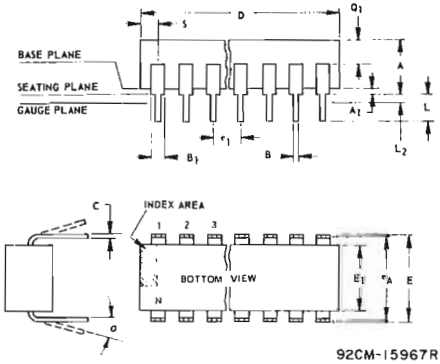
92SS-4296RI

NOTES:

1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

● When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

16-LEAD DUAL-IN-LINE PLASTIC AND FRIT- SEAL PACKAGE
JEDEC MO-001-AC



92CM-15967RI

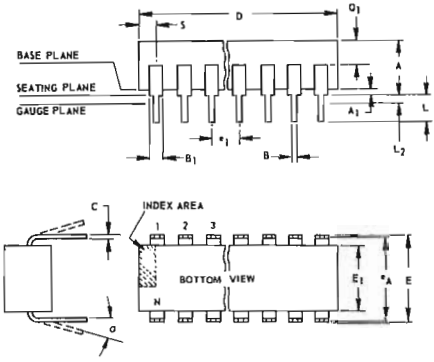
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	●0.012		0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

NOTES:

1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

● When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

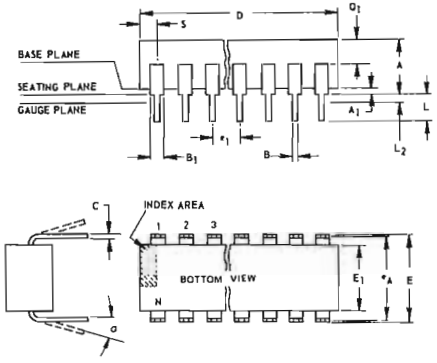
14-LEAD DUAL-IN-LINE CERAMIC PACKAGE JEDEC MO-001-AD



SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	●0.012		0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.65	2.28

92SS-4411R1

16-LEAD DUAL-IN-LINE CERAMIC PACKAGE JEDEC MO-001-AE



SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	●0.012		0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.78
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

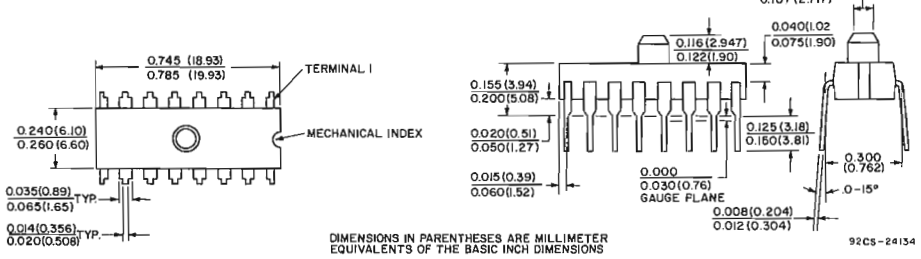
92SS-4286R3

Notes for 14- and 16-Lead Dual-in-Line Ceramic Packages

1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

●When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

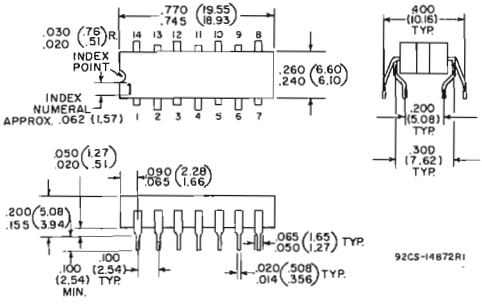
16-LEAD DUAL-IN-LINE "POWER-STUD" PLASTIC PACKAGE

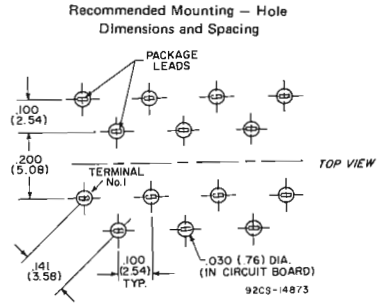


DIMENSIONS IN PARENTHESES ARE MILLIMETER EQUIVALENTS OF THE BASIC INCH DIMENSIONS

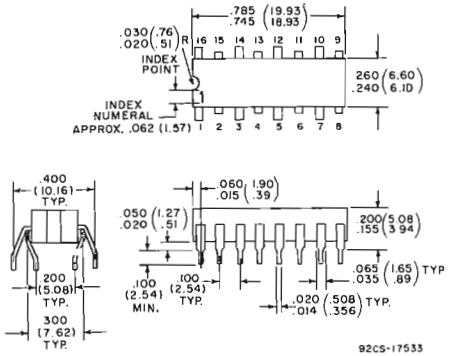
92CS-24134

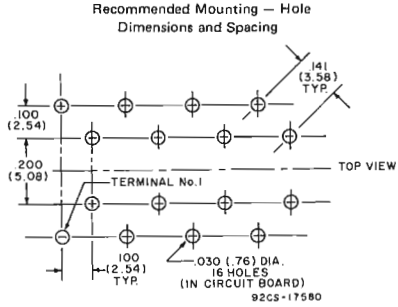
14-LEAD QUAD-IN-LINE PLASTIC PACKAGE



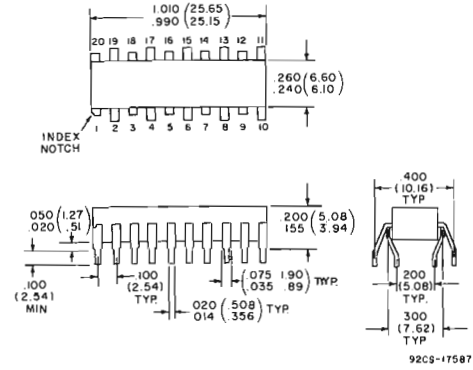


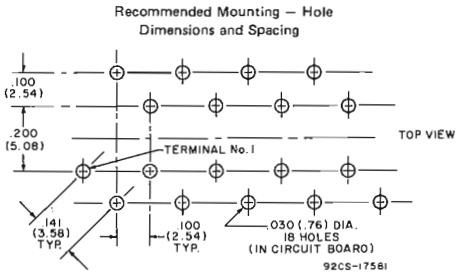
16-LEAD QUAD-IN-LINE PLASTIC PACKAGE



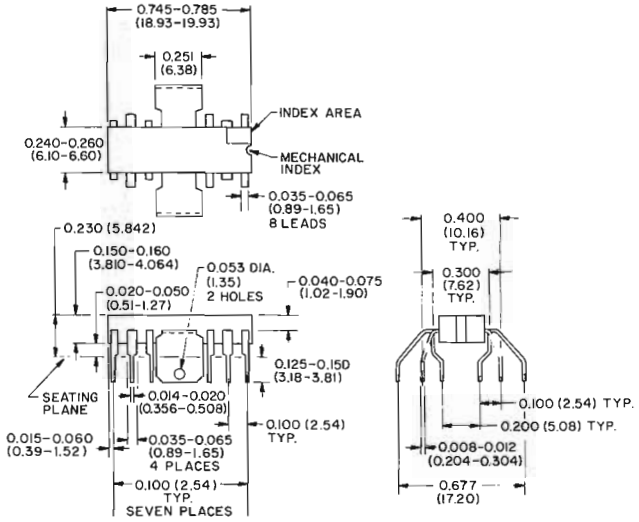


20-LEAD QUAD-IN-LINE PLASTIC PACKAGE





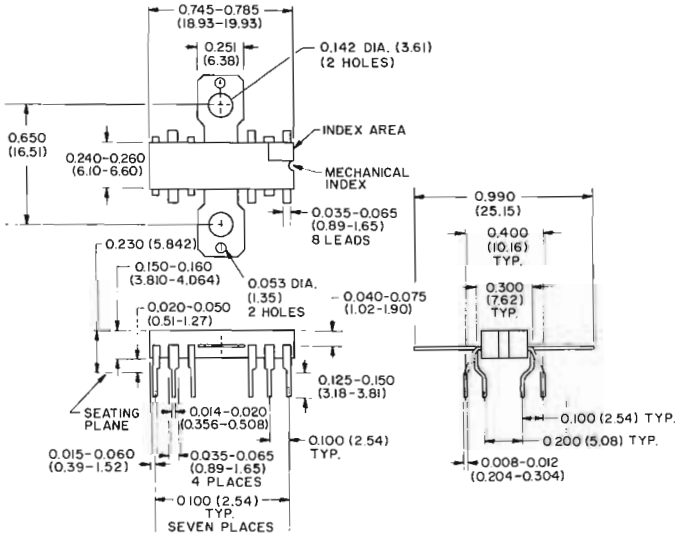
MODIFIED 16-LEAD QUAD-IN-LINE PLASTIC PACKAGE WITH INTEGRAL BENT DOWN WING-TAB HEAT SINK



DIMENSIONS IN PARENTHESES ARE MILLIMETER EQUIVALENTS OF THE BASIC INCH DIMENSIONS

92CM-25044

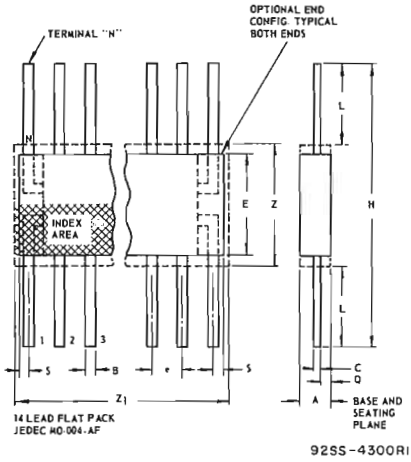
MODIFIED 16-LEAD QUAD-IN-LINE PLASTIC PACKAGE WITH INTEGRAL FLAT WING-TAB HEAT SINK



DIMENSIONS IN PARENTHESES ARE MILLIMETER EQUIVALENTS OF THE BASIC INCH DIMENSIONS

92CM-25045

14-LEAD CERAMIC FLAT PACKAGE JEDEC MO-004AF

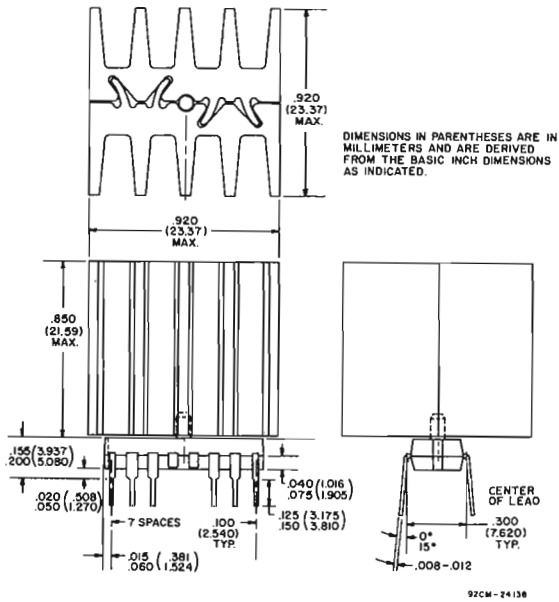


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

NOTES:

1. Refer to Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

MODIFIED 16-LEAD DUAL-IN-LINE PLASTIC PACKAGE WITH INTEGRAL HEAT SINK



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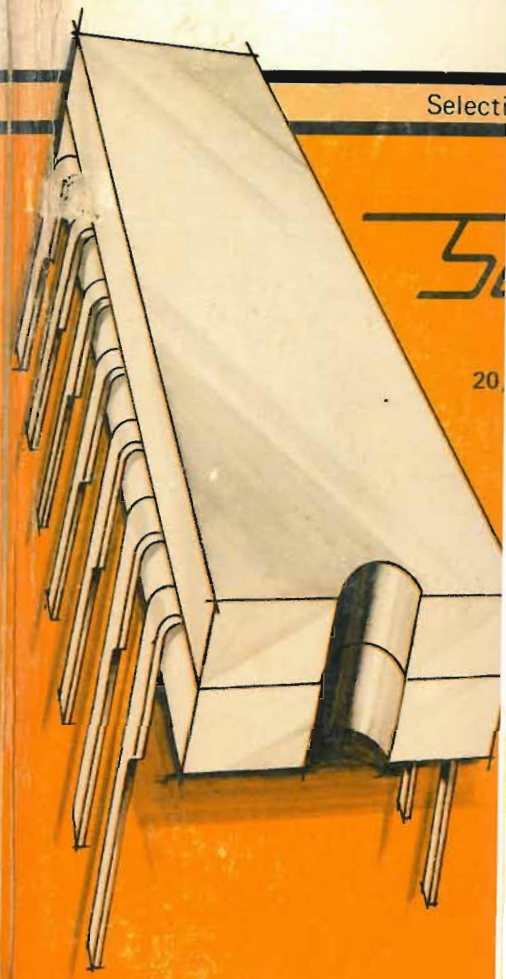

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